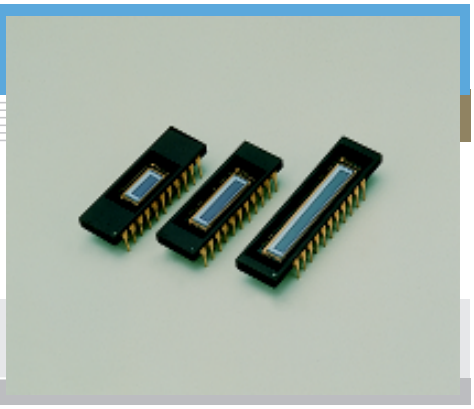


NMOS linear image sensor
S3921/S3924 series

Voltage output type with current-integration readout circuit and impedance conversion circuit

NMOS linear image sensors are self-scanning photodiode arrays designed specifically as detectors for multichannel spectroscopy. The scanning circuit is made up of N-channel MOS transistors, operates at low power consumption and is easy to handle. Each photodiode has a large active area, high UV sensitivity yet very low noise, delivering a high S/N even at low light levels. NMOS linear image sensors also offer excellent output linearity and wide dynamic range.

S3921/S3924 series have a current-integration readout circuit utilizing the video line and an impedance conversion circuit. The output is available in boxcar waveform allowing signal readout with a simple external circuit.

The photodiodes of S3921 series have a height of 2.5 mm and are arrayed in a row at a spacing of 50 µm. The photodiodes of S3924 series also have a height of 2.5 mm but are arrayed at a spacing of 25 µm. The photodiodes are available in 3 different pixel quantities for each series, 128 (S3921-128Q), 256 (S3921-256Q, S3924-256Q) and 512 (S3921-512Q, S3924-512Q) and 1024 (S3924-1024Q). Quartz glass is the standard window material.

Features

- Built-in current-integration readout circuit utilizing video line capacitance and impedance conversion circuit (boxcar waveform output)
- Wide active area
  Pixel pitch: 50 µm (S3921 series)
  25 µm (S3924 series)
  Pixel height: 2.5 mm
- High UV sensitivity with good stability
- Low dark current and high saturation charge allow a long integration time and a wide dynamic range at room temperature
- Excellent output linearity and sensitivity spatial uniformity
- Low voltage, single power supply operation
- Start pulse, clock pulse and video line reset pulse are CMOS logic compatible

Applications

- Multichannel spectrophotometry
- Image readout system

Figure 1 Equivalent circuit

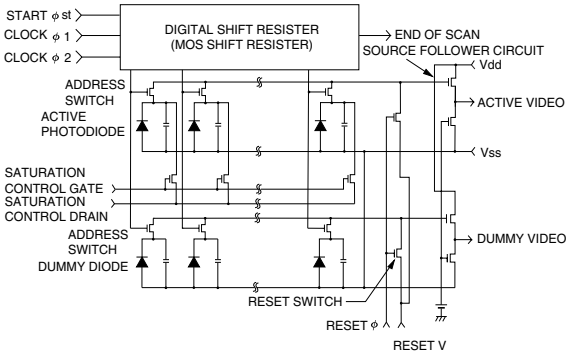
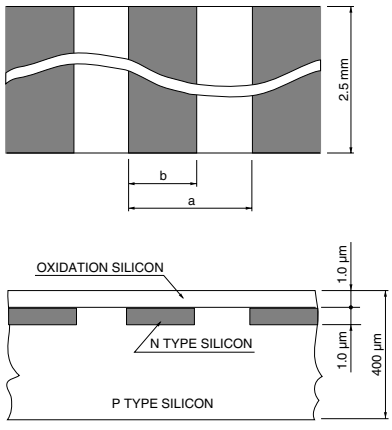


Figure 2 Active area structure



■ Absolute maximum ratings

Parameter	Symbol	Value	Unit
Supply voltage	Vdd	15	V
Input pulse (φ1, φ2, φst) voltage	Vφ	15	V
Power consumption *1	P	10	mW
Operating temperature *2	Topr	-40 to +65	°C
Storage temperature	Tstg	-40 to +85	°C

*1: Vdd=5 V, Vr=2.5 V
*2: No condensation

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■ Shape specifications

Parameter	S3921-128Q	S3921-256Q	S3921-512Q	S3924-256Q	S3924-512Q	S3924-1024Q	Unit
Number of pixels	128	256	512	256	512	1024	-
Package length	31.75		40.6	31.75		40.6	mm
Number of pin	22			22			-
Window material *3	Quartz			Quartz			-
Weight	3.0		3.5	3.0		3.5	g

*3: Fiber optic plate is available.

■ Specifications (Ta=25 °C)

Parameter	Symbol	S3921 series			S3924 series			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Pixel pitch	-	-	50	-	-	25	-	μm
Pixel height	-	-	2.5	-	-	2.5	-	mm
Spectral response range (10 % of peak)	λ	200 to 1000			200 to 1000			nm
Peak sensitivity wavelength	λp	-	600	-	-	600	-	nm
Photodiode dark current *4	ID	-	0.2	0.6	-	0.1	0.3	pA
Photodiode capacitance *4	Cph	-	20	-	-	10	-	pF
Saturation exposure *4, *5	Esat	-	220	-	-	220	-	mlx· s
Saturation charge *4	Qsat	-	50	-	-	25	-	pC
Saturation output voltage *4	Vsat	-	1350 (-128Q)	-	-	1050 (-256Q)	-	mV
		-	1300 (-256Q)	-	-	820 (-512Q)	-	mV
		-	1100 (-512Q)	-	-	570 (-1024Q)	-	mV
Photo response non-uniformity *6	PRNU	-	-	±3	-	-	±3	%

*4: Reset V=2.5 V, Vdd=5.0 V, Vϕ=5.0 V
*5: 2856 K, tungsten lamp
*6: 50 % of saturation, excluding the start pixel and last pixel

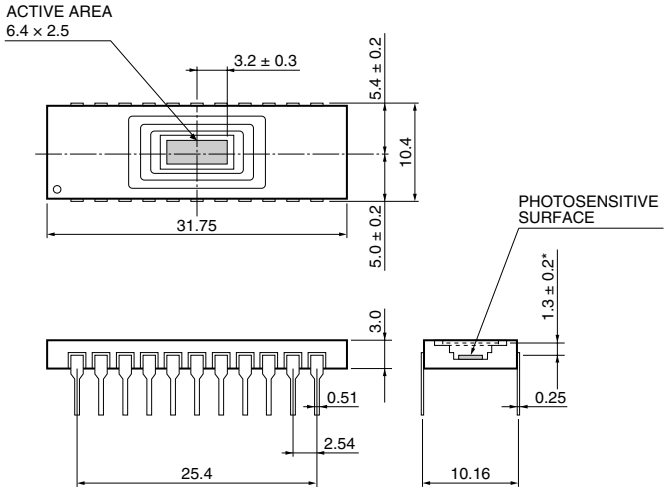
■ Electrical characteristics (Ta=25 °C)

Parameter		Symbol	Condition	S3921 series			S3924 series			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock pulse (ϕ1, ϕ2) voltage	High	Vϕ1, Vϕ2 (H)	-	4.5	5	10	4.5	5	10	V
	Low	Vϕ1, Vϕ2 (L)	-	0	-	0.4	0	-	0.4	V
Start pulse (ϕst) voltage *7	High	Vϕs (H)	-	4.5	Vϕ	10	4.5	Vϕ	10	V
	Low	Vϕs (L)	-	0	-	0.4	0	-	0.4	V
Reset pulse (Reset ϕ) voltage *7	High	Vrϕ (H)	-	4.5	Vϕ	10	4.5	Vϕ	10	V
	Low	Vrϕ (L)	-	0	-	0.4	0	-	0.4	V
Source follower circuit drain voltage *7		Vdd	-	4.5	Vϕ	10	4.5	Vϕ	10	V
Reset voltage (Reset V) *8		Vr	-	2.0	Vϕ - 2.5	Vϕ - 2.0	2.0	Vϕ - 2.5	Vϕ - 2.0	V
Saturation control gate voltage		Vscg	-	-	0	-	-	0	-	V
Saturation control drain voltage *8		Vscd	-	-	Vr	-	-	Vr	-	V
Clock pulse (ϕ1, ϕ2) rise / fall time		trϕ1, trϕ2 tfϕ1, tfϕ2	-	-	20	-	-	20	-	ns
Clock pulse (ϕ1, ϕ2) pulse width		tpwϕ1, tpwϕ2	-	200	-	-	200	-	-	ns
Start pulse (ϕst) rise / fall time		trϕs, tfϕs	-	-	20	-	-	20	-	ns
Start pulse (ϕst) pulse width		tpwϕs	-	200	-	-	200	-	-	ns
Reset pulse rise / fall time		trrϕ, tfrϕ	-	-	20	-	-	20	-	ns
Start pulse (ϕst) and clock pulse (ϕ2) overlap		tϕov	-	200	-	-	200	-	-	ns
Clock pulse (ϕ2) and reset pulse (Reset ϕ) overlap		tϕovr	-	660	-	-	660	-	-	ns
Clock pulse (ϕ2) and reset pulse (Reset ϕ) delay time		tdϕr-2	-	50	-	-	50	-	-	ns
Clock pulse (ϕ1, ϕ2) space *9		X1, X2	-	trf - 20	-	-	trf - 20	-	-	ns
Clock pulse (ϕ2, Reset ϕ) space *9		tsϕr-2	-	0	-	-	0	-	-	ns
Data rate *10		f	-	0.1	-	500	0.1	-	500	kHz
Video delay time		tvd	50 % of saturation *10	-	100 (-128 Q)	-	-	100 (-256 Q)	-	ns
				-	150 (-256 Q)	-	-	150 (-512 Q)	-	ns
				-	200 (-512 Q)	-	-	200 (-1024 Q)	-	ns
Clock pulse (ϕ1, ϕ2) line capacitance		Cϕ	5 V bias	-	21 (-128 Q)	-	-	27 (-256 Q)	-	pF
				-	36 (-256 Q)	-	-	50 (-512 Q)	-	pF
				-	67 (-512 Q)	-	-	100 (-1024 Q)	-	pF
Reset pulse (Reset ϕ) line capacitance		Cr	5 V bias	-	6	-	-	6	-	pF
Saturation control gate (Vscg) line capacitance		Cscg	5 V bias	-	12 (-128 Q)	-	-	14 (-256 Q)	-	pF
				-	20 (-256 Q)	-	-	24 (-512 Q)	-	pF
				-	35 (-512 Q)	-	-	45 (-1024 Q)	-	pF
Output impedance		Zo	Vdd=5 V Vr=2.5 V	-	200	-	-	200	-	Ω

*7: Vϕ is input pulse voltage (refer to figure 8)
*8: Terminal pin 7 is used for both Reset V and saturation control drain voltage
*9: trf is the clock pulse rise or fall time. A clock pulse space of "rise time/fall time - 20" ns (nanoseconds) or more should be input if the clock pulse rise or fall time is longer than 20 ns. (refer to figure 7)
*10: Reset V=2.5 V, Vdd=5.0 V, Vϕ=5.0 V

Figure 3 Dimensional outlines (unit: mm)

S3921-128Q, S3924-256Q



* Optical distance from the outer surface of the quartz window to the chip surface

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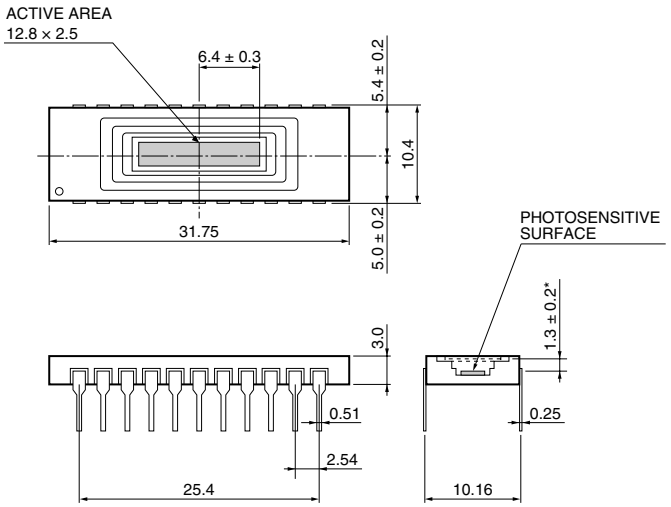
S3921-256Q, S3924-512Q



* Optical distance from the outer surface of the quartz window to the chip surface

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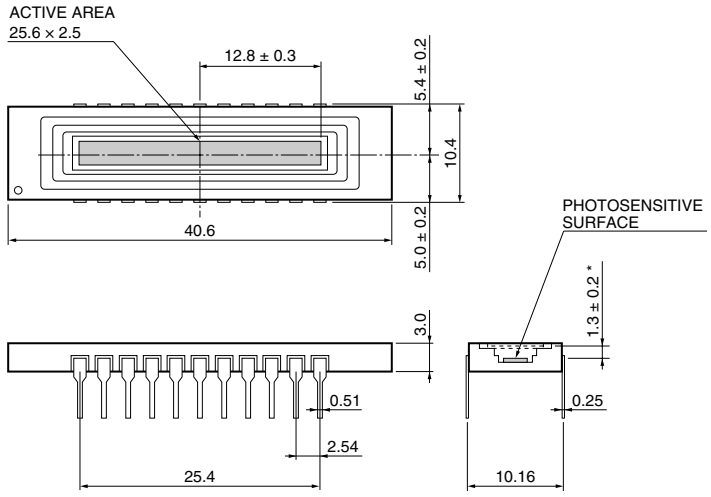
S3921-512Q, S3924-1024Q



* Optical distance from the outer surface of the quartz window to the chip surface

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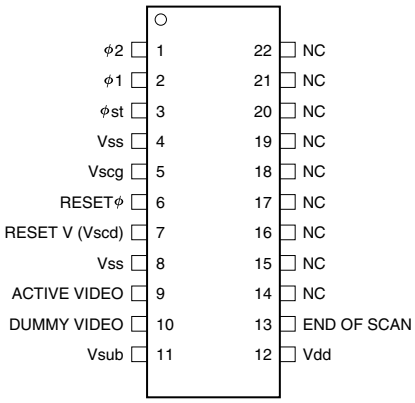
Figure 4 Pin connection



Vss, Vsub and NC should be grounded.

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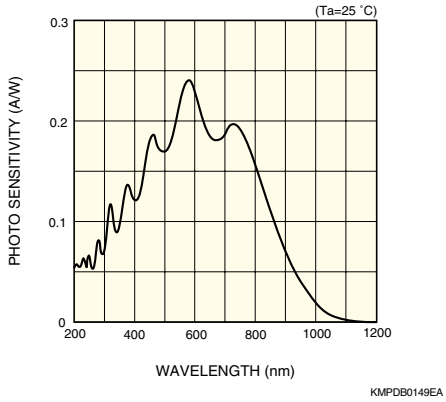
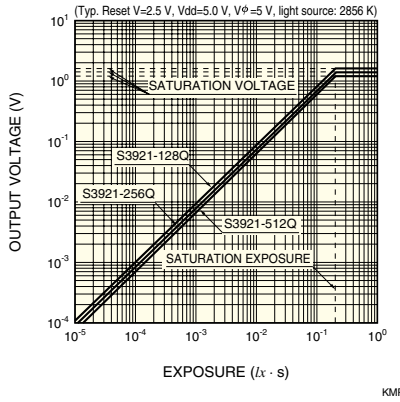
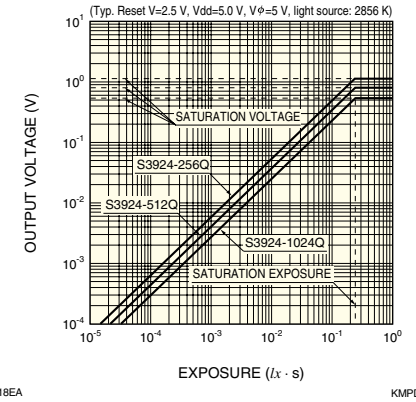
Terminal	Input or output	Description
ϕ1, ϕ2	Input (CMOS logic compatible)	Pulses for operating the MOS shift register. The video data rate is equal to the clock pulse frequency since the video output signal is obtained synchronously with the rise of ϕ2 pulse.
ϕst	Input (CMOS logic compatible)	Pulse for starting the MOS shift register operation. The time interval between start pulses is equal to the signal accumulation time.
Vss	-	Connected to the anode of each photodiode. This should be grounded.
Vscg	Input	Used for restricting blooming. This should be grounded.
Reset ϕ	Input (CMOS logic compatible)	With Reset ϕ at high level, the video line is reset at the Reset V voltage.
Reset V	Input	The Reset V terminal connects to each photodiode cathode via the video line when the address turns on. A positive voltage should be applied to the Reset V terminal to use each photodiode at a reverse bias. Setting the Reset V voltage to 2.5 V is recommended when the amplitude of ϕ1, ϕ2 and Reset ϕ is 5 V. Terminal pin 7 is used for both Reset V and Vscd.
Vscd	Input	Used for restricting blooming. This should be biased at a voltage equal to “Reset V”.
Active video	Output	Low-impedance video output signal after internal current-voltage conversion. Negative-going output including DC offset.
Dummy video	Output	This has the same structure as the active video, but is not connected to photodiodes, so only DC offset is output. Leave this terminal open when not used.
Vsub	-	Connected to the silicon substrate. This should be grounded.
Vdd	Input	Supply voltage to the internal impedance conversion circuit. A voltage equal to the amplitude of each clock should be applied to this terminal.
End of scan	Output (CMOS logic compatible)	This should be pulled up at 5 V by using a 10 kΩ resistor. This is a negative going pulse that appears synchronously with the ϕ2 timing right after the last photodiode is addressed.
NC	-	Should be grounded.

Figure 5 Spectral response (typical example) Figure 6 Output voltage vs. exposure







■ Construction of image sensor

The NMOS image sensor consists of a scanning circuit made up of MOS transistors, a photodiode array, and a switching transistor array that addresses each photodiode, all integrated onto a monolithic silicon chip. Figure 1 shows the circuit of a NMOS linear image sensor.

The MOS scanning circuit operates at low power consumption and generates a scanning pulse train by using a start pulse and 2-phase clock pulses in order to turn on each address sequentially. Each address switch is comprised of an NMOS transistor using the photodiode as the source, the video line as the drain and the scanning pulse input section as the gate.

The photodiode array operates in charge integration mode so that the output is proportional to the amount of light exposure (light intensity × integration time).

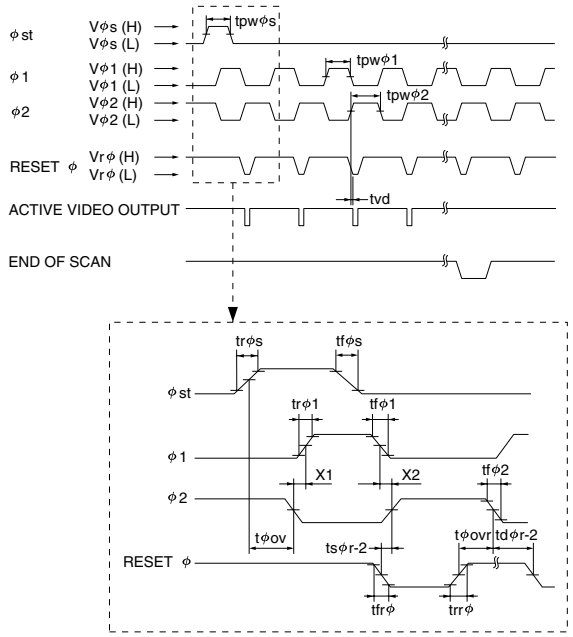
Each cell consists of an active photodiode and a dummy diode, which are respectively connected to the active video line and the dummy video line via a switching transistor. Each of the active photodiodes is also connected to the saturation control drain via the saturation control gate, so that the photodiode blooming can be suppressed by grounding the saturation control gate. Applying a pulse signal to the saturation control gate triggers all reset. (See “Auxiliary functions”.)

Figure 2 shows the schematic diagram of the photodiode active area. This active area has a PN junction consisting of an N-type diffusion layer formed on a P-type silicon substrate. A signal charge generated by light input accumulates as a capacitive charge in this PN junction. The N-type diffusion layer provides high UV sensitivity but low dark current.

■ Driver circuit

A start pulse φst and 2-phase clock pulses φ1, φ2 are needed to drive the shift register. These start and clock pulses are positive going pulses and CMOS logic compatible.
The 2-phase clock pulses φ1, φ2 can be either completely separated or complementary. However, both pulses must not be "High" at the same time.
A clock pulse space (X_1 and X_2 in Figure 7) of a "rise time/fall time - 20" ns or more should be input if the rise and fall times of φ1, φ2 are longer than 20 ns. The φ1 and φ2 clock pulses must be held at "High" at least 200 ns. Since the photodiode signal is obtained at the rise of each φ2 pulse, the clock pulse frequency will equal the video data rate.
The amplitude of start pulse φst is the same as the φ1 and φ2 pulses. The shift register starts the scanning at the "High" level of φst, so the start pulse interval is equal to signal accumulation time. The φst pulse must be held "High" at least 200 ns and overlap with φ2 at least for 200 ns. To operate the shift register correctly, φ2 must change from the "High" level to the "Low" level only once during "High" level of φst. The timing chart for each pulse is shown in Figure 7.

Figure 7 Timing chart for driver circuit



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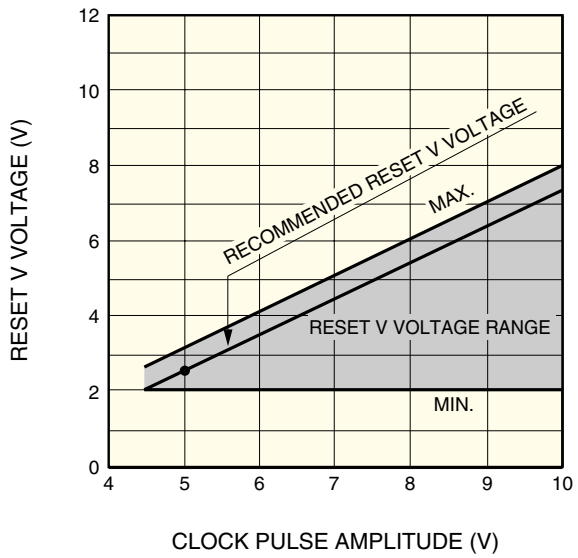
■ End of scan

The end of scan ($\overline{EOS}$) signal appears in synchronization with the φ2 timing right after the last photodiode is addressed, and the $\overline{EOS}$ terminal should be pulled up at 5 V using a 10 kΩ resistor.

Figure 8 Reset V voltage margin



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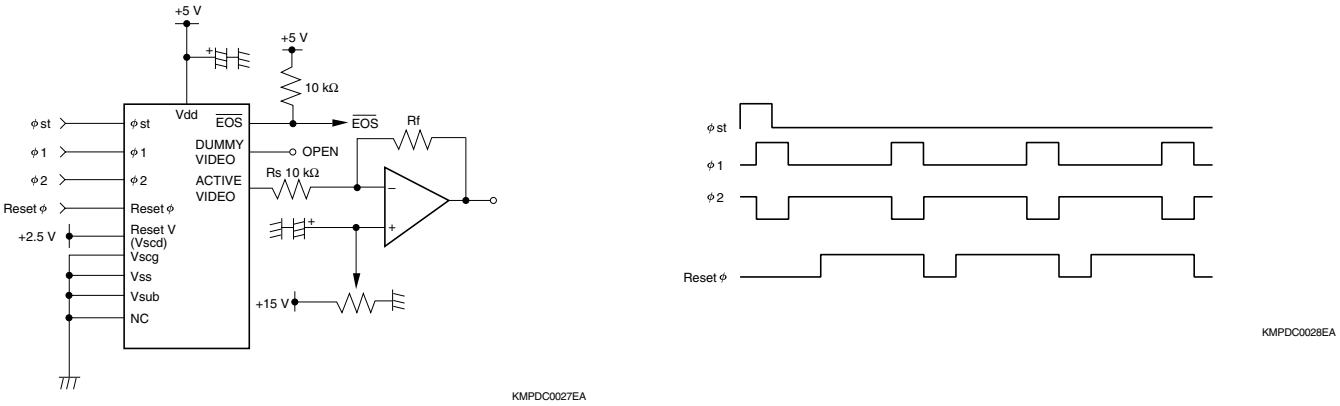
■ Signal readout circuit

S3921/S3924 series include a current integration circuit utilizing the video line capacitance and an impedance conversion circuit. This allows signal readout with a simple external circuit. However, a positive bias must be applied to the video line because the photodiode anode of NMOS linear image sensors is at 0 V (Vss). This is done by adding an appropriate pulse to the reset φ terminal. The amplitude of the reset pulse should be equal to φ1, φ2 and φst.
When the reset pulse is at the high level, the video line is set at the Reset V voltage. Figure 8 shows the Reset V voltage margin. A higher clock pulse amplitude allows higher Reset V voltage and saturation charge. Conversely, if the Reset V voltage is set at a low level with a higher clock pulse amplitude, the rise and fall times of video output waveform can be shortened. Setting the Reset V voltage to 2.5 V is recommended when the amplitude of φ1, φ2, φst and Reset φ is 5 V.
To obtain a stable output, an overlap between the reset pulse (Reset φ) and φ2 must be settled. (Reset φ must rise while φ2 is at the high level.) Furthermore, Reset φ must fall while φ2 is at the low level.
S3921/S3924 series provide output signals with negative-going boxcar waveform which include a DC offset of approximately 1 V when Reset V is 2.5 V. If you want to remove the DC offset to obtain the positive-going output, the signal readout circuit and pulse timing shown in Figure 9 are recommended. In this circuit, Rs must be larger than 10 kΩ. Also, the gain is determined by the ratio of Rf to Rs, so choose the Rf value that suits your application.

Hamamatsu provides the following driver circuits and related products (sold separately).

Product name	Type No.	Content	Feature
Driver circuit	C7885	Low cost driver circuit	Low price Single power supply (+15 V) operation Boxcar waveform output
	C7885G	C7885 + C8225-02	
Pulse generator	C8225-02	C7885 series	
Cable	A8226	C7883 to C7885 series	BNC, length 1 m

Figure 9 Readout circuit example and timing chart



■ Anti-blooming function

If the incident light intensity is higher than the saturation charge level, even partially, a signal charge in excess of the saturation charge cannot accumulate in the photodiode. This excessive charge flows out into the video line degrading the signal purity. To avoid this problem and maintain the signal purity, applying the same voltage as the Reset V voltage to the saturation control drain and grounding the saturation control gate are effective. If the incident light intensity is extremely high, a positive bias should be applied to the saturation control gate. The larger the voltage applied to the saturation control gate, the higher the function for suppressing the excessive saturation charge will be. However, this voltage also lowers the amount of saturation charge, so an optimum bias voltage should be selected.

■ Auxiliary functions

1) All reset

In normal operation, the accumulated charge in each photodiode is reset when the signal is read out. Besides this method that uses the readout line, S3921/S3924 series can reset the photodiode charge by applying a pulse to the saturation control gate. The amplitude of this pulse should be equal to the φ1, φ2, φst, Reset φ pulses and the pulse width should be longer than 5 μs. When the saturation control gate is set at the “High” level, all photodiodes are reset to the saturation control drain potential. Conversely, when the saturation control gate is set at the “Low” level (0 V), the signal charge accumulates in each photodiode without being reset.

2) Dummy video

S3921/S3924 series have a dummy video line. Positive-polarity video signals with the DC offset remove can be obtained by differential amplification of the active video line and dummy video line outputs. When not needed, leave this unconnected.

■ Precautions for using NMOS linear image sensors

1) Electrostatic countermeasures

NMOS linear image sensors are designed to resist static electrical charges. However, take sufficient cautions and countermeasures to prevent damage from static charges when handling the sensors.

2) Window

If dust or grime sticks to the surface of the light input window, it appears as a black blemish or smear on the image. Before using the image sensor, the window surface should be cleaned. Wipe off the window surface with a soft cloth, cleaning paper or cotton swab slightly moistened with organic solvent such as alcohol, and then lightly blow away with compressed air. Do not rub the window with dry cloth or cotton swab as this may generate static electricity.

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