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MICROCIRCUIT DATA SHEET

MNDP83950B-VQB REV 0B0

Original Creation Date: 10/24/94
Last Update Date: 02/24/99
Last Major Revision Date: 10/24/94

REPEATER INTERFACE CONTROLLER

General Description

The "RIC" may be used to implement an IEEE 802.3 multiport repeater unit including the functions defined by the repeater, segment partition, and jabber lockup protection state machines.

The RIC has an on-chip phase-locked-loop (PLL) for Manchester data decoding, a Manchester encoder, and an Elasticity Buffer for preamble regeneration.

Each RIC can connect to 13 cable segments via its network interface ports. One port is fully AUI compatible and is able to connect to an external MAU using the maximum lenght of AUI cable. The other 12 ports have integrated 10BASE-T transceivers. These transceiver functions may be bypassed so that the RIC may be used with external transceivers. In addition, large repeater units, containing several hundred ports may be constructed by cascading RICs together over an Inter-RIC bus.

The RIC is configurable for specific applications. It provides port status information for LED array displays and a simple interface for system processors. The RIC posseses multi-function counter and status flag arrays to facilitate network statistics gathering. A serial interface, known as the Management Interface is available for the collection of data in Managed Hub applications.

Industry Part Number

DP83950BVQB

NS Part Numbers

DP83950BVQB-MPC

Prime Die

DP63950

Processing

(blank)

Quality Conformance Inspection

(blank)

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+85
3	Static tests at	-40
4	Dynamic tests at	+25
5	Dynamic tests at	+85
6	Dynamic tests at	-40
7	Functional tests at	+25
8A	Functional tests at	+85
8B	Functional tests at	-40
9	Switching tests at	+25
10	Switching tests at	+85
11	Switching tests at	-40

Features

- Compliant with the IEEE 802.3 Repeater Specification
- 13 network connections (ports) per chip
- Selectable on-chip twisted-pair transceivers
- Cascadable for large hub applications
- Compatible with AUI compliant transceivers
- On-chip Elasticity Buffer, Manchester encoder and decoder
- Separate partition state machines for each port
- Provides port status information for LED displays including: receive, collision, partition and link status
- Power-up configuration options:

  Repeater and Partition Specifications, Transceiver interface, Status Display, Processor Operations
- Simple processor interface for repeater management and port disable
- On-chip Event Counters and Event Flag Arrays
- Serial Management Interface to combine packet and repeater status information together
- CMOS process for low power dissipation
- Single 5V supply

(Absolute Maximum Ratings)

Supply Voltage(Vcc)	-0.3V to 7.0V
DC Input Voltage(Vin)	-0.3V to Vcc +0.3V
DC Output Voltage(Vout)	-0.3V to Vcc +0.3V
Storage Temperature(Tstg)	-40 C to +150 C
Power Dissipation(Pd)	2W
Lead Temperature(Tl) (Soldering, 10 seconds)	260 C

Recommended Operating Conditions

Vcc Supply Voltage	4.75V min 5.25V max

Electrical Characteristics

DC: PROCESSOR,LED,TWISTED PAIR,INTER-RIC & MGMT. INTERFACES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5V ±5%

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Voh	Minimum High Level Output Voltage	Ioh = -8mA			3.5		V	1, 2, 3
Vol	Minimum Low Level Output Voltage	Iol = 8mA				0.4	V	1, 2, 3
Vih	Minimum High Level Input Voltage				2.0		V	1, 2, 3
Vil	Maximum Low Level Input Voltage					0.8	V	1, 2, 3
Iin	Input Current	Vin = Vcc OR GND			-1.0	1.0	uA	1, 2, 3
Ioz	Maximum TRI-STATE Output Leakage Current	Vout = Vcc or GND			-10	10	uA	1, 2, 3
Icc	Average Supply Current	Vin = Vcc or GND, Vcc = 5.25V				380	mA	1, 2, 3

DC PARAMETERS: AUI

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5V ±5%

Vod	Differential Output Voltage(TX±)	78 Ohms Termination and 270 Ohms Pulldowns		PORT 1	±550	±1200	mV	1, 2, 3
Vds	Differential Squelch Threshold (RX±, CD±)		3, 5	PORT 1	-175	-300	mV	1, 2, 3

DC PARAMETERS: PSEUDO AUI

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5V ±5%

Vpod	Differential Output Voltage (TX±)	270 Ohms Termination and 1K Ohm Pulldowns	3, 5	PORTS 2-13	±450	±1200	mV	1, 2, 3
Vpds	Differential Squelch Threshold (RX±, CD±)		3, 5	PORTS 2-13	-175	-300	mV	1, 2, 3

Electrical Characteristics

DC PARAMETERS: TWISTED PAIR

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5V ±5%

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vron	Minimum Squelch Threshold	Normal Mode		PORTS 2-13	±300	±585	mV	1, 2, 3
		Reduced Mode		PORTS 2-13		±340	mV	1, 2, 3

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 5V ±5%, Cl = 50pF, Vil(TTL) = 0V, Vih(TTL) = 3V

T1	ACKI low to $\overline{\text{ACKO}}$ Low		2, 3			24	nS	9, 10, 11
T2	ACKI High to $\overline{\text{ACKO}}$ High		2, 3			21	nS	9, 10, 11
T3a	$\overline{\text{RX}}$ Active to $\overline{\text{ACKO}}$ Low		3, 4	AUI & PSEUDO AUI		66	nS	9, 10, 11
T4a	$\overline{\text{RX}}$ Inactive to $\overline{\text{ACKO}}$ High		3, 4	AUI & PSEUDO AUI		325	nS	9, 10, 11
T5a	RX Active to ACTNd Active		3, 4	AUI & PSEUDO AUI		105	nS	9, 10, 11
T6a	RX Inactive to ACTNd Inactive		3, 4	AUI & PSEUDO AUI		325	nS	9, 10, 11
T3t	RX Active to $\overline{\text{ACKO}}$ Low		4	TWISTED PAIR ONLY		240	nS	9, 10, 11
T4t	$\overline{\text{RX}}$ Inactive to $\overline{\text{ACKO}}$ High		4	TWISTED PAIR ONLY		255	nS	9, 10, 11
T5t	RX Active to ACTNd Active		4	TWISTED PAIR ONLY		270	nS	9, 10, 11
T6t	RX Inactive to ACTNd Inactive		4	TWISTED PAIR ONLY		265	nS	9, 10, 11
T15a	ACTNd Active to TX Active		3, 4, 5	AUI & PSEUDO AUI		585	nS	9, 10, 11
T15t	ACTNd Active to TX Active		4, 5	TWISTED PAIR ONLY		790	nS	9, 10, 11

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 5V ±5%, Cl = 50pF, Vil(TTL) = 0V, Vih(TTL) = 3V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
T30a	CD Active to ANYXN Active		3	AUI & PSEUDO AUI		65	nS	9, 10, 11
T31a	CD Inactive to ANYXN Inactive		3, 6, 7	AUI & PSEUDO AUI		400	nS	9, 10, 11
T32a	CD Active to COLN Active		3, 8	AUI & PSEUDO AUI		55	nS	9, 10, 11
T33a	CD Inactive to COLN Inactive		3	AUI & PSEUDO AUI		215	nS	9, 10, 11
T39	COLN Active to Start of JAM		3			400	nS	9, 10, 11
T40	COLN Inactive to End of JAM		3, 9			800	nS	9, 10, 11
T30t	Collision Active to ANYXN Active		3	TWISTED PAIR ONLY		800	nS	9, 10, 11
T31t	Collision Inactive to ANYXN Inactive		3, 6	TWISTED PAIR ONLY		400	nS	9, 10, 11
T34	ANYXN Active Time				96		Bits	9, 10, 11
T35	ANYXN Inactive to TX to all inactive				120	180	nS	9, 10, 11
T38	ANTXN Active to Start of Jam					400	nS	9, 10, 11
T36	ACTN Inactive to TX Inactive		3			415	nS	9, 10, 11
T37	ANYXN Inactive to TX "One Port Left" Inactive		3		120	180	nS	9, 10, 11
T101	IRC Output High Time		3, 10		45	55	nS	9, 10, 11
T102	IRC Output Low Time		3, 10		45	55	nS	9, 10, 11
T103	IRC Output Cycle Time		3, 10		90	110	nS	9, 10, 11
T104	ACTNd Active to PKEN Active		3, 10		555		nS	9, 10, 11

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 5V ±5%, Cl = 50pF, Vil(TTL) = 0V, Vih(TTL) = 3V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
T105	ACTNd Active to IRE Active		3, 10		560		nS	9, 10, 11
T106	IRE Output Active to IRC Active		3, 10			1.8	uS	9, 10, 11
T107	IRD Output Valid from IRC		3, 10			10	nS	9, 10, 11
T108	IRD Output Stable Valid Time		3, 10		75		nS	9, 10, 11
T109	IRC Output High to IRE Inactive		3, 10		30	70	nS	9, 10, 11
T110	Number of IRCs after IRE Inactive		3, 10		5		Clks	9, 10, 11
T111	IRC Input High Time		3		20		nS	9, 10, 11
T112	IRC Input Low Time		3		20		nS	9, 10, 11
T114	IRD Input Setup to IRC		3		5		nS	9, 10, 11
T115	IRD Input Hold from IRC		3		10		nS	9, 10, 11
T116	IRC Input High to IRE Inactive		3		10	90	nS	9, 10, 11
T50	MRXC High Time		3, 11		45	55	nS	9, 10, 11
T51	MRXC Low Time		3, 11		45	55	nS	9, 10, 11
T52	MRXC Cycle Time		3, 11		90	110	nS	9, 10, 11
T53	ACTNd Active to MEN Active		3, 11			725	nS	9, 10, 11
T54	ACTNd Active to MCRS Active		3, 11			730	nS	9, 10, 11
T55	MRXD Setup		3, 11		35		nS	9, 10, 11
T56	MRXD Hold		3, 11		40		nS	9, 10, 11
T57	MRXC Low to MCRS Inactive		3, 11		-5	6	nS	9, 10, 11
T58	MCRS Inactive to MEN Low		3, 11			510	nS	9, 10, 11

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 5V ±5%, Cl = 50pF, Vil(TTL) = 0V, Vih(TTL) = 3V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
T59	Min Number of MRXCs after MCRS Inactive		3, 11		5	5	Clks	9, 10, 11
T60	PCOMP Pulse Width		3, 11		20		nS	9, 10, 11
T61	Data Setup				10		nS	9, 10, 11
T62	Data Hold				10		nS	9, 10, 11
T63	MLOAD Active to BUFEN Active					35	nS	9, 10, 11
T64	MLOAD Inactive to BUFEN Inactive					35	nS	9, 10, 11
T65	MLOAD Width				800		nS	9, 10, 11
T66	Strobe Address Setup				80	115	nS	9, 10, 11
T67	Strobe Data Setup				35	65	nS	9, 10, 11
T68	Strobe Data Hold				135	165	nS	9, 10, 11
T69	Strobe Width				30	65	nS	9, 10, 11
T70	CDEC Pulse Width				20	100	nS	9, 10, 11
T71	CDEC to CDEC Width				200		nS	9, 10, 11
T80	Read Address Setup		12		0		nS	9, 10, 11
T81	Read Address Hold		12		0		nS	9, 10, 11
T82	Read Active to $\overline{\text{BUFEN}}$ Active		12		95	345	nS	9, 10, 11
T83	Read Inactive to $\overline{\text{BUFEN}}$ Inactive		12			35	nS	9, 10, 11
T84	Read Active to Data Invalid		12		245		nS	9, 10, 11
T85	Read Data Hold		12		75		nS	9, 10, 11
T86	Read Active to $\overline{\text{RDY}}$ Active		12		340	585	nS	9, 10, 11

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 5V ±5%, Cl = 50pF, Vil(TTL) = 0V, Vih(TTL) = 3V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
T87	Read Inactive to $\overline{\text{RDY}}$ Inactive		12			30	nS	9, 10, 11
T88	Read Width		12		600		nS	9, 10, 11
T90	Write Address Setup		12, 13, 14, 15		0		nS	9, 10, 11
T91	Write Address Hold		12, 13, 14, 15		0		nS	9, 10, 11
T92	Write Active to $\overline{\text{BUFEN}}$ Active		12, 13, 14, 15		95	355	nS	9, 10, 11
T93	Write Inactive to $\overline{\text{BUFEN}}$ Inactive		12, 13, 14, 15			35	nS	9, 10, 11
T94	Write Active to Data Valid		12, 13, 14, 15			275	nS	9, 10, 11
T95	Write Data Hold		12, 13, 14, 15		0		nS	9, 10, 11
T96	Write Active to $\overline{\text{RDY}}$ Active		12, 13, 14, 15		340	585	nS	9, 10, 11
T97	Write Inactive to $\overline{\text{RDY}}$ Inactive		12, 13, 14, 15			30	nS	9, 10, 11
T98	Write Width		12, 13, 14, 15		600		nS	9, 10, 11
T99	Write Active to Data TRI-STATE		12, 13, 14, 15			350	nS	9, 10, 11

Note 1: The operation in Reduced Mode is not guaranteed below 300 mV.
Note 2: Timing Valid with no receive or collision activities
Note 3: The Inter-RIC and Management Busses use active high signals, active low signals may also be used.
Note 4: $\overline{\text{ACKI}}$ assumed high

(Continued)

Note 5: ACTNd and ACTNs are tied together
Note 6: TX collision extension has already been performed and no other port is driving ANYXN.

Note 7: Includes TW2
Note 8: PKEN assumed high
Note 9: Assuming reception ended before COLN goes inactive. TW2 is included in this parameter. Assuming ACTNd to ACTNs delay is 0.
Note 10: In a Multi-RIC system, the PKEN signal is valid only for the first receiving RIC.
Note 11: The preamble on this bus consists of the following string: 01011
Note 12: Minimum high time between read/write cycles is 100nS.
Note 13: Assuming zero propagation delay on external buffer.
Note 14: The data will always TRI-STATE before $\overline{\text{BUFEN}}$ goes active with a load of 100pF on the data bus.
Note 15: When $\overline{\text{RDY}}$ is used, the minimum 600nS write width does not have to be maintained.

Burn-in/QCI Electrical End-Point Tests

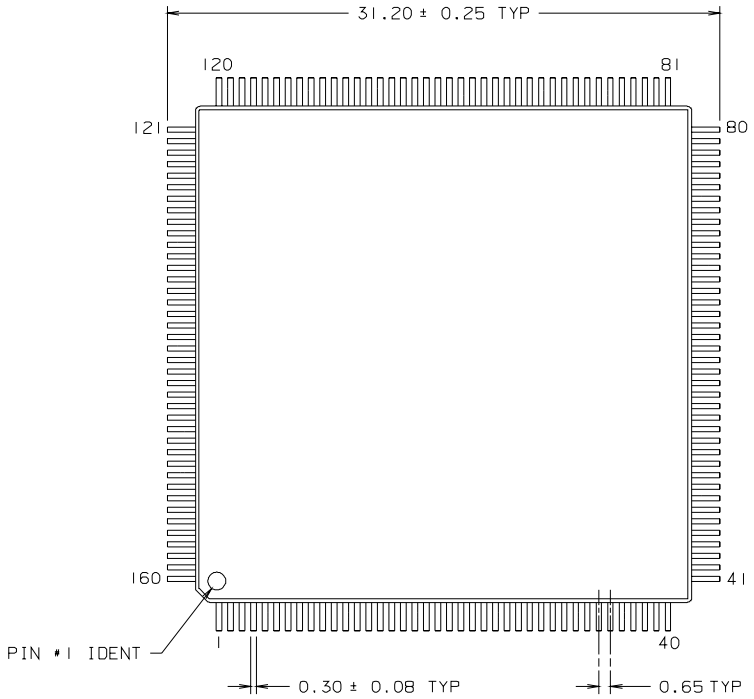
OP#	Operation description	Sub-Groups
01	Post Burn-In PDA 10%	1,7,9
02	Final Electrical	1,2,3,7,8A,8B,9,10,11
03	Group A	1,2,3,7,8A,8B,9,10,11
04	Subgroup B-4 (For Initial Qual ONLY)	1,7,9
05	Subgroup C-1 (For Initial Qual ONLY)	1,2,3,7,8A,8B,9,10,11
06	Subgroup C-2 (For Initial Qual ONLY)	1,7,9
07	Subgroup D-2 (For Initial Qual ONLY)	1,7,9
08	Subgroup D-3 (For Initial Qual ONLY)	1,2,7,8A,9,10
09	Subgroup D-4 (For Initial Qual ONLY)	1,2,7,8A,9,10

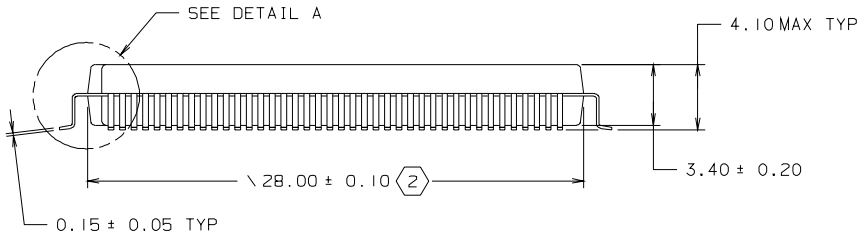
Graphics and Diagrams

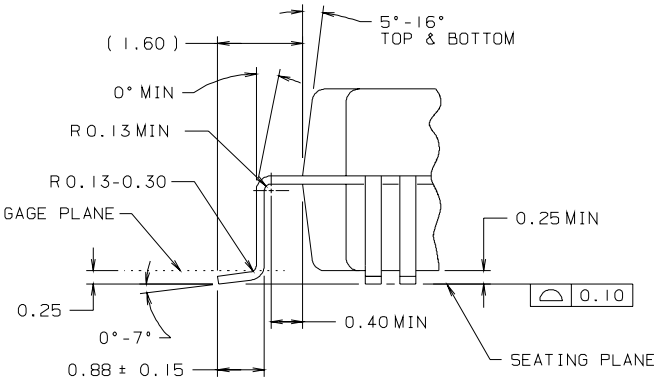
GRAPHICS#	DESCRIPTION
VUL160ARB	PQFP, JEDEC METRIC, 28x28x3.4MM, 160LD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	09264	08/06/92	TL/HJK
B	REVISE NOTE 3 & DETAIL A	09959	09/09/93	TL/







DETAIL A
TYPICAL

NOTES: UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH:
   5.08 MICROMETERS MINIMUM SOLDER PLATING (85/15)THICKNESS ON COPPER.

(2) DIMENSION DOES NOT INCLUDE MOLD PROTRUSION.
MAXIMUM ALLOWABLE MOLD PROTRUSION 0.25mm PER SIDE.

3. REFERENCE JEDEC REGISTRATION MO-108, VARIATION DD-1, DATED 10/90; NSSG, ASAT DWG# DG 2004 REV 1, DATED 10/19/92, SEIKO EPSON DWG# QFP8-160 PIN E1 DATED 11/27/89.

DIMENSIONS ARE IN MILLIMETERS

APPROVALS	DATE
DRAWN T. LEQUANG	08/06/92
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

PQFP, JEDEC METRIC, 28 X 28 X 3.4 mm, 160 LEAD

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-VUL160A	B

DO NOT SCALE DRAWING | SHEET 1 OF 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0B0	M0003282	02/24/99	Rose Malone	Update MDS: MNDP83950B-VQB, Rev. 0A0 to MNDP83950B-VQB, Rev. 0B0.