

Preliminary

TOSHIBA Photocoupler GaAlAs IRED + Photo IC

TLP350

Inverter for Air Conditioner

IGBT/Power MOS FET Gate Drive

Industrial Inverter

The TOSHIBA TLP350 consists of a GaAlAs light emitting diode and a integrated photodetector.

This unit is 8-lead DIP package.

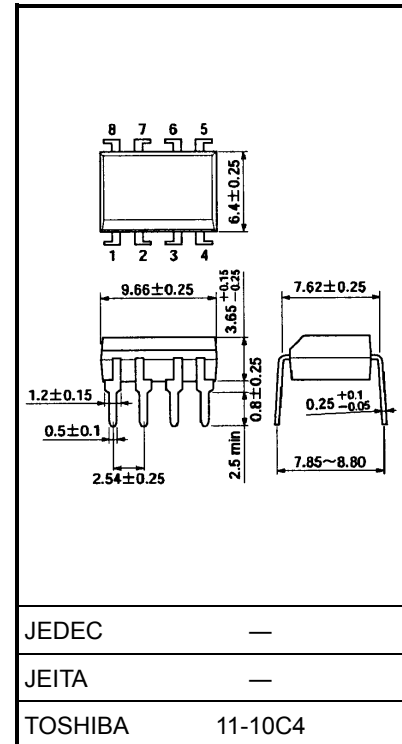
TLP350 is suitable for gate driving circuit of IGBT or power MOS FET..

- Peak output current: $I_O = \pm 2.0$ A (max)
- Guaranteed performance over temperature: -40 to 100°C
- Supply current: $I_{CC} = 2$ mA (max)
- Power supply voltage: $V_{CC} = 15$ to 30 V
- Threshold input current : $I_{FLH} = 5$ mA (max)
- Switching time (t_{pLH}/t_{pHL}) : 500 ns (max)
- Common mode transient immunity: 15 kV/ μs
- Isolation voltage: 3750 Vrms

Truth Table

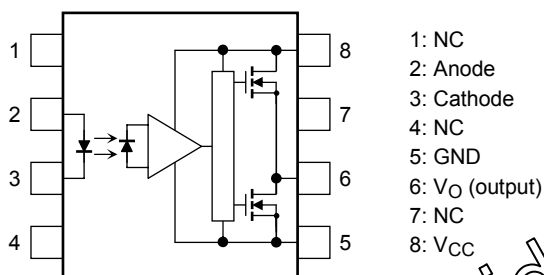
Input	LED	Tr1	Tr2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

Unit: mm

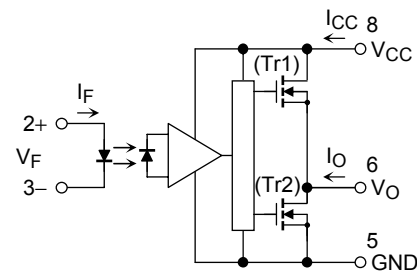


Weight: 0.54 g (typ.)

Pin Configuration (top view)



Schematic



A 0.1 μF bypass capacitor must be connected between pin 8 and 5. (See Note 6)

Development idea
Not fixed yet

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
LED	Forward current	I_F	20	mA
	Forward current derating (Ta ≥ 85°C)	$\Delta I_F / \Delta T_a$	-0.54	mA/°C
	Peak transient forward current (Note 1)	I_{FP}	1	A
	Reverse voltage	V_R	5	V
	Junction temperature	T_j	125	°C
Detector	"H" peak output current (Note 2)	I_{OPH}	-2.0	A
	"L" peak output current (Note 2)	I_{OPL}	2.0	A
	Output voltage (Note 3)	V_O	35	V
	Supply voltage (Note 3)	V_{CC}	35	V
	Junction temperature	T_j	125	°C
Operating frequency (Note 4)		f		kHz
Storage temperature range		T_{stg}	-55 to 125	°C
Operating temperature range		T_{opr}	-40 to 100	°C
Lead soldering temperature (10 s) (Note 5)		T_{sol}	260	°C
Isolation voltage (AC, 1 minute, R.H. ≤ 60%) (Note 6)		BV_S	3750	Vrms

Note 1: Pulse width $P_W \leq 1 \mu s$, 300 pps

Note 2: Exponential waveform pulse width $P_W \leq \mu s$, $f \leq$ kHz

Note 3: $T_a \leq 100^\circ C$

Note 4: Exponential waveform $I_{OPH} \leq$ A ($\leq \mu s$), $I_{OPL} \leq +$ A ($\leq \mu s$), $T_a =$ °C

Note 5: It is 2 mm or more from a lead root.

Note 6: Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Note 7: A ceramic capacitor(0.1 μF) should be connected from pin 8 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property.
The total lead length between capacitor and coupler should not exceed 1 cm.

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Input current, ON (Note 8)	$I_F (ON)$	7.5	—	10	mA
Input voltage, OFF	$V_F (OFF)$	0	—	0.8	V
Supply voltage	V_{CC}	15	—	30	V
Peak output current	I_{OPH}/I_{OPL}	—	—	± 1.0	A
Operating temperature	T_{opr}	-40	—	100	°C

Note 8: Input signal rise time (fall time) < 0.5 μs .

Electrical Characteristics (Ta = -40 to 100°C, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.*	Max	Unit
Forward voltage		V_F	—	$I_F = 5 \text{ mA}$, $T_a = 25^\circ\text{C}$		—	1.55	1.70	V
Temperature coefficient of forward voltage		$\Delta V_F / \Delta T_a$	—	$I_F = 5 \text{ mA}$		—	-2.0	—	mV/°C
Input reverse current		I_R	—	$V_R = 5 \text{ V}$, $T_a = 25^\circ\text{C}$		—	—	10	μA
Input capacitance		C_T	—	$V = 0$, $f = 1 \text{ MHz}$, $T_a = 25^\circ\text{C}$		—	45	—	pF
Output current (Note 9)	“H” Level	I_{OPH1}	1	$V_{CC} = 30 \text{ V}$ $I_F = 5 \text{ mA}$	$V_{8-6} = 4.0 \text{ V}$	-1.0	-1.5	—	A
		I_{OPH2}			$V_{8-6} =$			—	
	“L” Level	I_{OPL1}	2	$V_{CC} = 30 \text{ V}$ $I_F = 0 \text{ mA}$	$V_{6-5} = 2.0 \text{ V}$	1.0	2.0	—	
		I_{OPL2}			$V_{6-5} =$			—	
Output voltage	“H” Level	V_{OH}	3	$V_{CC} 1 = +15 \text{ V}$	$I_O = -100 \text{ mA}$, $I_F = 5 \text{ mA}$	11		—	V
	“L” Level	V_{OL}	4	$V_{EE} 1 = -15 \text{ V}$	$I_O = 100 \text{ mA}$, $V_F = 0.8 \text{ V}$	—		1.0	
Supply current	“H” Level	I_{CCH}	5	$V_{CC} = 30 \text{ V}$ V_O open	$I_F = 10 \text{ mA}$	—		2.0	mA
	“L” Level	I_{CCL}	6		$I_F = 0 \text{ mA}$	—		2.0	
Threshold input current	L → H	I_{FLH}	—	$V_{CC} 1 = +15 \text{ V}$ $V_{EE} 1 = -15 \text{ V}$, $V_O > 0 \text{ V}$		—		5	mA
Threshold input voltage	H → L	V_{FHL}	—	$V_{CC} 1 = +15 \text{ V}$ $V_{EE} 1 = -15 \text{ V}$, $V_O < 0 \text{ V}$		0.8	—	—	V
Supply voltage		V_{CC}	—	—		15	—	30	V
UVLO thresh hold		V_{UVLO+}	—	$V_O > 2.5 \text{ V}$, $I_F = 5 \text{ mA}$, $I_O = 100 \text{ mA}$		11.0	—	13.5	V
		V_{UVLO-}	—			9.5	—	12.0	V

*: All typical values are at $T_a = 25^\circ\text{C}$

Note 9: Duration of I_O time $\leq 50 \mu\text{s}$

Note 10: This product is more sensitive than the conventional product to static electricity (ESD) because of a lowest power consumption design.

General precaution to static electricity (ESD) is necessary for handling this component.

Isolation Characteristics (Ta = 25°C)

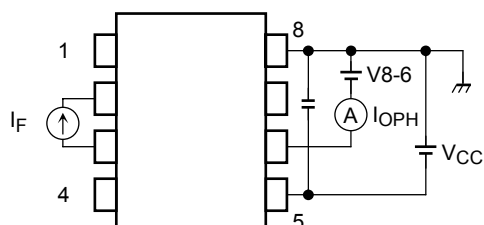
Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Capacitance input to output	C_S	$V = 0$, $f = 1 \text{ MHz}$ (Note6)	—	0.8	—	pF
Isolation resistance	R_S	$V_S = 500 \text{ V}$, $T_a = 25^\circ\text{C}$, $R.H. \leq 60\%$ (Note6)	1×10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S	AC, 1 minute	3750	—	—	V_{rms}
		AC, 1 second, in oil	—	10000	—	
		DC, 1 minute, in oil	—	10000	—	Vdc

Switching Characteristics (Ta = -40 to 100°C, unless otherwise specified)

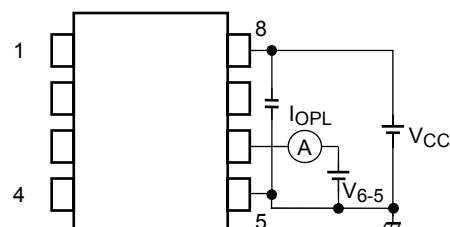
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.*	Max	Unit
Propagation delay time	L → H	7	$V_{CC1} = +15\text{ V}$ $V_{EE1} = -15\text{ V}$ $R_g = 20\ \Omega$ $C_g = 10\text{ nF}$	50	250	500	ns
	H → L						
Propagation delay difference between any two parts or channels	PDD $ t_{pHL} - t_{pLH} $	7	$V_{CC1} = +15\text{ V}$, $V_{EE1} = -15\text{ V}$, $R_g = 20\ \Omega$, $C_g = 10\text{ nF}$	—	—	450	ns
Output rise time (10-90%)	t_r	8	$V_{CC1} = +15\text{ V}$ $V_{EE1} = -15\text{ V}$ $R_g = 20\ \Omega$ $C_g = 10\text{ nF}$	—	—	—	ns
Output fall time (90-10%)	t_f						
Common mode transient immunity at high level output	CM_H	8	$V_{CM} = 1000\text{ V}_{p-p}$ $T_a = 25^\circ\text{C}$ $V_{CC} = 30\text{ V}$	$I_F = 5\text{ mA}$ $V_O(\text{min}) = 26\text{ V}$	—	—	V/ μs
Common mode transient immunity at low level output	CM_L			$I_F = 0\text{ mA}$ $V_O(\text{max}) = 1\text{ V}$	—	—	

*: All typical values are at Ta = 25°C

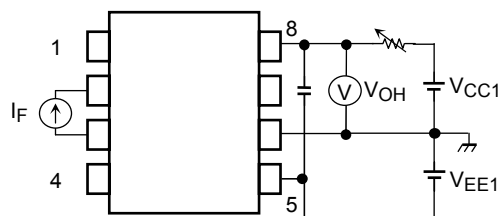
Test Circuit 1: I_{OPH}



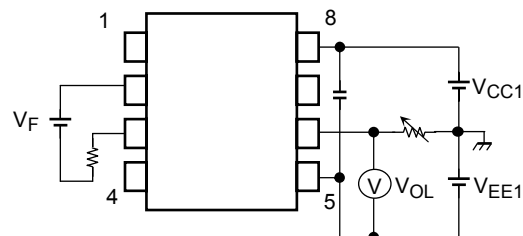
Test Circuit 2: I_{OPL}



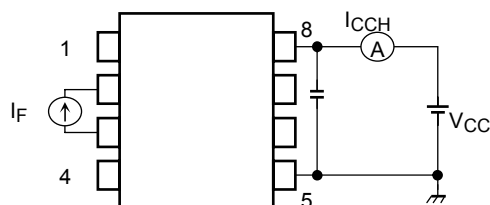
Test Circuit 3: V_{OH}



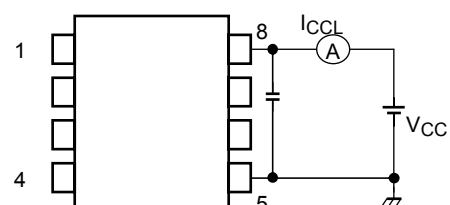
Test Circuit 4: V_{OL}



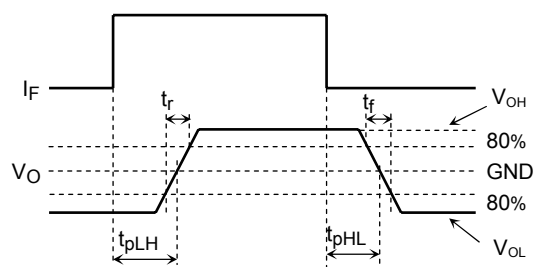
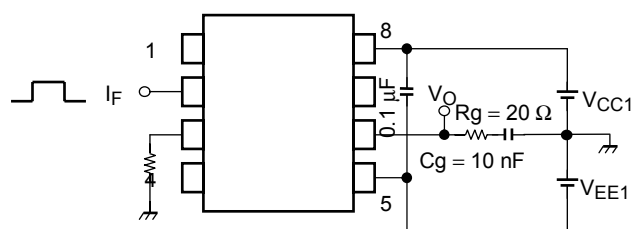
Test Circuit 5: I_{CCH}



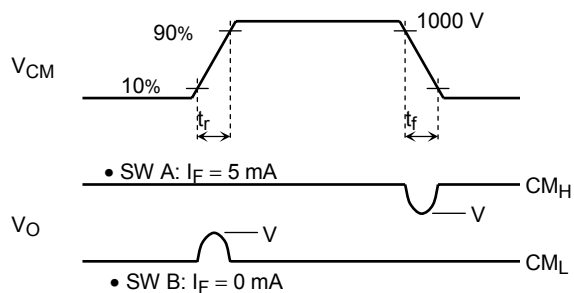
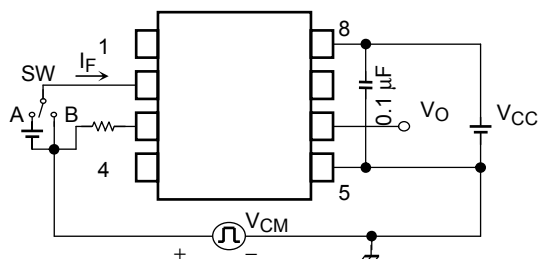
Test Circuit 6: I_{CCL}



Test Circuit 7: t_{pLH} , t_{pHL} , t_r , t_f , PDD



Test Circuit 8: CM_H , CM_L



$$CM_L = \frac{800 \text{ V}}{t_f (\mu\text{s})}$$

$$CM_H = \frac{800 \text{ V}}{t_r (\mu\text{s})}$$

CM_L (CM_H) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the low (high) state.

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