April 1998

National Semiconductor

LF147/LF347
Wide Bandwidth Quad JFET Input Operational Amplifiers

General Description

The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

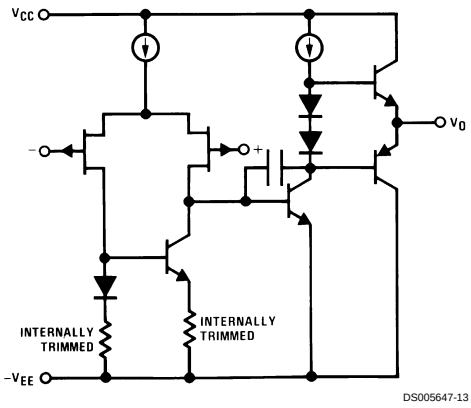
The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

- Internally trimmed offset voltage: 5 mV max
- Low input bias current: 50 pA
- Low input noise current: 0.01 pA/$\sqrt{\text{Hz}}$
- Wide gain bandwidth: 4 MHz
- High slew rate: 13 V/µs
- Low supply current: 7.2 mA
- High input impedance: $10^{12}\Omega$
- Low total harmonic distortion A_V=10,: <0.02%
  R_L=10k, V_O=20 Vp-p, BW=20 Hz−20 kHz
- Low 1/f noise corner: 50 Hz
- Fast settling time to 0.01%: 2 µs

Simplified Schematic

¼ Quad



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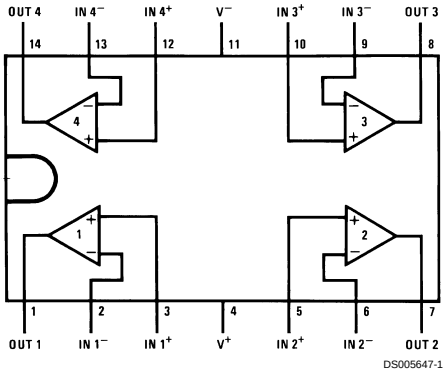
Connection Diagram

Dual-In-Line Package



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Note 1: Available per SMD #8102306, JM38510/11906.

Top View
Order Number LF147J, LF347M, LF347BN, LF347N, LF147D/883 or LF147J/883 (Note 1)
See NS Package Number D14E, J14A, M14A or N14A

BI-FET II™ is a trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LF147	LF347B/LF347
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 3)	±19V	±15V
Output Short Circuit Duration (Note 4)	Continuous	Continuous
Power Dissipation (Notes 5, 11)	900 mW	1000 mW
T_j max	150˚C	150˚C
θ_{jA}		
Cavity DIP (D) Package		80˚C/W
Ceramic DIP (J) Package		70˚C/W
Plastic DIP (N) Package		75˚C/W
Surface Mount Narrow (M)		100˚C/W
Surface Mount Wide (WM)		85˚C/W
Operating Temperature Range	(Note 6)	(Note 6)
Storage Temperature Range	$-65˚C \le T_A \le 150˚C$	
Lead Temperature (Soldering, 10 sec.)	260˚C	260˚C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)		260˚C
Small Outline Package		
Vapor Phase (60 seconds)		215˚C
Infrared (15 seconds)		220˚C

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

ESD Tolerance (Note 12) 900V

DC Electrical Characteristics (Note 7)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10 kΩ, T_A=25˚C		1	5		3	5		5	10	mV
		Over Temperature			8			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ		10			10			10		µV/˚C
I_{OS}	Input Offset Current	T_j=25˚C, (Notes 7, 8)		25	100		25	100		25	100	pA
		Over Temperature			25			4			4	nA
I_B	Input Bias Current	T_j=25˚C, (Notes 7, 8)		50	200		50	200		50	200	pA
		Over Temperature			50			8			8	nA
R_{IN}	Input Resistance	T_j=25˚C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25˚C	50	100		50	100		25	100		V/mV
		V_O=±10V, R_L=2 kΩ										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S=±15V	±11	+15		±11	+15		±11	+15		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio	R_S≤10 kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 9)	80	100		80	100		70	100		dB
I_S	Supply Current			7.2	11		7.2	11		7.2	11	mA

AC Electrical Characteristics (Note 7)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A=25˚C, f=1 Hz−20 kHz (Input Referred)		−120			−120			−120		dB
SR	Slew Rate	V_S=±15V, T_A=25˚C	8	13		8	13		8	13		V/µs
GBW	Gain-Bandwidth Product	V_S=±15V, T_A=25˚C	2.2	4		2.2	4		2.2	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25˚C, R_S=100Ω, f=1000 Hz		20			20			20		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j=25˚C, f=1000 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 3: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 4: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 5: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 6: The LF147 is available in the military temperature range −55˚C≤T_A≤125˚C, while the LF347B and the LF347 are available in the commercial temperature range 0˚C≤T_A≤70˚C. Junction temperature can rise to T_j max = 150˚C.

Note 7: Unless otherwise specified the specifications apply over the full temperature range and for V_S=±20V for the LF147 and for V_S=±15V for the LF347B/LF347. V_{OS}, I_B, and I_{OS} are measured at V_{CM}=0.

Note 8: The input bias currents are junction leakage currents which approximately double for every 10˚C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. T_j=T_A+θ_{jA} P_D where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 9: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from V_S = ± 5V to ±15V for the LF347 and LF347B and from V_S = ±20V to ±5V for the LF147.

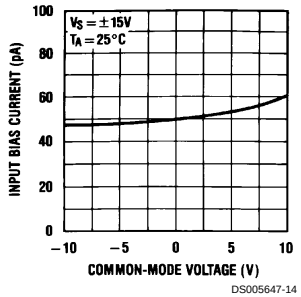
Note 10: Refer to RETS147X for LF147D and LF147J military specifications.

Note 11: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Note 12: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

Input Bias Current



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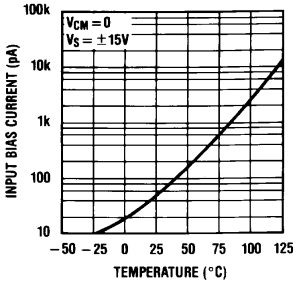
Input Bias Current



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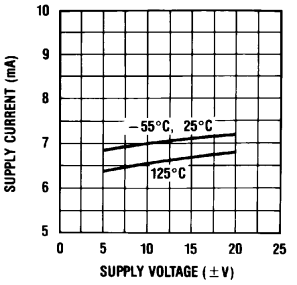
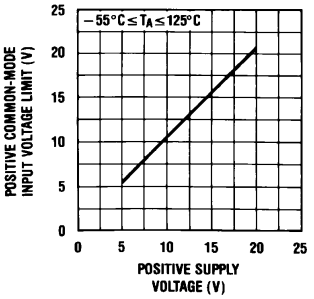
Supply Current



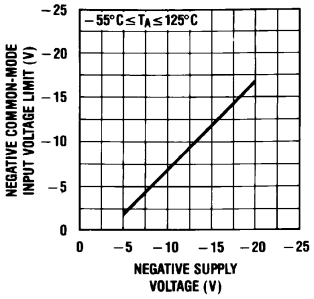
DS005647-16

Positive Common-Mode Input Voltage Limit



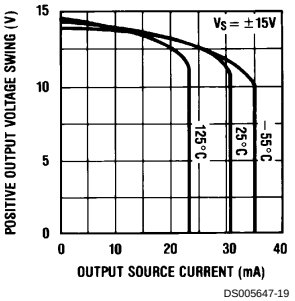
DS005647-17

Negative Common-Mode Input Voltage Limit



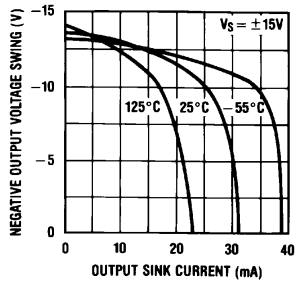
DS005647-18

Positive Current Limit



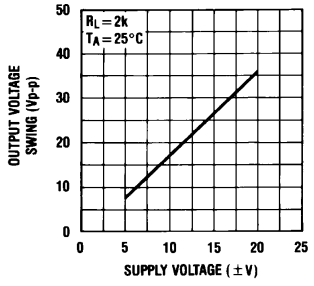
DS005647-19

Negative Current Limit



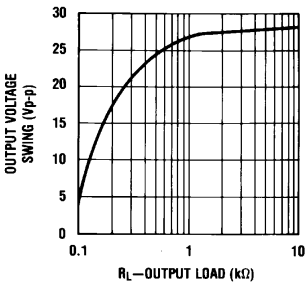
DS005647-20

Output Voltage Swing



DS005647-21

Output Voltage Swing



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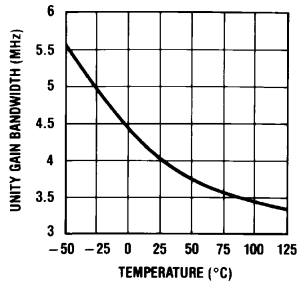
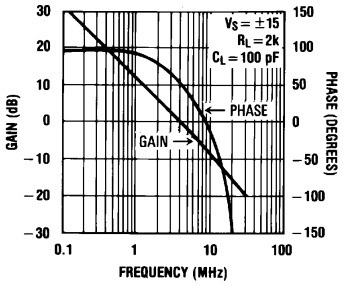
Typical Performance Characteristics (Continued)

Gain Bandwidth



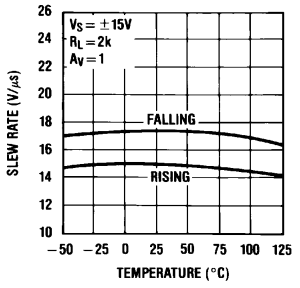
DS005647-23

Bode Plot



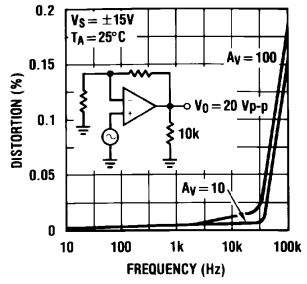
DS005647-24

Slew Rate



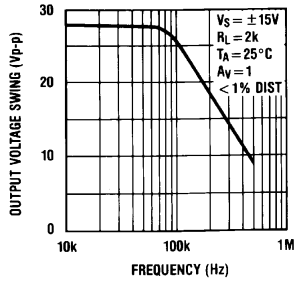
DS005647-25

Distortion vs Frequency



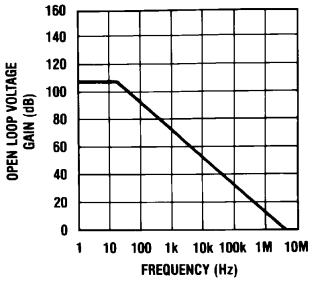
DS005647-26

Undistorted Output Voltage Swing



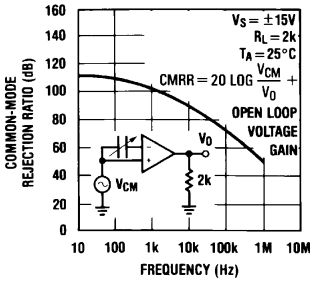
DS005647-27

Open Loop Frequency Response



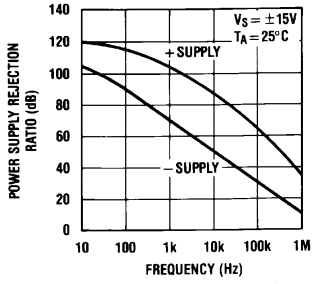
DS005647-28

Common-Mode Rejection Ratio



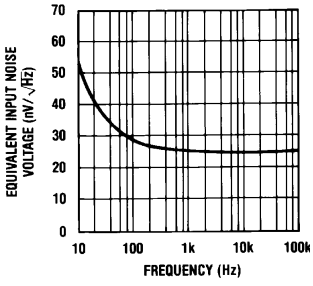
DS005647-29

Power Supply Rejection Ratio



DS005647-30

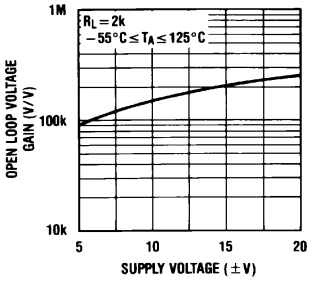
Equivalent Input Noise Voltage



DS005647-31

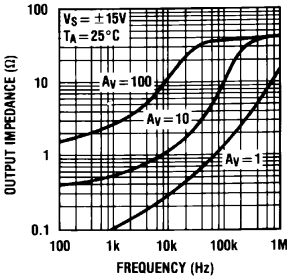
Typical Performance Characteristics (Continued)

Open Loop Voltage Gain



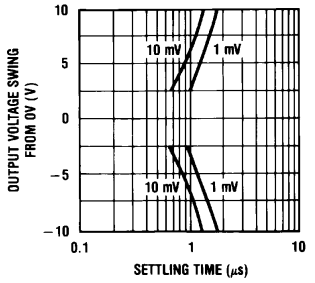
DS005647-32

Output Impedance



DS005647-33

Inverter Settling Time



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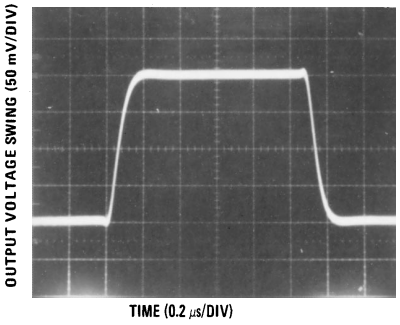
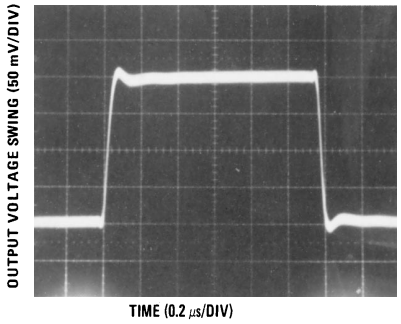
Pulse Response R_L=2 kΩ, C_L=10 pF

Small Signal Inverting



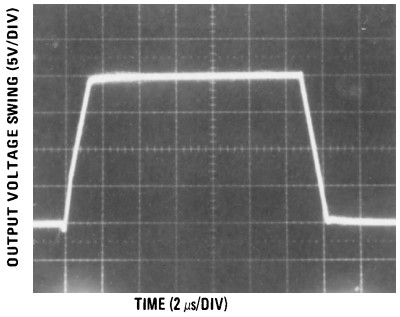
DS005647-4

Small Signal Non-Inverting



DS005647-5

Large Signal Inverting



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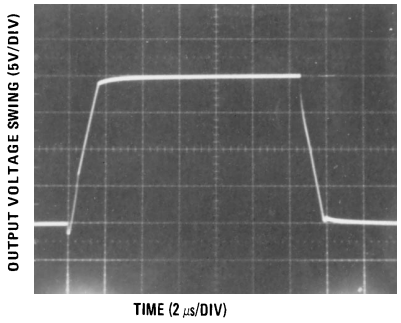
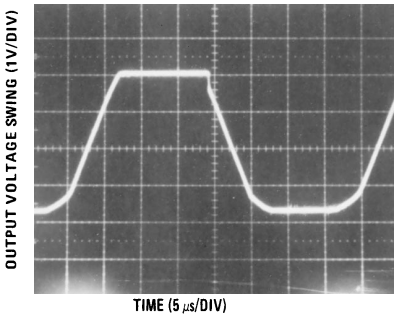
Large Signal Non-Inverting



DS005647-7

Current Limit (R_L=100Ω)



DS005647-8

Application Hints

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Application Hints (Continued)

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

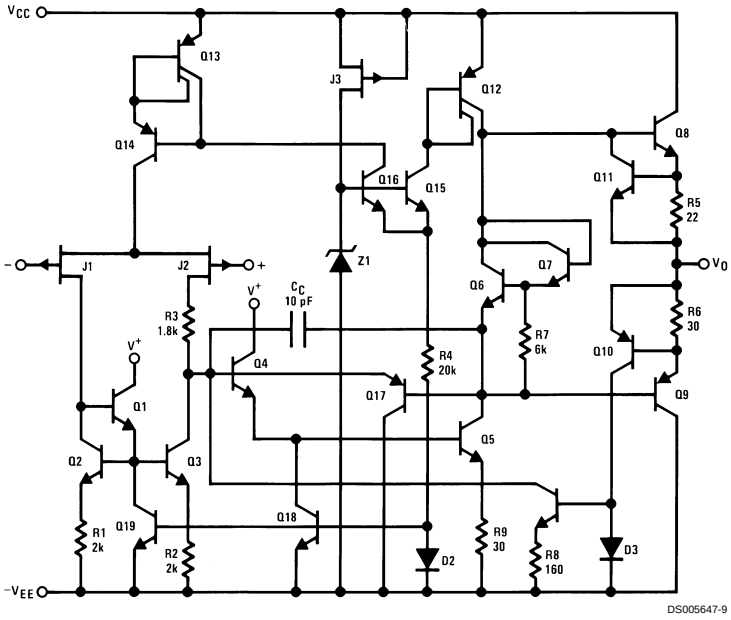
The LF147 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

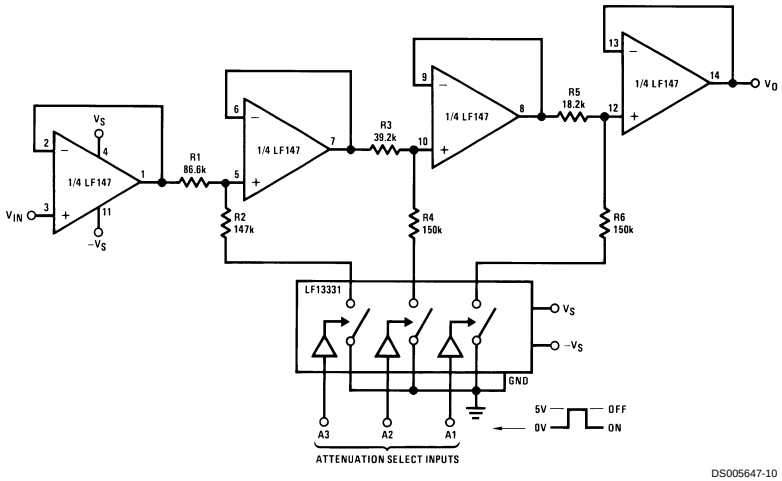
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



Typical Applications

Digitally Selectable Precision Attenuator



DS005647-10

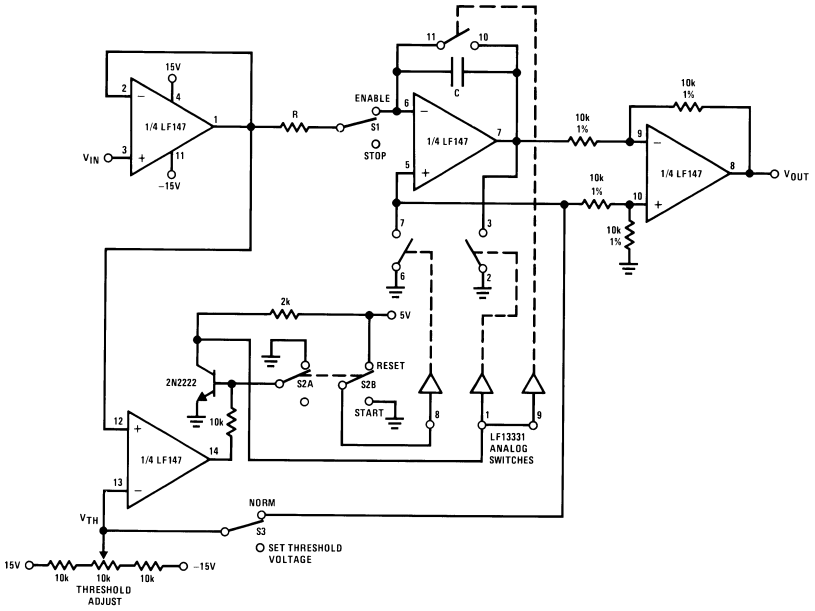
All resistors 1% tolerance

- Accuracy of better than 0.4% with standard 1% value resistors
- No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

A1	A2	A3	V_O Attenuation
0	0	0	0
0	0	1	−1 dB
0	1	0	−2 dB
0	1	1	−3 dB
1	0	0	−4 dB
1	0	1	−5 dB
1	1	0	−6 dB
1	1	1	−7 dB

Typical Applications (Continued)

Long Time Integrator with Reset, Hold and Starting Threshold Adjustment



DS005647-11

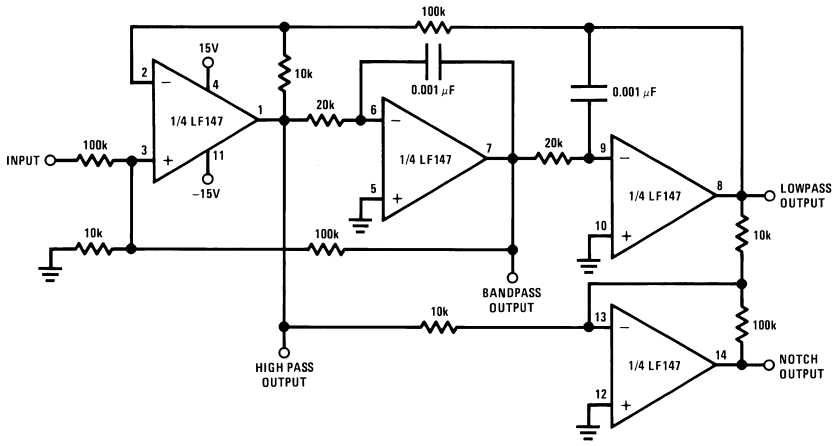
- V_{OUT} starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:

$$V_{OUT} = \frac{1}{RC}\int_0^t (V_{IN} - V_{TH})dt$$

- Output starts when $V_{IN} \geq V_{TH}$
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

Typical Applications (Continued)

Universal State Variable Filter

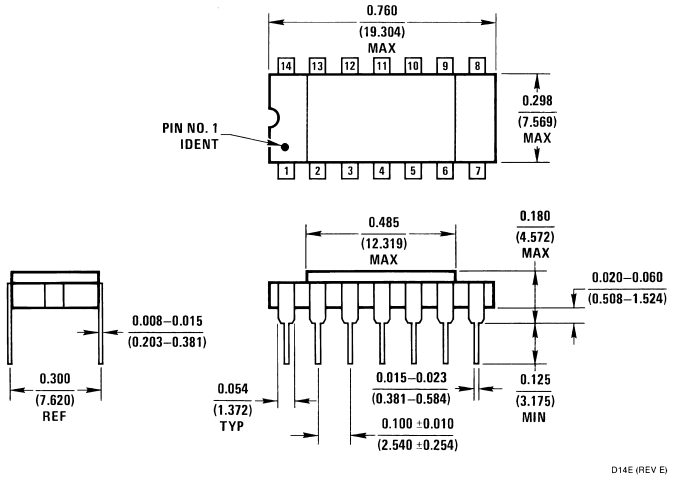


DS005647-12

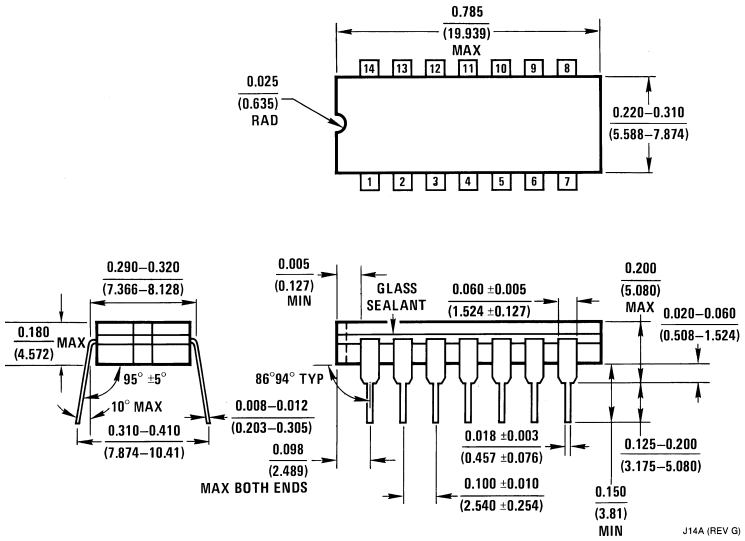
For circuit shown:
f_0=3 kHz, f_{NOTCH}=9.5 kHz
Q=3.4
Passband gain:
Highpass — 0.1
Bandpass — 1
Lowpass — 1
Notch — 10

- f_0xQ≤200 kHz
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM148 data sheet for design equations

Physical Dimensions inches (millimeters) unless otherwise noted

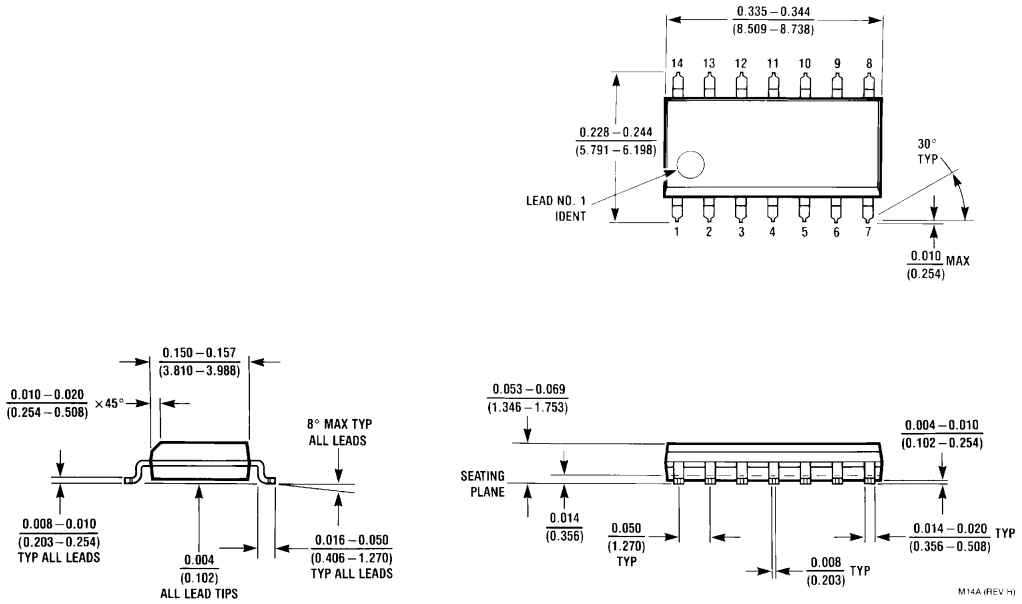


Hermetic Dual-In-Line Package (D)
Order Number LF147D/883
NS Package Number D14E

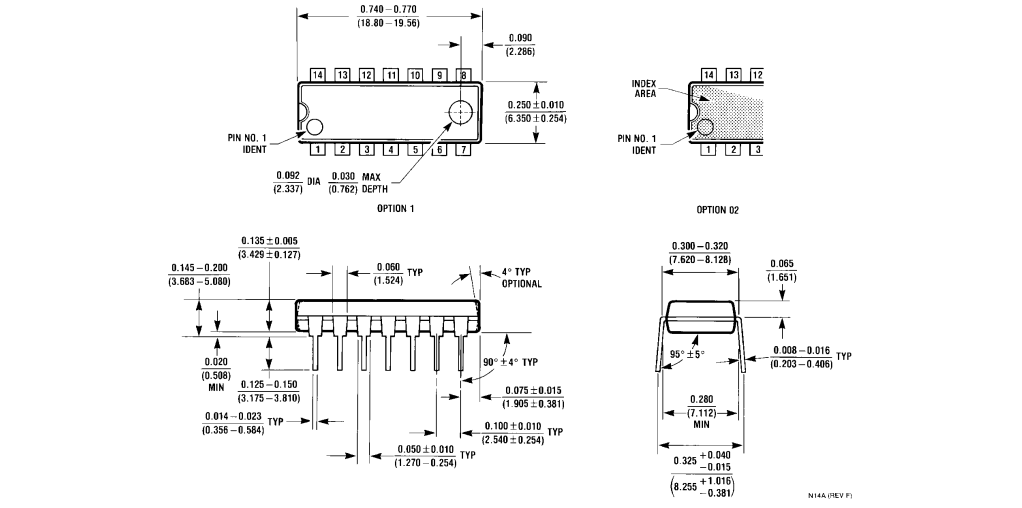


Ceramic Dual-In-Line Package (J)
Order Number LF147J or LF147J/883
NS Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



S.O. Package (M)
Order Number LF347M
NS Package Number M14A



Molded Dual-In-Line Package (N)
Order Number LF347BN or LF347N
NS Package Number N14A

Notes

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507