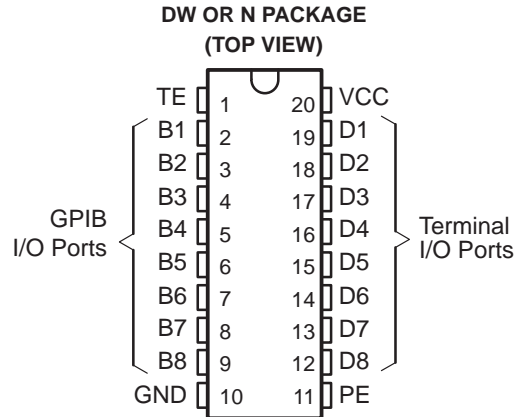


- Meets IEEE Standard 488-1978 (GPIB)
- 8-Channel Bidirectional Transceiver
- Power-Up/Power-Down Protection (Glitch Free)
- High-Speed, Low-Power Schottky Circuitry
- Low Power Dissipation . . . 72 mW Max Per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance pnp Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device Is Powered Down ($V_{CC} = 0$)



description

The SN75160B 8-channel general-purpose interface bus (GPIB) transceiver is a monolithic, high-speed, low-power Schottky device designed for two-way data communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the passive-pullup or 3-state mode. If talk enable (TE) is high, these ports have the characteristics of passive-pullup outputs when pullup enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 mA of sink current.

Output glitches during power up and power down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when $V_{CC} = 0$. When combined with the SN75161B or SN75162B management bus transceivers, the pair provides the complete 16-wire interface for the IEEE-488 bus.

The SN75160B is characterized for operation from 0°C to 70°C.

Function Tables

| EACH DRIVER | | | |
|-------------|----|----|-------------|
| INPUTS | | | OUTPUT B |
| D | TE | PE | |
| H | H | H | H |
| L | H | X | L |
| H | X | L | Z† |
| X | L | X | Z† |

| EACH RECEIVER | | | |
|---------------|----|----|-------------|
| INPUTS | | | OUTPUT D |
| B | TE | PE | |
| L | L | X | L |
| H | L | X | H |
| X | H | X | Z |

H = high level, L = low level, X = irrelevant, Z = high impedance

† This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and GND.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

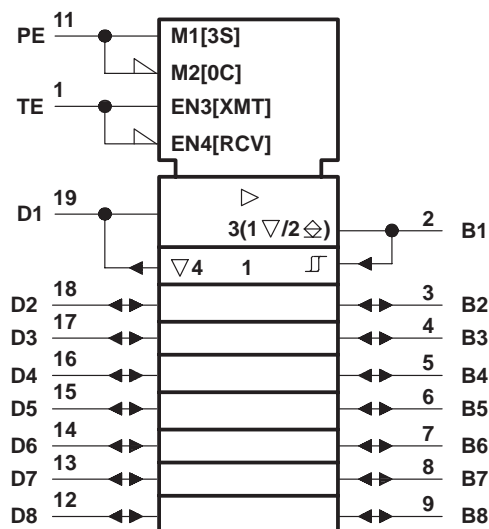
 **TEXAS
INSTRUMENTS**

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SN75160B
OCTAL GENERAL-PURPOSE
INTERFACE BUS TRANSCEIVER
 SLLS004B – OCTOBER 1985 – REVISED MAY 1995

logic symbol†

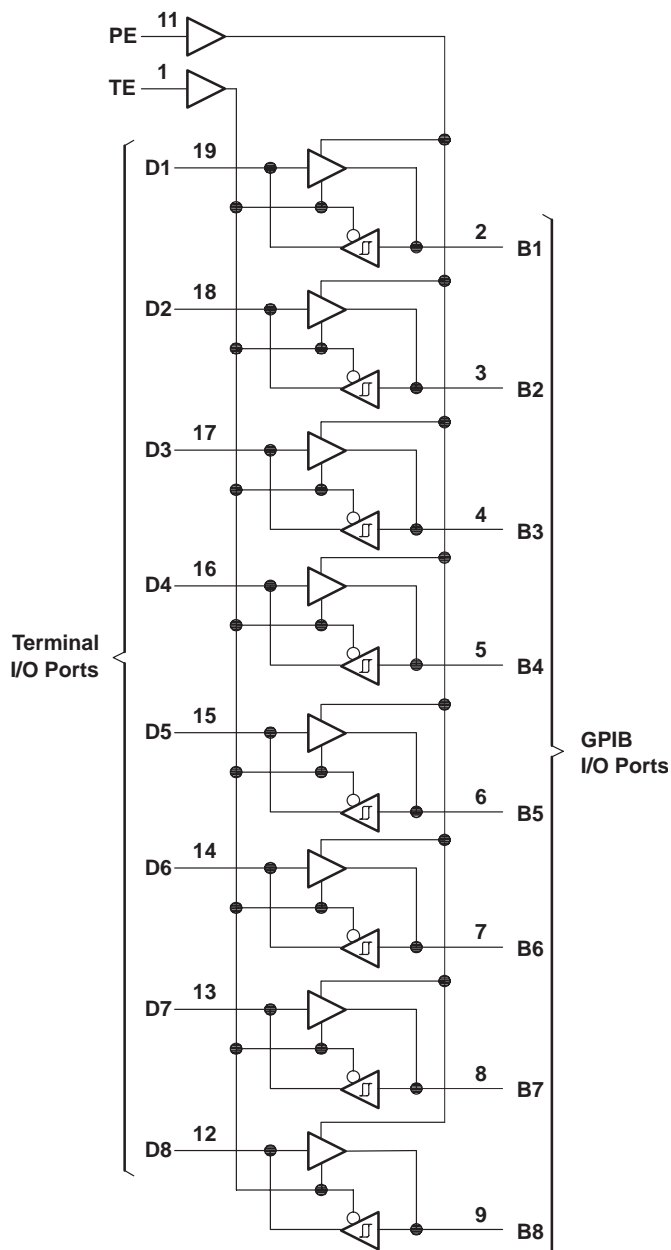


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

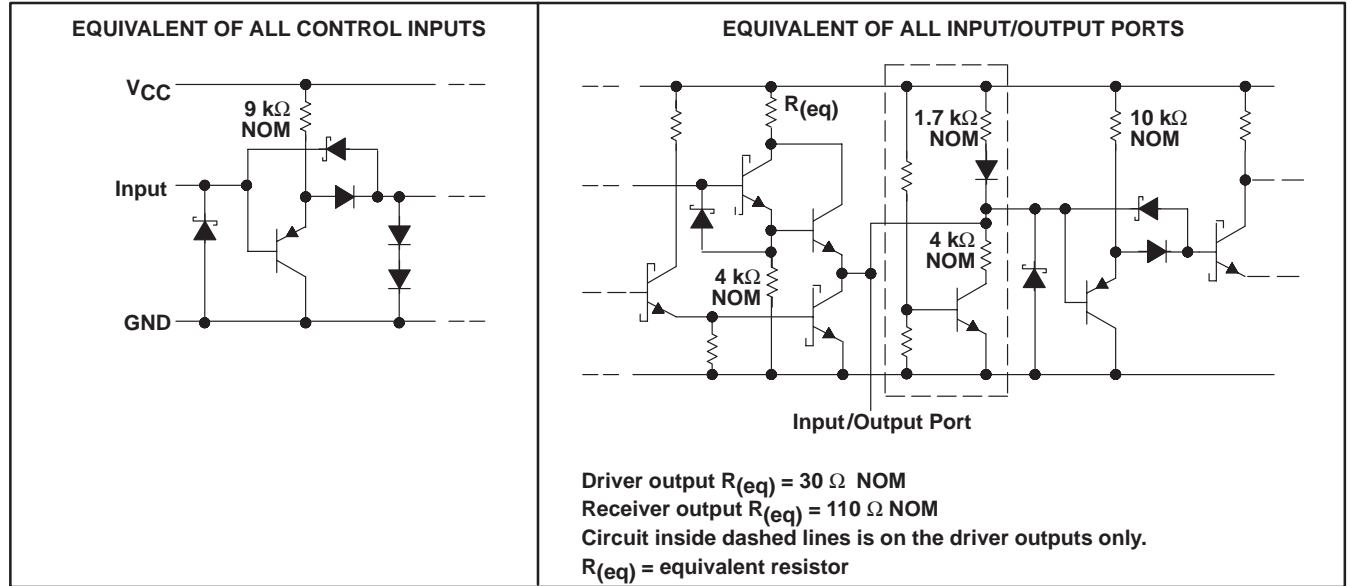
▽ Designates 3-state outputs

⊕ Designates passive-pullup outputs

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|--|------------------------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage, V_I | 5.5 V |
| Low-level driver output current, I_{OL} | 100 mA |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, T_A | 0°C to 70°C |
| Storage temperature range, T_{stg} | –65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING |
|---------|---|---|--|
| DW | 1125 mW | 9.0 mW/°C | 720 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

SN75160B

OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

SLLS004B – OCTOBER 1985 – REVISED MAY 1995

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---------------------------------------|-------------------------------|------|-----|------|--------------|
| Supply voltage, V_{CC} | | 4.75 | 5 | 5.25 | V |
| High-level input voltage, V_{IH} | | 2 | | | V |
| Low-level input voltage, V_{IL} | | | | 0.8 | V |
| High-level output current, I_{OH} | Bus ports with pullups active | | | -5.2 | mA |
| | Terminal ports | | | -800 | μ A |
| Low-level output current, I_{OL} | Bus ports | | | 48 | mA |
| | Terminal ports | | | 16 | |
| Operating free-air temperature, T_A | | 0 | | 70 | $^{\circ}$ C |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|-----------------------|--|----------------------------------|--------------------------------------|---|------|------|------|---------|
| V_{IK} | Input clamp voltage | | $I_I = -18$ mA | | -0.8 | -1.5 | | V |
| V_{hys} | Hysteresis voltage ($V_{IT+} - V_{IT-}$) | Bus | See Figure 8 | | 0.4 | 0.65 | | V |
| V_{OH} | High-level output voltage | Terminal | $I_{OH} = -800$ μ A, TE at 0.8 V | | 2.7 | 3.5 | | V |
| | | Bus | $I_{OH} = -5.2$ mA, PE and TE at 2 V | | 2.5 | 3.3 | | |
| V_{OL} | Low-level output voltage | Terminal | $I_{OL} = 16$ mA, TE at 0.8 V | | 0.3 | 0.5 | | V |
| | | Bus | $I_{OL} = 48$ mA, TE at 2 V | | 0.35 | 0.5 | | |
| I_I | Input current at maximum input voltage | Terminal | $V_I = 5.5$ V | | 0.2 | 100 | | μ A |
| I_{IH} | High-level input current | Terminal | $V_I = 2.7$ V | | 0.1 | 20 | | μ A |
| I_{IL} | Low-level input current | Terminal | $V_I = 0.5$ V | | -10 | -100 | | μ A |
| $V_{I/O}(\text{bus})$ | Voltage at bus port | Driver disabled | $I_{I(\text{bus})} = 0$ | | 2.5 | 3.0 | 3.7 | V |
| | | | $I_{I(\text{bus})} = -12$ mA | | | | -1.5 | |
| $I_{I/O}(\text{bus})$ | Current into bus port | Power on | Driver disabled | $V_{I(\text{bus})} = -1.5$ V to 0.4 V | -1.3 | | | mA |
| | | | | $V_{I(\text{bus})} = 0.4$ V to 2.5 V | 0 | | -3.2 | |
| | | | | $V_{I(\text{bus})} = 2.5$ V to 3.7 V | | | 2.5 | |
| | | | | $V_{I(\text{bus})} = 3.7$ V to 5 V | 0 | | 2.5 | |
| | | | | $V_{I(\text{bus})} = 5$ V to 5.5 V | 0.7 | | 2.5 | |
| | | | | $V_{CC} = 0$, $V_{I(\text{bus})} = 0$ to 2.5 V | | | -40 | |
| | | Power off | | | | | | |
| I_{OS} | Short-circuit output current | Terminal | | | -15 | -35 | -75 | mA |
| | | Bus | | | -25 | -50 | -125 | |
| I_{CC} | Supply current | No load | Receivers low and enabled | | 70 | 90 | | mA |
| | | | Drivers low and enabled | | 85 | 110 | | |
| $C_{I/O}(\text{bus})$ | Bus-port capacitance | $V_{CC} = 0$ to 5 V, $f = 1$ MHz | | $V_{I/O} = 0$ to 2 V, | | 16 | | pF |

† All typical values are at $V_{CC} = 5$ V, $T_A = 25^{\circ}$ C.

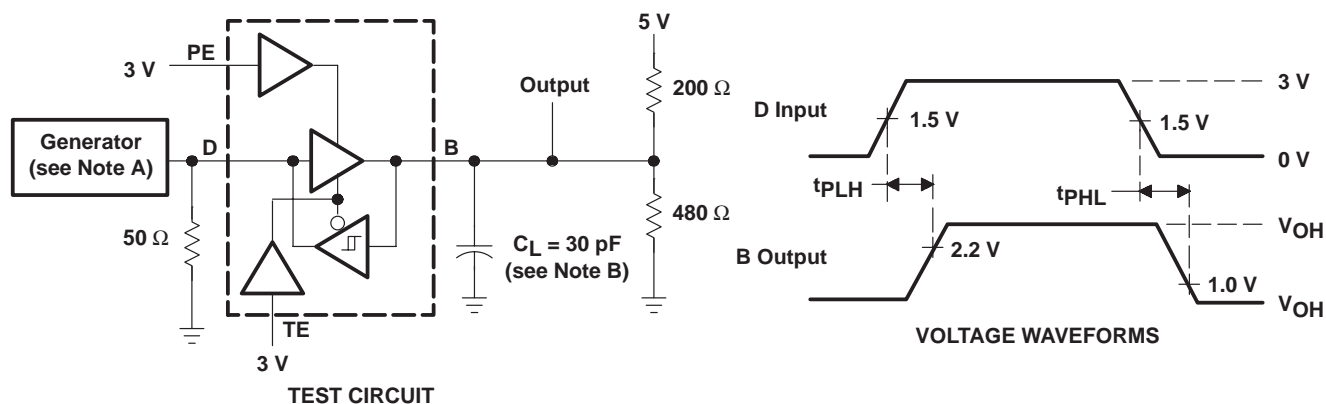


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switching characteristics, $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

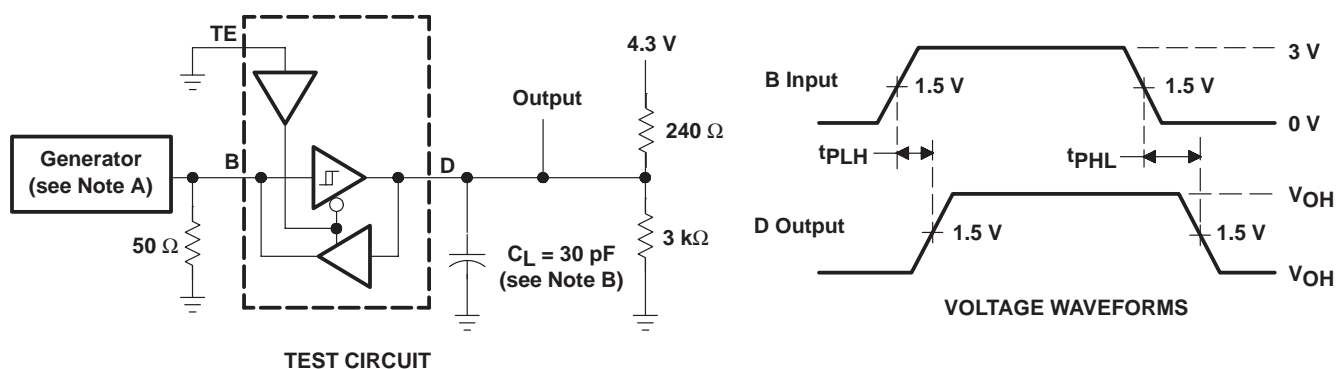
| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--|-----------------|----------------|--|-----|-----|-----|------|
| t_{PLH} | Propation delay time, low- to high-level output | Terminal | Bus | $C_L = 30\text{ pF}$, See Figure 1 | | 14 | 20 | ns |
| t_{PHL} | Propagation delay time, high- to low-level output | | | | | 14 | 20 | |
| t_{PLH} | Propagation delay time, low- to high-level output | Bus | Terminal | $C_L = 30\text{ pF}$, See Figure 2 | | 10 | 20 | ns |
| t_{PHL} | Propagation delay time, high- to low-level output | | | | | 15 | 22 | |
| t_{PZH} | Output enable time to high level | TE | BUS | See Figure 3 | | 25 | 35 | ns |
| t_{PHZ} | Output disable time from high level | | | | | 13 | 22 | |
| t_{PZL} | Output enable time to low level | | | | | 22 | 35 | |
| t_{PLZ} | Output disable time from low level | | | | | 22 | 32 | |
| t_{PZH} | Output enable time to high level | TE | Terminal | See Figure 4 | | 20 | 30 | ns |
| t_{PHZ} | Output disable time from high level | | | | | 12 | 20 | |
| t_{PZL} | Output enable time to low level | | | | | 23 | 32 | |
| t_{PLZ} | Output disable time from low level | | | | | 19 | 30 | |
| t_{en} | Output pullup enable time | PE | Bus | See Figure 5 | | 15 | 22 | ns |
| t_{dis} | Output pullup disable time | | | | | 13 | 20 | |

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, t_r \leq 6 ns, t_f \leq ns, Z_O = 50 Ω .
 B. C_L includes probe and jig capacitance.

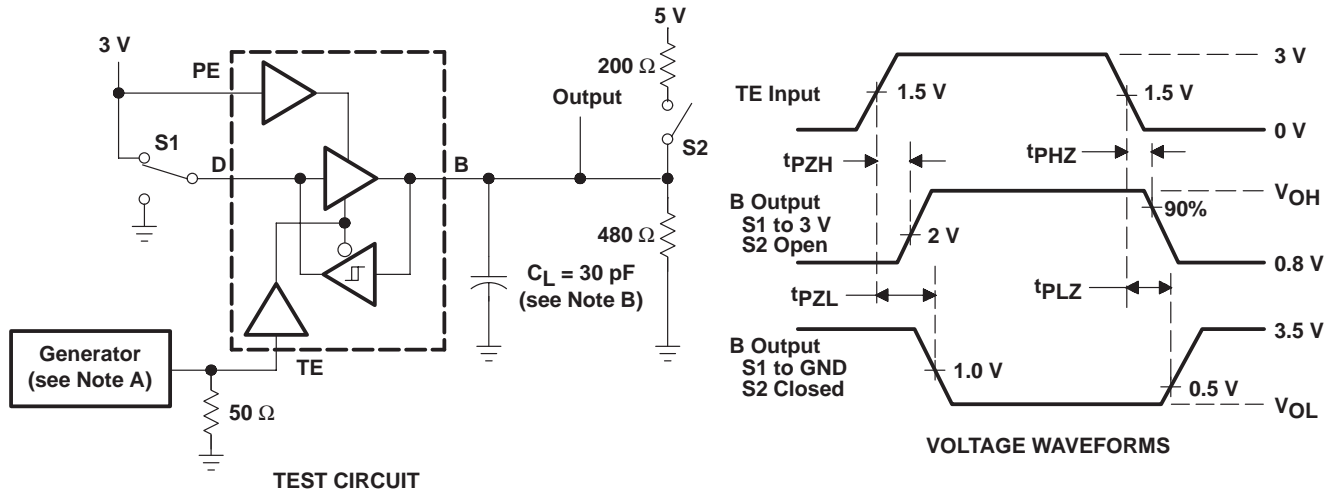
Figure 1. Terminal-to-Bus Test Circuit and Voltage Waveforms



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, t_r \leq 6 ns, t_f \leq ns, Z_O = 50 Ω .
 B. C_L includes probe and jig capacitance.

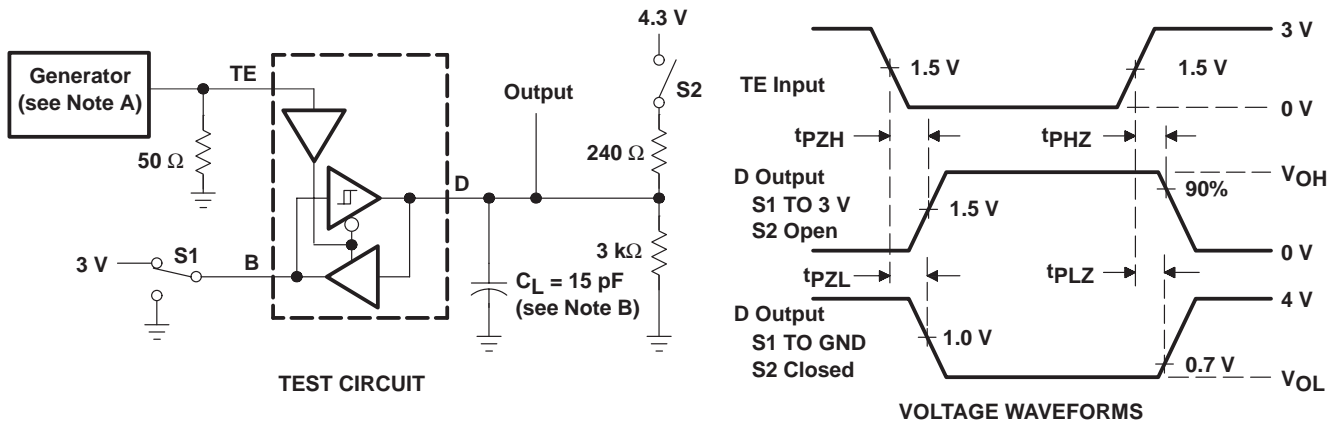
Figure 2. Bus-to-Terminal Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq \text{ns}$, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

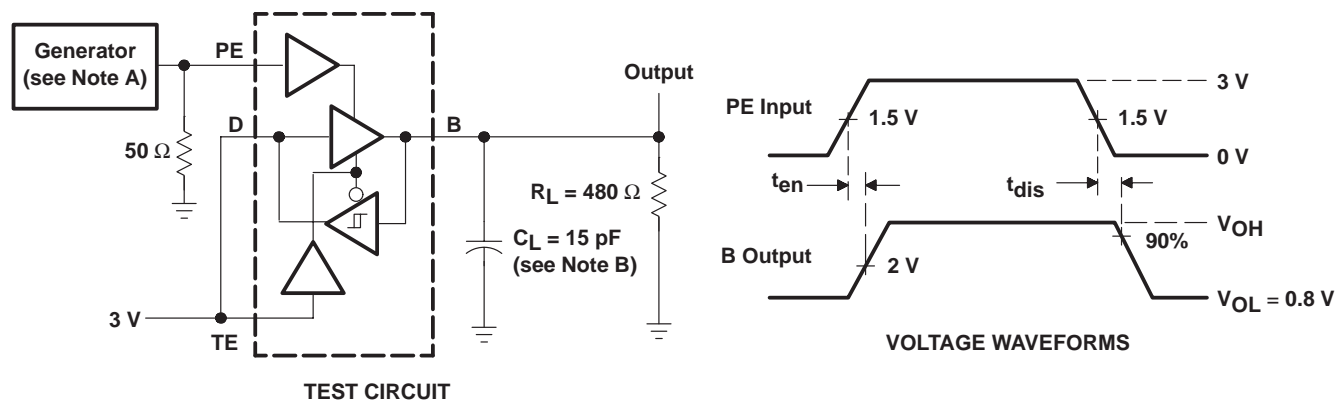
Figure 3. TE-to-Bus Test Circuit and Voltage Waveforms



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq \text{ns}$, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 4. TE-to-Terminal Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $\text{PRR} \leq 1\ \text{MHz}$, 50% duty cycle, $t_r \leq 6\ \text{ns}$, $t_f \leq \text{ns}$, $Z_0 = 50\ \Omega$.
- B. C_L includes probe and jig capacitance.

Figure 5. PE-to-Bus Pullup Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

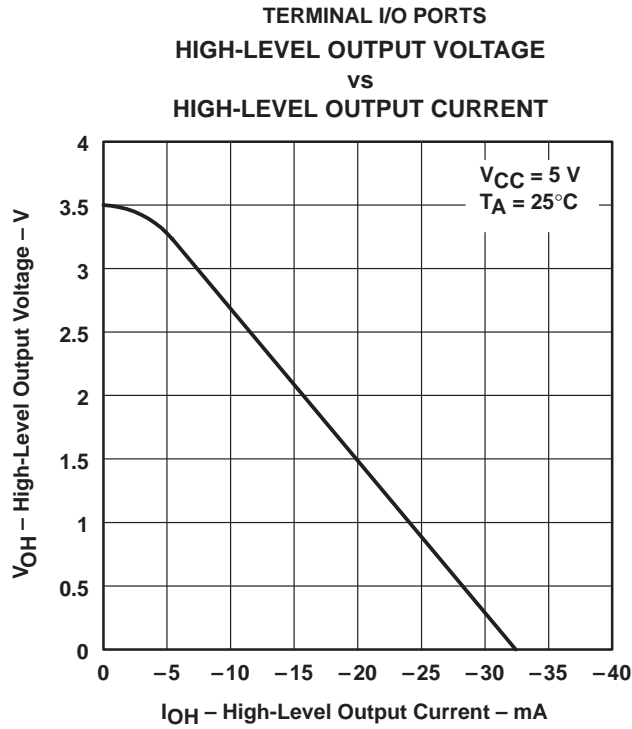


Figure 6

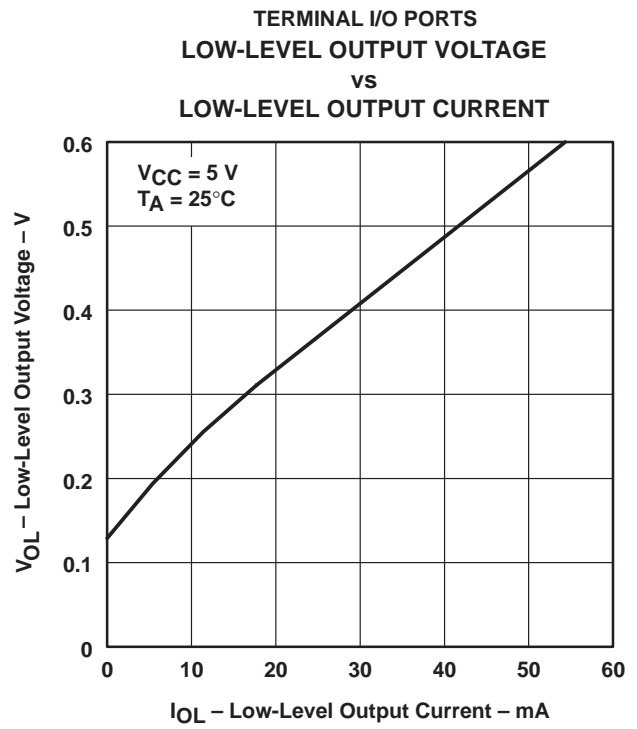


Figure 7

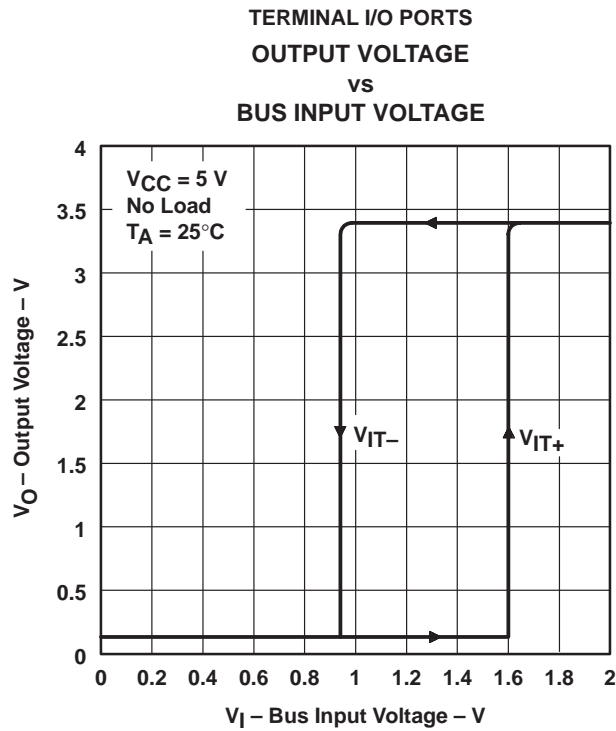


Figure 8

TYPICAL CHARACTERISTICS

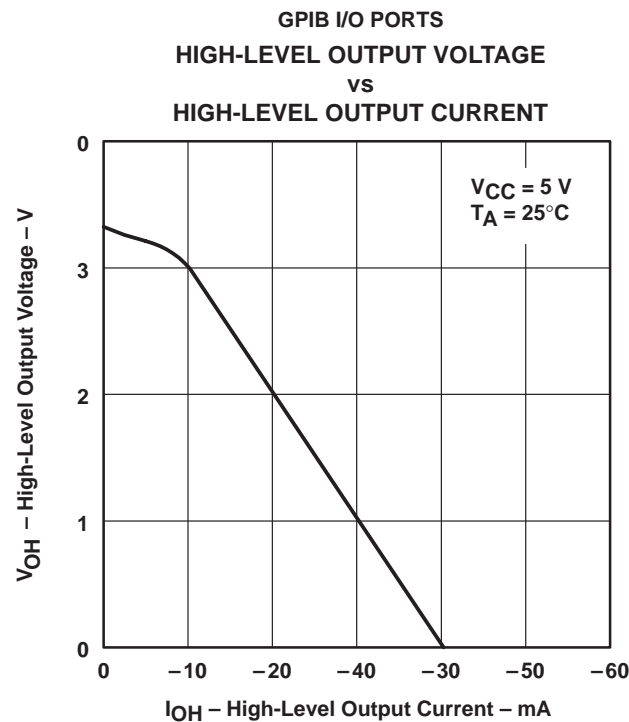


Figure 9

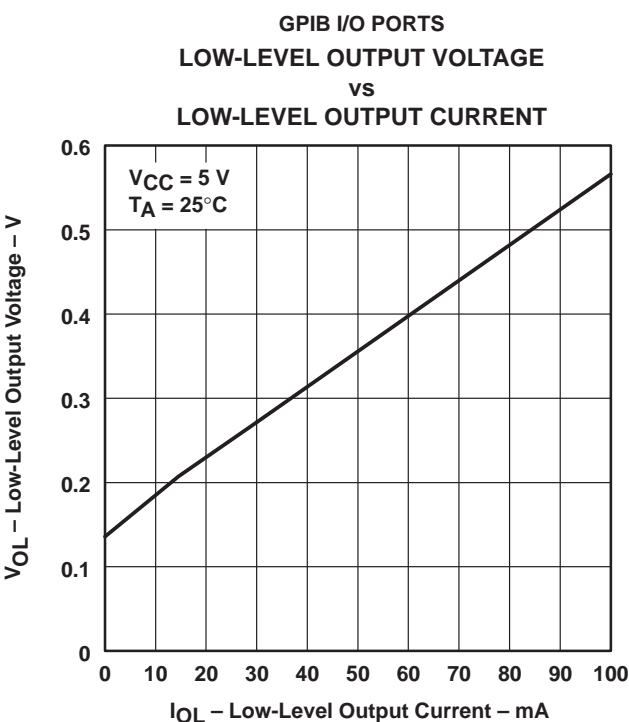


Figure 10

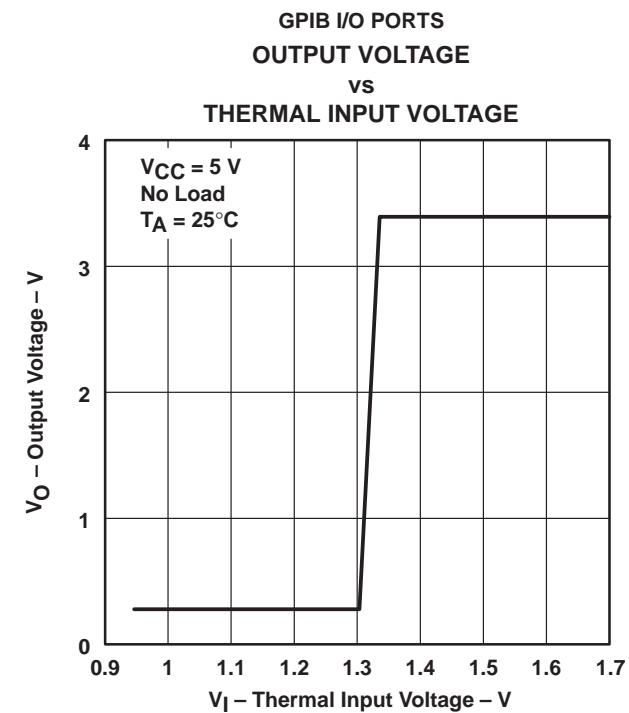


Figure 11

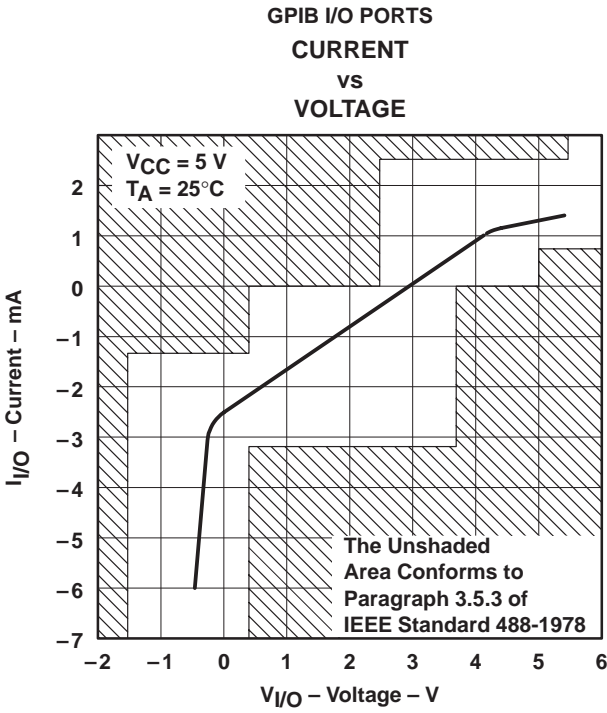


Figure 12

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN75160BDW | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75160B |
| SN75160BDW.A | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75160B |
| SN75160BDWE4 | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75160B |
| SN75160BDWG4 | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75160B |
| SN75160BDWR | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75160B |
| SN75160BDWR.A | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75160B |
| SN75160BDWRE4 | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75160B |
| SN75160BDWRG4 | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75160B |
| SN75160BN | Active | Production | PDIP (N) 20 | 20 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN75160BN |
| SN75160BN.A | Active | Production | PDIP (N) 20 | 20 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN75160BN |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75160BDWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75160BDWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |

TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN75160BDW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN75160BDW | DW | SOIC | 20 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN75160BDW.A | DW | SOIC | 20 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN75160BDW.A | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN75160BDWE4 | DW | SOIC | 20 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN75160BDWE4 | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN75160BDWG4 | DW | SOIC | 20 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN75160BDWG4 | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN75160BN | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN75160BN.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



| PINS ** | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| DIM | | | | |
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |

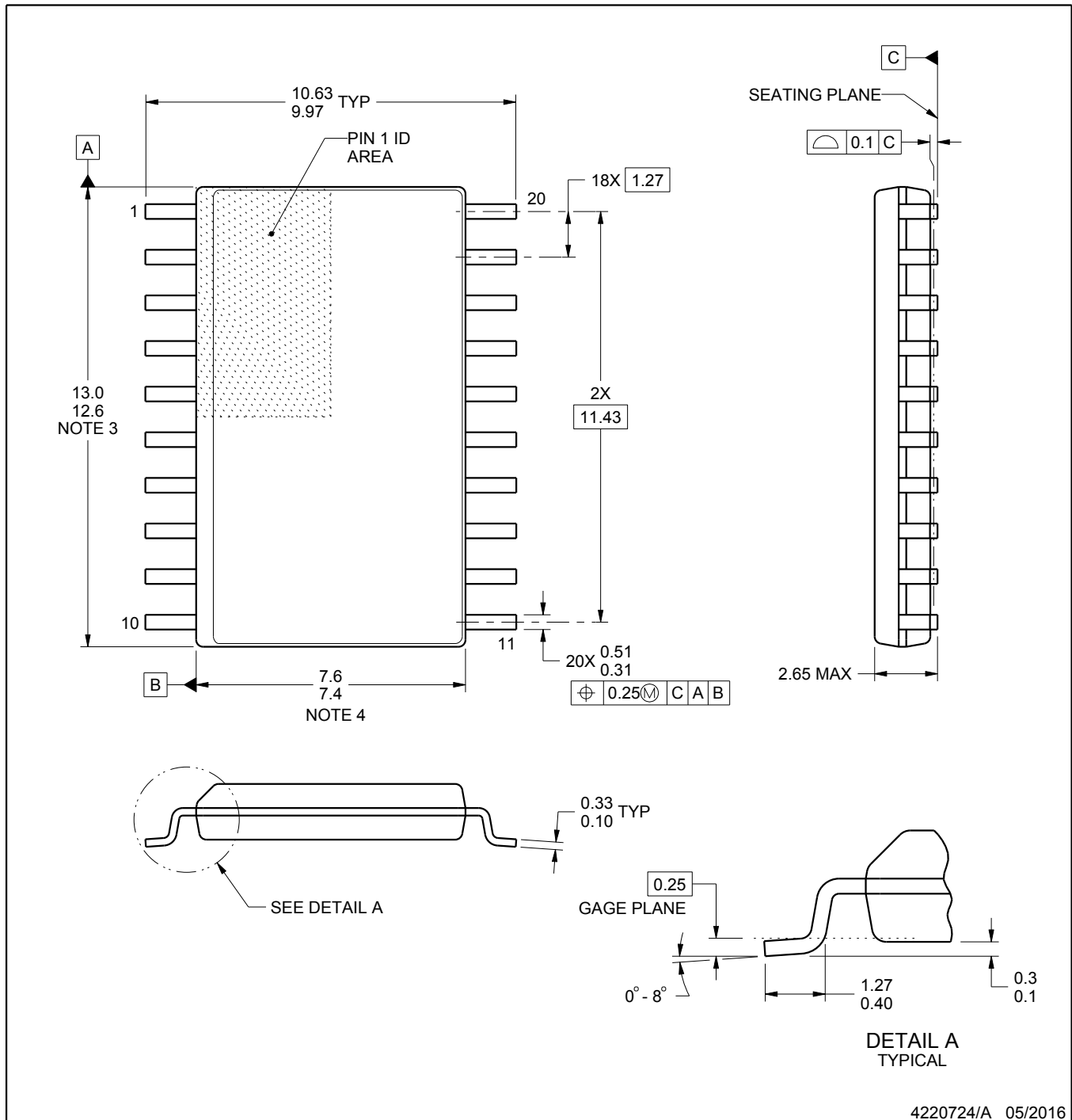


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A**PACKAGE OUTLINE****SOIC - 2.65 mm max height**

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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