High Speed Four Channel MOSFET Driver with Two Inverting and Two Non-Inverting Outputs

Features

- Mixed inversion MOSFET driver
- 6.0ns rise and fall time
- 2.0A peak output source/sink current
- 1.8 to 5.0V input CMOS compatible
- 5.0 to 10V total supply voltage
- Smart logic threshold
- Low jitter design
- Four matched channels
- Drives two P- and two N-channel MOSFETs
- Outputs can swing below ground
- Low inductance, quad flat no-lead package
- High performance, thermally enhanced packaging

Applications

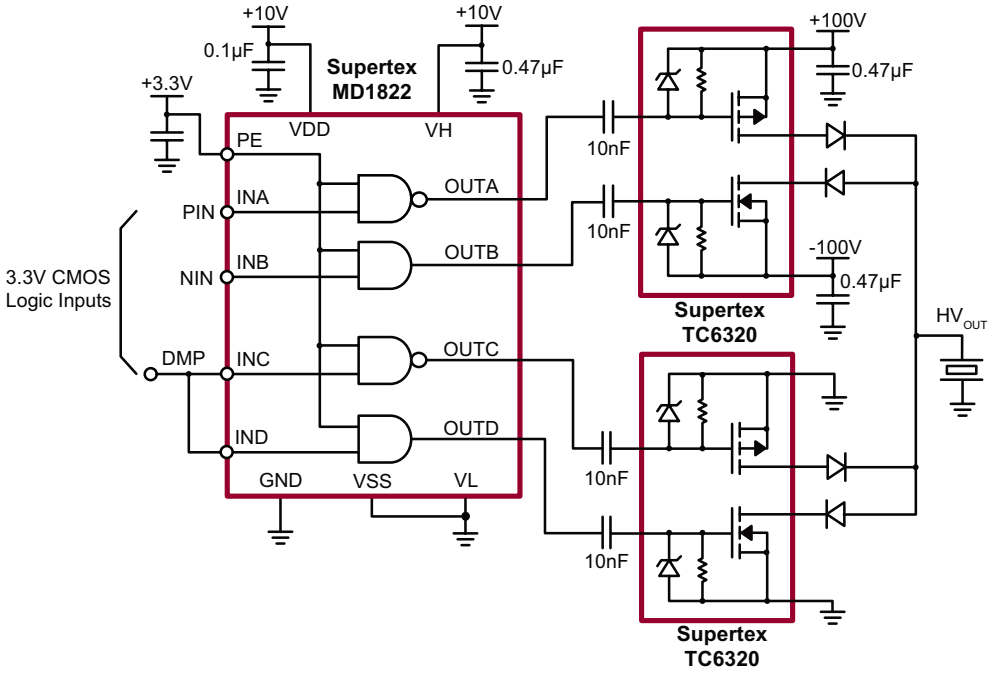
- Medical ultrasound imaging
- Piezoelectric transducer drivers
- Non-Destructive Testing (NDT)
- PIN diode driver
- CCD Clock driver/buffer
- High speed level translator

General Description

The Supertex MD1822 is a high speed, four channel MOSFET driver designed to drive high voltage P- and N-channel MOSFETs for medical ultrasound applications and other applications requiring a high output current for a capacitive load. The high-speed input stage of the MD1822 can operate from a 1.8 to 5.0V logic interface with an optimum operating input signal range of 1.8 to 3.3V. An adaptive threshold circuit is used to set the level translator switch threshold to the average of the input logic 0 and logic 1 levels. The input logic levels may be ground referenced, even though the driver is putting out bipolar signals. The level translator uses a proprietary circuit, which provides DC coupling together with high-speed operation.

The output stage of the MD1822 has separate power connections enabling the output signal L and H levels to be chosen independently from the supply voltages used for the majority of the circuit. As an example, the input logic levels may be 0 and 1.8V, the control logic may be powered by +5.0 and -5.0V, and the output L and H levels may be varied anywhere over the range of -5.0 to +5.0V. The output stage is capable of peak currents of up to ±2.0A, depending on the supply voltages used and load capacitance present. The PE pin serves a dual purpose. First, its logic H level is used to compute the threshold voltage level for the channel input level translators. Second, when PE is low, the outputs are disabled, with the A & C output high and the B & D output low. This assists in properly precharging the AC coupling capacitors that may be used in series in the gate drive circuit of an external PMOS and NMOS transistor pair.

Typical Application Circuit



Ordering Information

Device	16-Lead QFN *3.00x3.00mm body* *1.00mm height (max)* *0.50mm pitch*
MD1822	MD1822K6-G

-G indicates package is RoHS compliant ('Green')

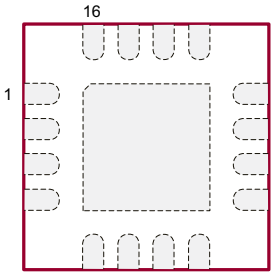
Absolute Maximum Ratings

Parameter	Value
V_{DD}-V_{SS}, Logic supply voltage	-0.5V to +12.5V
V_H, Output high supply voltage	V_L - 0.5V to V_{DD} +0.5V
V_L, Output low supply voltage	V_{SS} - 0.5V to V_H+0.5V
V_{SS}, Low side supply voltage	-6.0V to +0.5V
Logic input levels	V_{SS} - 0.5V to GND +5.5V
Maximum junction temperature	+125°C
Storage temperature	-65°C to 150°C
Operating temperature	-20°C to +85°C
Package power dissipation	2.2W
Thermal resistance (θ_{JA})*	55°C/W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

** 1.0oz 4-layer 3x4" PCB*

Pin Configuration



16-Lead QFN (K6)
(top view)

Product Marking

Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
____ = "Green" Packaging

Package may or may not include the following marks: Si or

16-Lead QFN (K6)

DC Electrical Characteristics *(V_H = V_{DD} = 10V, V_L = V_{SS} = GND = 0V, V_{PE} = 3.3V, T_A = 25°C)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{DD} - V_{SS}	Logic supply voltage	4.75	-	11.5	V	4.0V ≤ V_{DD} ≤11.5V
V_{SS}	Low side supply voltage	-5.5	-	0	V	---
V_H	Output high supply voltage	V_{SS} +2.0	-	V_{DD}	V	---
V_L	Output low supply voltage	V_{SS}	-	V_{DD} -4.0	V	---
I_{DDQ}	V_{DD} quiescent current	-	60	-	µA	No input transitions, PE = 0
I_{HQ}	V_H quiescent current	-	2.0	-	µA	
I_{DDQ}	V_{DD} quiescent current	-	1.0	-	mA	No input transitions, PE = 1
I_{HQ}	V_H quiescent current	-	2.0	-	µA	
I_{DD}	V_{DD} average current	-	4.0	-	mA	One channel on at 5.0Mhz, No load
I_H	V_H average current	-	10	-	mA	
V_{IH}	Input logic voltage high	V_{PE} -0.3	-	V_{PE}	V	For logic inputs INA, INB, INC, and IND
V_{IL}	Input logic voltage low	0	-	0.3	V	
I_{IH}	Input logic current high	-		1.0	µA	
I_{IL}	Input logic current low	-	-	1.0	µA	
V_{IH}	PE input logic voltage high	1.70	3.30	5.25	V	For logic input PE
V_{IL}	PE input logic voltage low	0	-	0.3	V	
R_{IN_PE}	PE input impedance to GND	100	-	-	KΩ	

DC Electrical Characteristics *(cont.)* ($V_H = V_{DD} = 10V$, $V_L = V_{SS} = GND = 0V$, $V_{PE} = 3.3V$, $T_A = 25°C$)

Sym	Parameter	Min	Typ	Max	Units	Conditions
C_{IN}	Logic input capacitance	-	5.0	10	pF	---
R_{SINK}	Output sink resistance	-	1.5	-	Ω	I_{SINK} = 50mA
R_{SOURCE}	Output source resistance	-	2.0	-	Ω	I_{SOURCE} = 50mA
I_{SINK}	Peak output sink current	-	2.0	-	A	---
I_{SOURCE}	Peak output source current	-	2.0	-	A	---

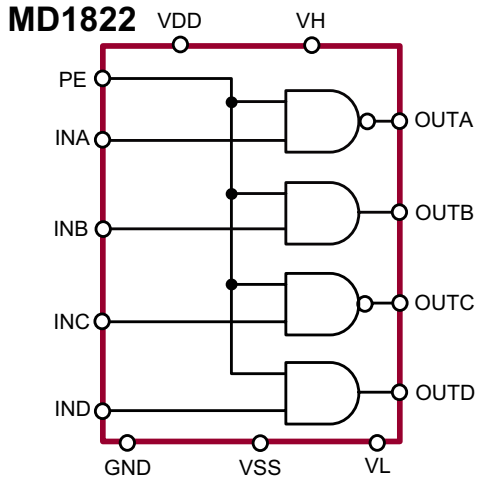
AC Electrical Characteristics ($V_H = V_{DD} = 10V$, $V_L = V_{SS} = GND = 0V$, $V_{PE} = 3.3V$, $T_A = 25°C$)

Sym	Parameter	Min	Typ	Max	Units	Conditions
t_{irf}	Input or PE rise & fall time	-	-	10	ns	Logic input edge speed requirement
t_{PLH}	Propagation delay when output is from low to high	-	6.5	-	ns	C_{LOAD} = 1000pF, see timing diagram Input signal rise/fall time 2.0ns
t_{PHL}	Propagation delay when output is from high to low	-	6.5	-	ns	
t_r	Output rise time	-	7.0	-	ns	
t_f	Output fall time	-	7.0	-	ns	
$\lvert t_r - t_f \rvert$	Rise and fall time matching	-	1.0	-	ns	For each channel
$\lvert t_{PLH} - t_{PHL} \rvert$	Propagation low to high and high to low matching	-	1.0	-	ns	
Δt_{dm}	Propagation delay matching	-	±2.0	-	ns	Device to device delay match
t_{PE-ON}	PE on-time	-	-	5.0	µs	V_{PE} = 1.7 ~ 5.25V V_{DD} = 7.5 ~ 11.5V -20 ~ 85°C
t_{PE-OFF}	PE off-time	-	-	4.0	µs	

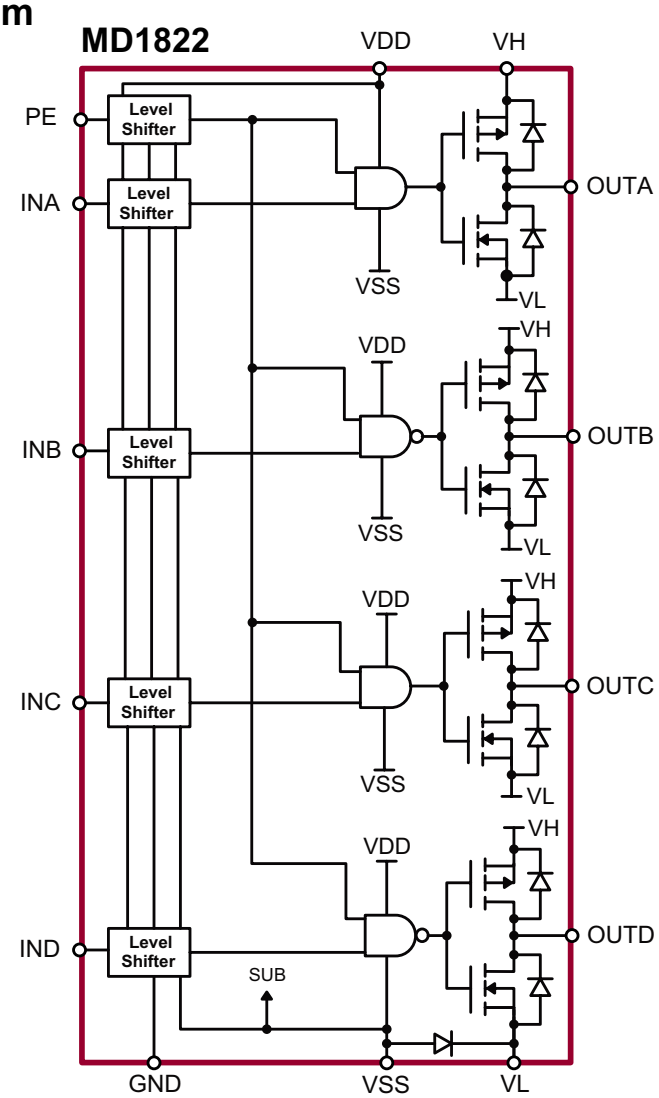
Logic Truth Table

Logic Inputs			Output	
PE	**INA**	**INB**	**OUTA**	**OUTB**
H	L	H	V_H	V_H
H	L	L	V_H	V_L
H	H	H	V_L	V_H
H	H	L	V_L	V_L
L	X	X	V_H	V_L
PE	**INC**	**IND**	**OUTC**	**OUTD**
H	L	H	V_H	V_H
H	L	L	V_H	V_L
H	H	H	V_L	V_H
H	H	L	V_L	V_L
L	X	X	V_H	V_L

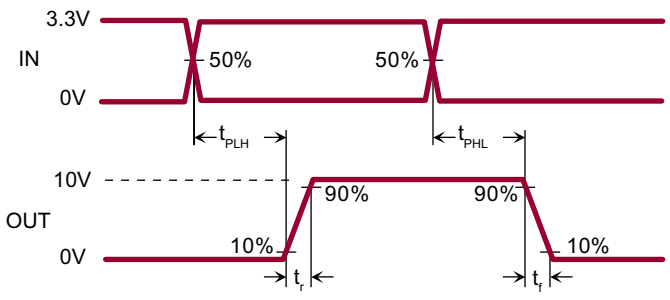
Simplified Block Diagram



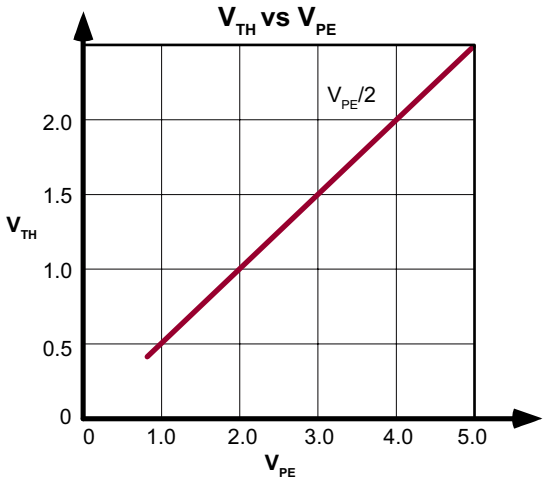
Detailed Block Diagram



Timing Diagram



V_{TH} / V_{PE} Curve



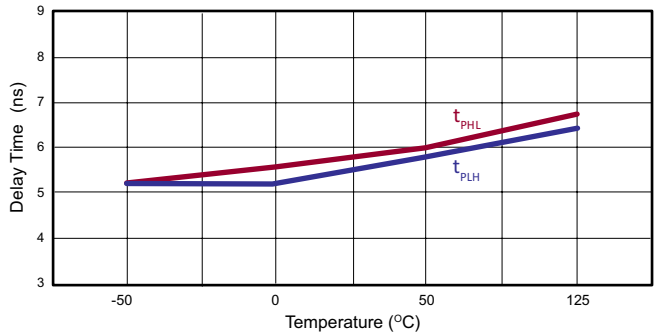
Application Information

For proper operation of the MD1822, low inductance bypass capacitors should be used on the various supply pins. The GND pin should be connected to the logic ground. The INA, INB, INC, IND, and PE pins should be connected to a logic source with a swing of GND to PE, where PE is 1.8 to 5.0V. Good trace practices should be followed corresponding to the desired operating speed. The internal circuitry of the MD1822 is capable of operating up to 100MHz, with the primary speed limitation being the loading effects of the load capacitance. Because of this speed and the high transient currents that result with capacitive loads, the bypass capacitors should be as close to the chip pins as possible. Unless the load specifically requires bipolar drive, the VSS and VL pins should have low inductance feed-through connections directly to a ground plane. If these voltages are not zero, then they need bypass capacitors in a manner similar to the positive power supplies. The power connection VDD should have a ceramic bypass capacitor to the ground plane with short leads and decoupling components to prevent resonance in the powerleads.

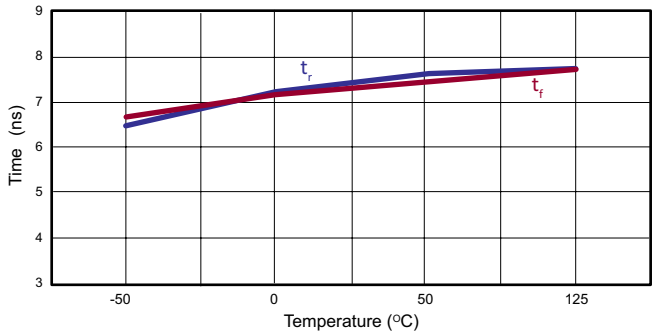
The voltages of VH and VL decide the output signal levels. These two pins can draw fast transient currents of up to 2.0A, so they should be provided with an appropriate bypass capacitor located next to the chip pins. A ceramic capacitor of up to 1.0µF may be appropriate, with a series ferrite bead to prevent resonance in the power supply lead coming to the capacitor. Pay particular attention to minimizing trace lengths, current loop area and using sufficient trace width to reduce inductance. Surface mount components are highly recommended. Since the output impedance of this driver is very low, in some cases it may be desirable to add a small series resistance in series with the output signal to obtain better waveform transitions at the load terminals. This will of course reduce the output voltage slew rate at the terminals of a capacitive load.

Pay particular attention that parasitic couplings are minimized from the output to the input signal terminals. The parasitic feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 1.8V even small coupled voltages may cause problems. Use of a solid ground plane and good power and signal layout practices will prevent this problem. Be careful that a circulating ground return current from a capacitive load cannot react with common inductance to cause noise voltages in the input logic circuitry.

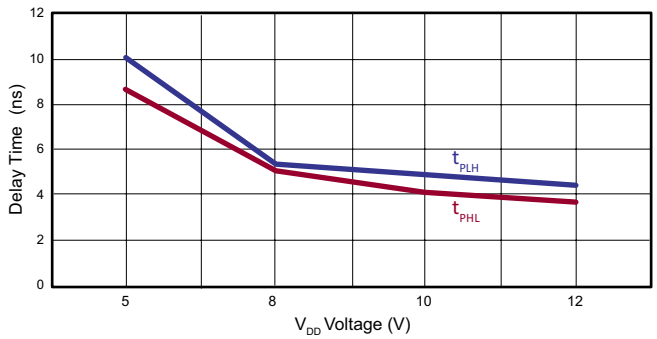
MD1822 Delay vs Temperature



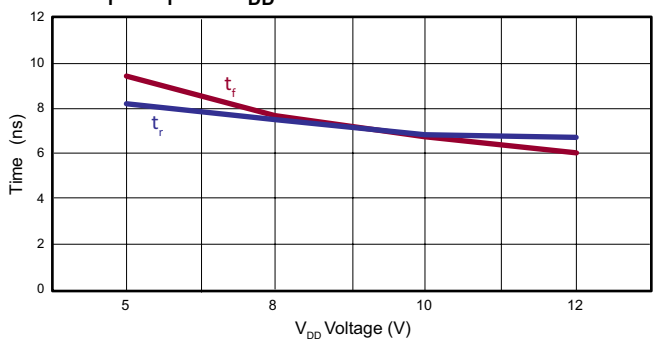
MD1822 t_r & t_f vs Temperature



MD1822 Delay vs V_{DD}



MD1822 t_r & t_f vs V_{DD}

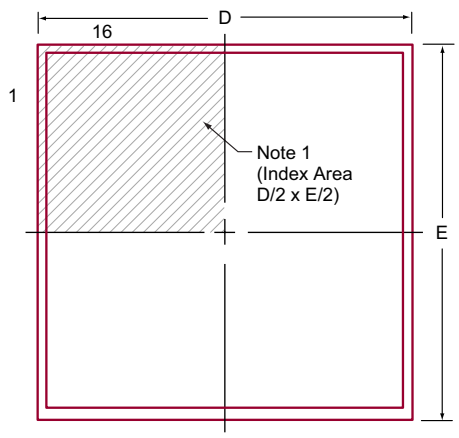


Pin Description

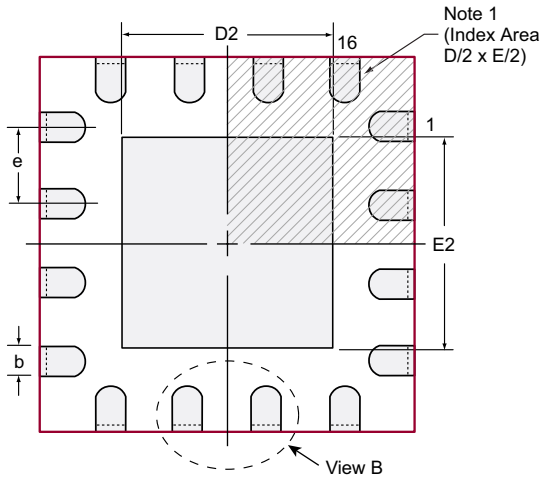
Pin #	Function	Description
1	INB	Logic input.
2	VDD	High side supply voltage.
3	VSS	Low side supply voltage. VSS is also connected to the IC substrate. It is required to connect to the most negative potential of voltage supplies.
4	INC	Logic input.
5	IND	
6	GND	Logic input ground reference.
7	VL	Supply voltage for N-channel output stage.
8	OUTC	Output drivers
9	OUTD	
10, 11	VH	Supply voltage for P-channel output stage.
12	OUTA	Output drivers
13	OUTB	
14	VL	Supply voltage for N-channel output stage.
15	PE	Power enable logic input. When PE is high, sets the input logic threshold. When PE is low, all outputs are at default state (see truth table) and IC in standby mode.
16	INA	Logic input.
Substrate		The IC substrate is internally connected to the thermal pad. Thermal pad and VSS must be connected externally.

16-Lead QFN Package Outline (K6)

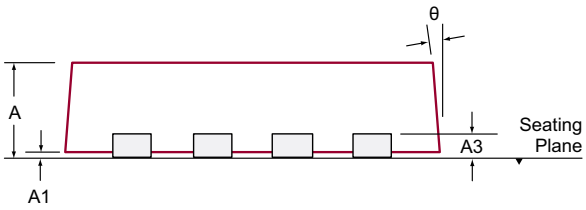
3.00x3.00mm body, 1.00mm height (max), 0.50mm pitch



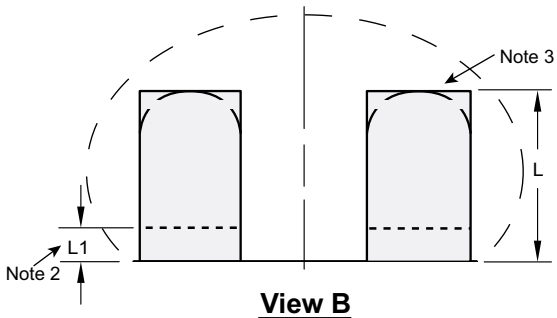
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	2.85*	1.50	2.85*	1.50	0.50 BSC	0.20†	0.00	0°
	NOM	0.90	0.02		0.25	3.00	1.65	3.00	1.65		0.30†	-	-
	MAX	1.00	0.05		0.30	3.15*	1.80	3.15*	1.80		0.45	0.15	14°

JEDEC Registration MO-220, Variation VEED-4, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc.#: *DSPD-16QFNK63X3P050, Version A092909.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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