ADC1061 10-Bit High-Speed µP-Compatible A/D Converter with Track/Hold Function

Check for Samples: ADC1061

FEATURES

- **1.8 µs Maximum Conversion Time to 10 Bits**
- **Low Power Dissipation: 235 mW (Maximum)**
- **Built-In Track-and-Hold**
- **No External Clock Required**
- **Single +5V Supply**
- **No Missing Codes Over Temperature**

APPLICATIONS

- **Waveform Digitizers**
- **Disk Drives**
- **Digital Signal Processor Front Ends**
- **Mobile Telecommunications**

DESCRIPTION

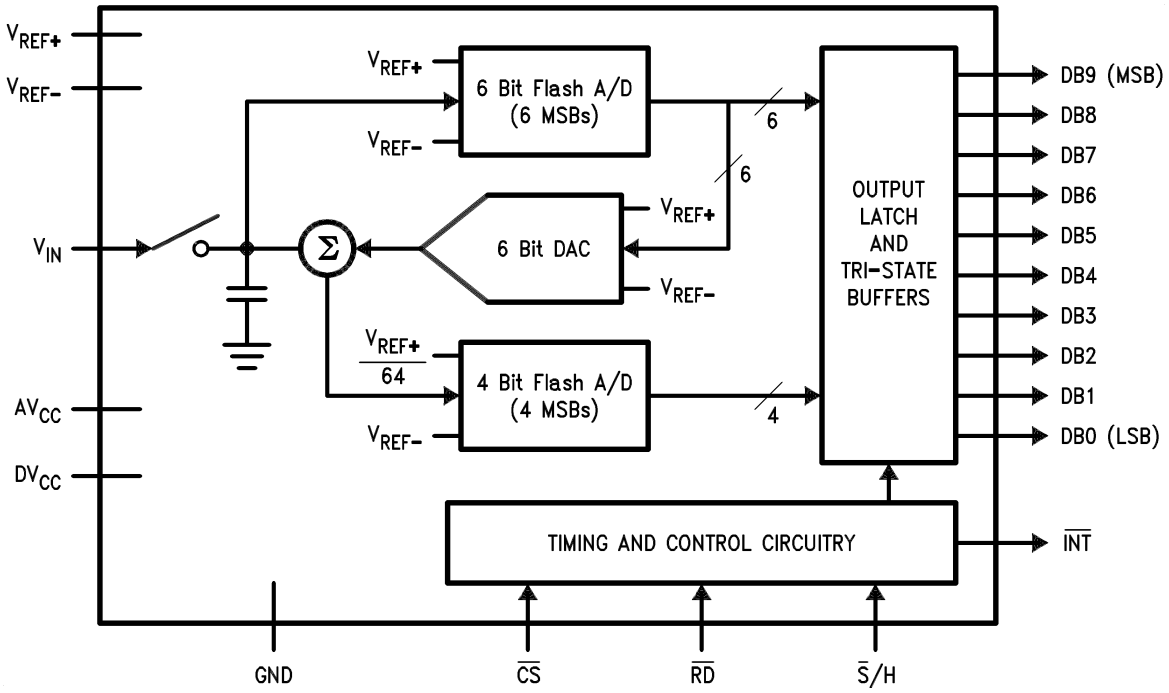
This product is on Lifetime Buy notification and NOT RECOMMENDED FOR NEW DESIGNS.

Using a modified half-flash conversion technique, the 10-bit ADC1061 CMOS analog-to-digital converter offers very fast conversion times yet dissipates a maximum of only 235 mW. The ADC1061 performs a 10-bit conversion in two lower-resolution “flashes”, thus yielding a fast A/D without the cost, power dissipation, and other problems associated with true flash approaches.

The analog input voltage to the ADC1061 is tracked and held by an internal sampling circuit. Input signals at frequencies from DC to greater than 160 kHz can therefore be digitized accurately without the need for an external sample-and-hold circuit.

For ease of interface to microprocessors, the ADC1061 has been designed to appear as a memory location or I/O port without the need for external interface logic.

Simplified Block and Connection Diagrams



Connection Diagram

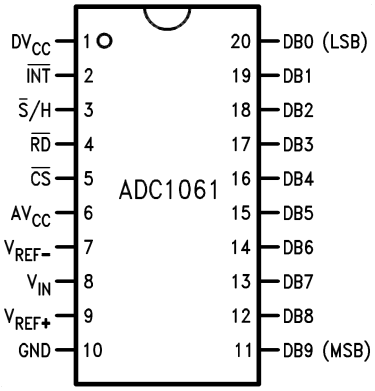


Figure 1. Dual-In-Line Package
CDIP, SOIC, and PDIP Packages (Top View)
See Package Number P, DW, or NFH

PIN DESCRIPTIONS

Symbol	Function
DV_{CC}, AV_{CC} (1, 6)	These are the digital and analog positive supply voltage inputs. They should always be connected to the same voltage source, but are brought out separately to allow for separate bypass capacitors. Each supply pin should be bypassed with a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor.
$\overline{INT}$ (2)	This is the active low interrupt output. $\overline{INT}$ goes low at the end of each conversion, and returns to a high state following the rising edge of $\overline{RD}$.
$\overline{S}$ /H (3)	This is the Sample/Hold control input. When this pin is forced low, it causes the analog input signal to be sampled and initiates a new conversion.
$\overline{RD}$ (4)	This is the active low Read control input. When this pin is low, any data present in the ADC1061's output registers will be placed on the data bus. In Mode 2, the Read signal must be low until $\overline{INT}$ goes low. Until $\overline{INT}$ goes low, the data at the output pins will be incorrect.
$\overline{CS}$ (5)	This is the active low Chip Select control input. This pin enables the $\overline{S}$ /H and $\overline{RD}$ inputs.
V_{REF-}, V_{REF+} (7, 9)	These are the reference voltage inputs. They may be placed at any voltage between GND − 50 mV and V_{CC} + 50 mV, but V_{REF+} must be greater than V_{REF-}. An input voltage equal to V_{REF-} produces an output code of 0, and an input voltage equal to V_{REF+} − 1LSB produces an output code of 1023.
V_{IN} (8)	This is the analog input pin. The impedance of the source should be less than 500Ω for best accuracy and conversion speed. To avoid damage to the ADC1061, V_{IN} should not be allowed to extend beyond the power supply voltages by more than 300 mV unless the drive current is limited. For accurate conversions, V_{IN} should not extend more than 50 mV beyond the supply voltages.
GND (10)	This is the power supply ground pin. The ground pin should be connected to a “clean” ground reference point.
DB0–DB9 (11-20)	These are the TRI-STATE output pins.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1) (2)(3)

Supply Voltage ($V^+ = AV_{CC} = DV_{CC}$)			−0.3V to +6V
Voltage at any Input or Output			−0.3V to V^+ +0.3V
Input Current at Any Pin(4)			5 mA
Package Input Current(4)			20 mA
Power Dissipation(5)			875 mW
ESD Susceptibility(6)			1500V
Soldering Information	NFH Package (10 seconds)		260°C
	P Package (10 seconds)		300°C
	DW Package	Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C
Junction Temperature, T_J			+150°C
Storage Temperature Range			−65°C to +150°C

(1) All voltages are measured with respect to GND, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can safely exceed the power supplies with an input of 5 mA to four.
(5) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{JMAX} = 150°C, and the typical thermal resistance (θ_{JA}) when board mounted is 47°C/W for the plastic (NFH) package, 85°C/W for the ceramic (P) package, and 65°C/W for the small outline (DW) package.
(6) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

OPERATING RATINGS(1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC1061CIN, ADC1061CIWM	−40°C ≤ T_A ≤ +85°C
Supply Voltage Range	+4.5V to +5.5V

(1) All voltages are measured with respect to GND, unless otherwise specified.

CONVERTER CHARACTERISTICS

The following specifications apply for V^+ = +5V, $V_{REF(+)}$ = 5V, and $V_{REF(-)}$ = GND unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical (1)	Limit (2)	Units (Limit)
	Resolution			**10**	Bits
TUE	Total Unadjusted Error		±1.0	**±2.0**	LSB (Max)
INL	Integral Linearity Error		±0.3	**±1.5**	LSB (Max)
DLE	Differential Linearity Error			**±1.0**	LSB (Max)
OE	Offset Error		±0.1	**±1.0**	LSB (Max)
FSE	Fullscale Error		±0.5	**±1.0**	LSB (Max)
R_{REF}	Reference Resistance		0.65	**0.4**	kΩ (Min)
R_{REF}	Reference Resistance		0.65	**0.9**	kΩ (Max)
$V_{REF(+)}$	$V_{REF(+)}$ Input Voltage			**V^+ + 0.05**	V (Max)
$V_{REF(-)}$	$V_{REF(-)}$ Input Voltage			**GND − 0.05**	V (Min)
$V_{REF(+)}$	$V_{REF(+)}$ Input Voltage			**$V_{REF(-)}$**	V (Min)
$V_{REF(-)}$	$V_{REF(-)}$ Input Voltage			**$V_{REF(-)}$**	V (Max)
V_{IN}	Input Voltage			**V^+ + 0.05**	V (Max)
V_{IN}	Input Voltage			**GND − 0.05**	V (Min)
	Analog Input Leakage Current	$\overline{CS}$ = V^+, V_{IN} = V^+ $\overline{CS}$ = V^+, V_{IN} = GND	0.01 0.01	**3** **−3**	µA (Max) µA (Max)
	Power Supply Sensitivity	V^+ = 5V ±5% V_{REF} = 4.75V	±0.125	**±0.5**	LSB

(1) Typicals are at 25°C and represent most likely parametric norm.
(2) Limits are specified to AOQL (Average Outgoing Quality Level).

DC ELECTRICAL CHARACTERISTICS

The following specifications apply for V^+ = +5V, $V_{REF(+)}$ = 5V, and $V_{REF(-)}$ = GND unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical (1)	Limit (2)	Units (Limits)
$V_{IN(1)}$	Logical “1” Input Voltage	V^+ = 5.25V		**2.0**	V (Min)
$V_{IN(0)}$	Logical “0” Input Voltage	V^+ = 4.75V		**0.8**	V (Max)
$I_{IN(1)}$	Logical “1” Input Current	$V_{IN(1)}$ = 5V	0.005	**1.0**	µA (Max)
$I_{IN(0)}$	Logical “0” Input Current	$V_{IN(0)}$ = 0V	−0.005	**−1.0**	µA (Max)
$V_{OUT(1)}$	Logical “1” Output Voltage	V^+ = 4.75V I_{OUT} = −360 µA		**2.4**	V (Min)
		V^+ = 4.75V I_{OUT} = −10 µA		**4.5**	V (Min)
$V_{OUT(0)}$	Logical “0” Output Voltage	V^+ = 4.75V I_{OUT} = 1.6 mA		**0.4**	V (Max)
I_{OUT}	TRI-STATE Output Current	V_{OUT} = 5V V_{OUT} = 0V	0.1 −0.1	**50** **−50**	µA (Max) µA (Max)
DI_{CC}	DV_{CC} Supply Current	CS = WR = $\overline{RD}$ = 0	0.1	**2**	mA (Max)
AI_{CC}	AV_{CC} Supply Current	CS = WR = $\overline{RD}$ = 0	30	**45**	mA (Max)

(1) Typicals are at 25°C and represent most likely parametric norm.
(2) Limits are specified to AOQL (Average Outgoing Quality Level).

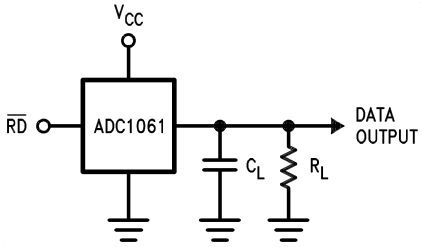
AC ELECTRICAL CHARACTERISTICS

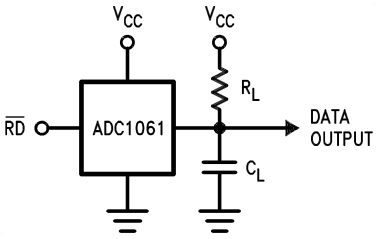
The following specifications apply for V^+ = +5V, $t_r = t_f$ = 20 ns, $V_{REF(+)}$ = 5V, and $V_{REF(-)}$ = GND unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

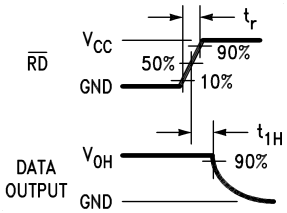
Symbol	Parameter	Conditions	Typical (1)	Limit (2)	Units (Limits)
t_{CONV}	Conversion Time from Rising Edge of $\overline{S}$ /H to Falling Edge of $\overline{INT}$	Mode 1	1.2	**1.8**	µs (Max)
t_{CRD}	Conversion Time for MODE 2 (RD Mode)	Mode 2	1.8	**2.4**	µs (Max)
t_{ACC1}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	Mode 1; C_L = 100 pF	20	**50**	ns (Max)
t_{ACC2}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	Mode 2; C_L = 100 pF		**t_{CRD} + 50**	ns (Max)
t_{SH}	Minimum Sample Time	(Figure 2); See (3)		**250**	ns (Max)
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to High-Z State)	R_L = 1k, C_L = 10 pF	20	**50**	ns (Max)
t_{INTH}	Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$		10	**50**	ns (Max)
t_{ID}	Delay from $\overline{INT}$ to Output Valid	C_L = 100 pF	20	**50**	ns (Max)
t_P	Delay from End of Conversion to Next Conversion		10	**20**	ns (Max)
SR	Slew Rate for Correct Track-and-Hold Operation		2.5		V/µs
C_{VIN}	Analog Input Capacitance		35		pF
C_{OUT}	Logic Output Capacitance		5		pF
C_{IN}	Logic Input Capacitance		5		pF

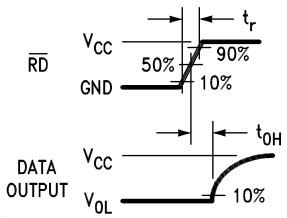
(1) Typicals are at 25°C and represent most likely parametric norm.
(2) Limits are specified to AOQL (Average Outgoing Quality Level).
(3) Accuracy may degrade if t_{SH} is shorter than the value specified.

TRI-STATE Test Circuits and Waveforms









Timing Diagrams

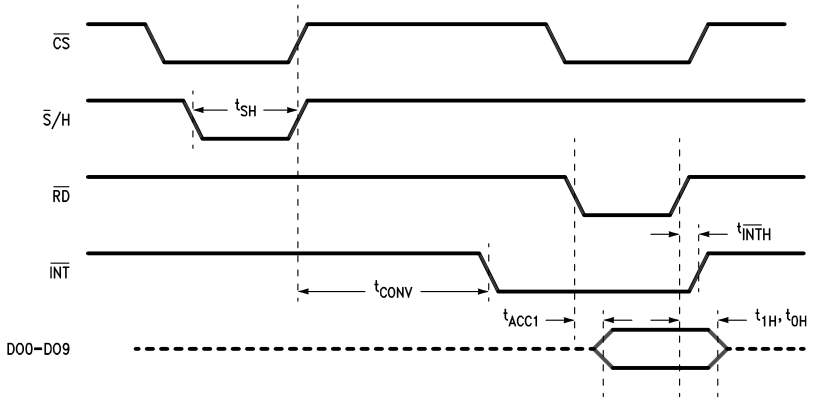


Figure 2. Mode 1. The conversion time (t_{CONV}) is determined by the internal timer.

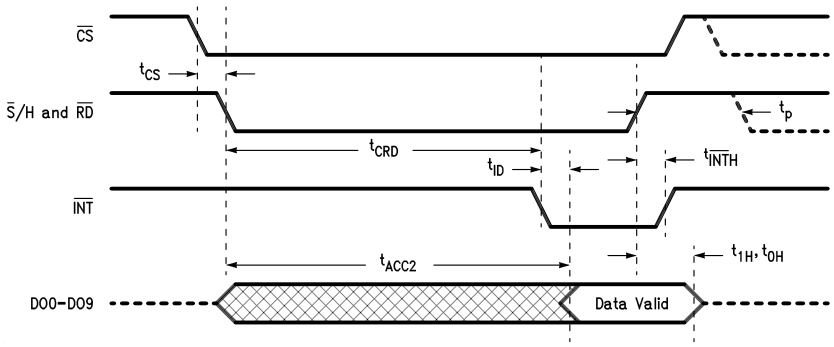


Figure 3. Mode 2 (RD Mode). The conversion time (t_{CRD}) includes the sampling time, and is determined by the internal timer.

TYPICAL PERFORMANCE CHARACTERISTICS

Zero (Offset) Error vs. Reference Voltage

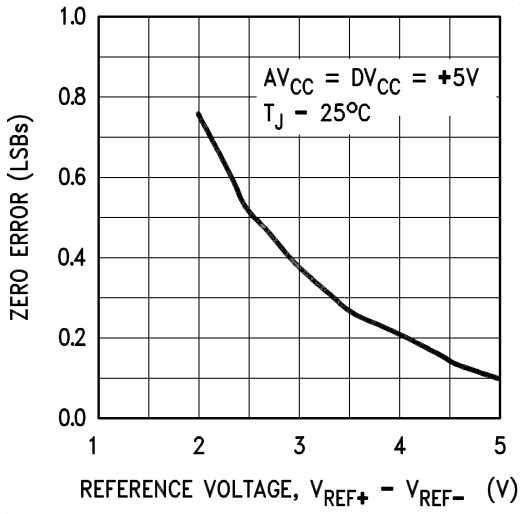


Figure 4.

Linearity Error vs. Reference Voltage

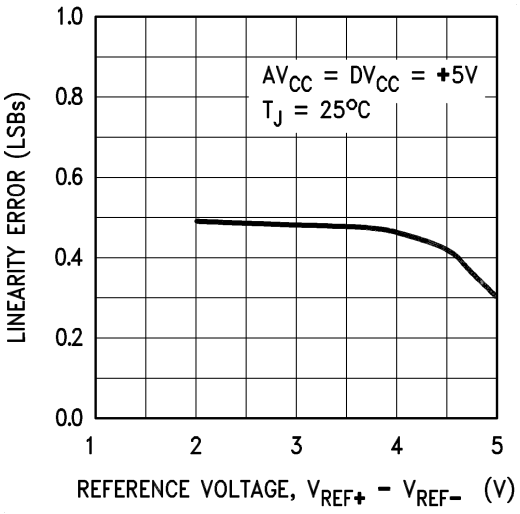


Figure 5.

Mode 1 Conversion Time vs. Temperature

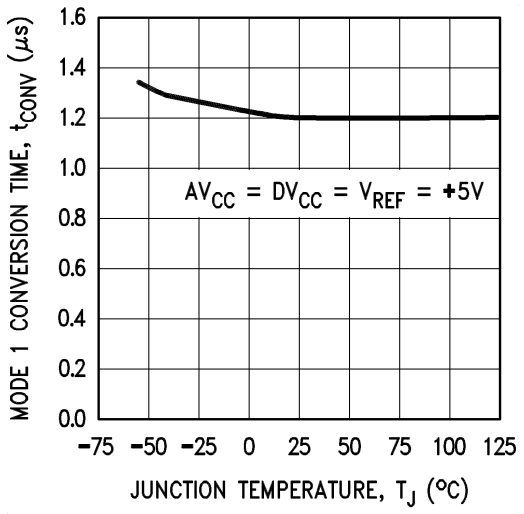


Figure 6.

Mode 2 Conversion Time vs. Temperature

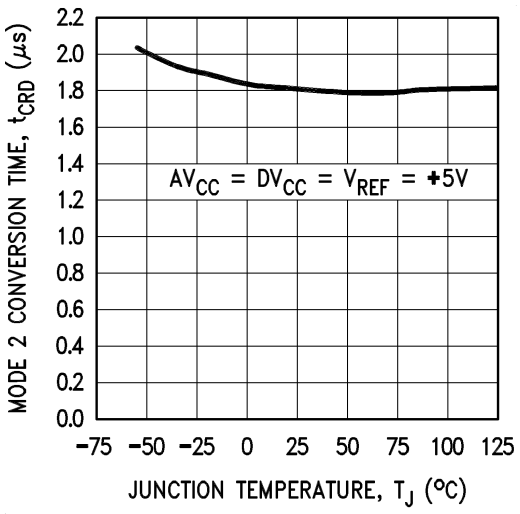


Figure 7.

FUNCTIONAL DESCRIPTION

The ADC1061 digitizes an analog input signal to 10 bits accuracy by performing two lower-resolution “flash” conversions. The first flash conversion provides the six most significant bits (MSBs) of data, and the second flash conversion provides the four least significant bits (LSBs).

Figure 8 is a simplified block diagram of the converter. Near the center of the diagram is a string of resistors. At the bottom of the string of resistors are 16 resistors, each of which has a value 1/1024th the resistance of the whole resistor string. These lower 16 resistors (the **LSB Ladder**) therefore have a voltage drop of 16/1024, or 1/64th of the total reference voltage ($V_{REF+} - V_{REF-}$) across them. The remainder of the resistor string is made up of eight groups of eight resistors connected in series. These comprise the **MSB Ladder**. Each section of the MSB Ladder has 1/8th of the total reference voltage across it, and each of the MSB resistors has 1/64th of the total reference voltage across it. Tap points across all of these resistors can be connected, in groups, to the sixteen comparators at the right of the diagram.

On the left side of the diagram is a string of seven resistors connected between $V_{REF+} - V_{REF-}$. Six comparators compare the input voltage with the tap voltages on the resistor string to provide an estimate of the input voltage. This estimate is then used to control the multiplexer that connects the MSB Ladder to the sixteen comparators on the right. Note that the comparators on the left needn't be very accurate; they simply provide an estimate of the input voltage. Only the sixteen comparators on the right and the six on the left are necessary to perform the initial six-bit flash conversion, instead of the 64 comparators that would be required using conventional half-flash methods.

To perform a conversion, the estimator compares the input voltage with the tap voltages on the seven resistors on the left. The estimator decoder then determines which MSB Ladder tap points will be connected to the sixteen comparators on the right. For example, assume that the estimator determines that V_{IN} is between 11/16 and 13/16 of V_{REF}. The estimator decoder will instruct the comparator mux to connect the 16 comparators to the taps on the MSB Ladder between 10/16 and 14/16 of V_{REF}. The 16 comparators will then perform the first flash conversion. Note that since the comparators are connected to Ladder voltages that extend beyond the range indicated by the estimator circuit, errors in the estimator as large as 1/16 of the reference voltage (64 LSBs) will be corrected. This first flash conversion produces the six most significant bits of data.

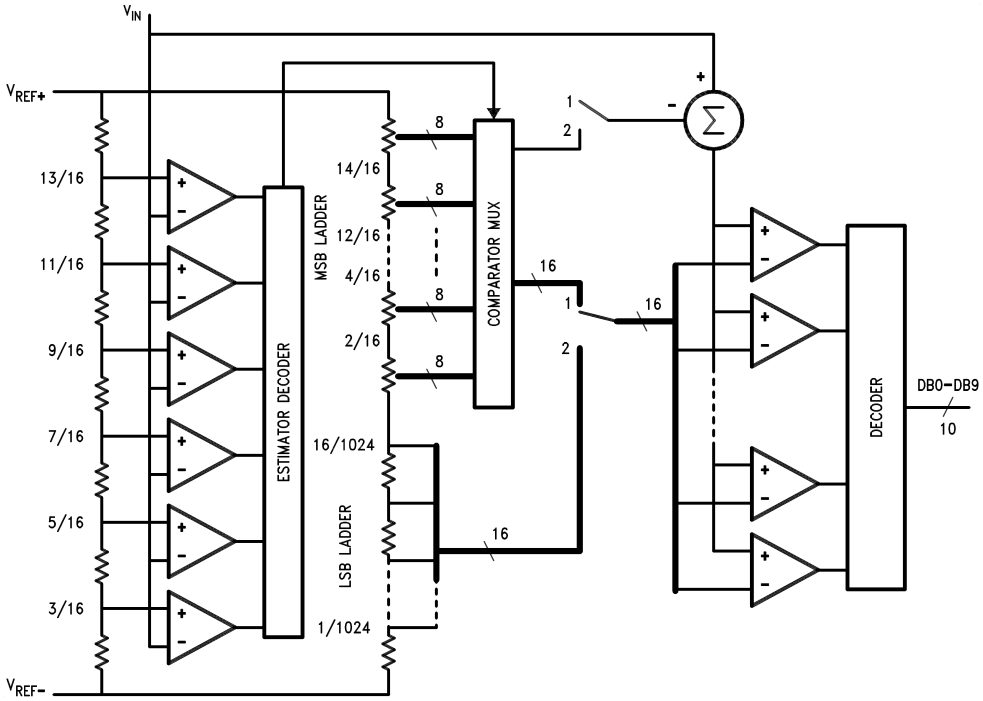


Figure 8. Block Diagram of the Modified Half-Flash Converter Architecture

The remaining four LSBs may now be determined using the same sixteen comparators that were used for the first flash conversion. The MSB Ladder tap voltage just below the input voltage (as determined by the first flash) is subtracted from the input voltage and compared with the tap points on the sixteen LSB Ladder resistors. The result of this second flash conversion is then decoded, and the full 10-bit result is latched.

Note that the sixteen comparators used in the first flash conversion are reused for the second flash. Thus, the half-flash conversion techniques used in the ADC1061 needs only a small fraction of the number of comparators that would be required for a traditional flash converter, and far fewer than would be used in a conventional half-flash approach. This allows the ADC1061 to perform high-speed conversions without excessive power drain.

APPLICATIONS INFORMATION

Modes of Operation

The ADC1061 has two basic digital interface modes. These are illustrated in Figure 2 and Figure 3.

MODE 1

In this mode, the $\overline{S}$ /H pin controls the start of conversion. $\overline{S}$ /H is pulled low for a minimum of 250 ns. This causes the comparators in the "coarse" flash converter to become active. When $\overline{S}$ /H goes high, the result of the coarse conversion is latched and the "fine" conversion begins. After approximately 1.2 µs (1.8 µs maximum), $\overline{INT}$ goes low, indicating that the conversion results are latched and can be read by pulling $\overline{RD}$ low. Note that $\overline{CS}$ must be low to enable $\overline{S}$ /H or $\overline{RD}$. $\overline{CS}$ is internally "ANDed" with the sample and read control signals; the input voltage is sampled when $\overline{CS}$ and $\overline{S}$ /H are low, and is read when $\overline{CS}$ and $\overline{RD}$ are low.

MODE 2

In Mode 2, also called "RD mode", the $\overline{S}$ /H and $\overline{RD}$ pins are tied together. A conversion is initiated by pulling both pins low. The ADC1061 samples the input voltage and causes the coarse comparators to become active. An internal timer then terminates the coarse conversion and begins the fine conversion.

About 1.8 µs (2.4 µs maximum) after $\overline{S}$ /H and $\overline{RD}$ are pulled low, $\overline{INT}$ goes low, indicating that the conversion is complete. Approximately 20 ns later the data appearing on the TRI-STATE output pins will be valid. Note that data will appear on these pins throughout the conversion, but will be valid only after $\overline{INT}$ goes low.

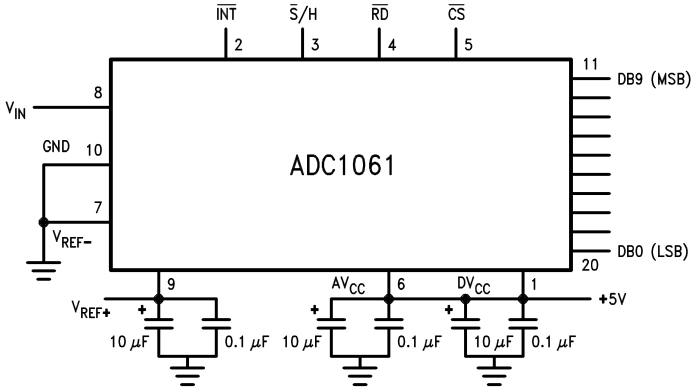


Figure 9. Typical connection. Note the multiple bypass capacitors on the reference and power supply pins. If $V_{REF}-$ is not grounded, it should also be bypassed to ground using multiple capacitors (see 5.0 "Power Supply Considerations").

Reference Considerations

The ADC1061 has two reference inputs. These inputs, V_{REF+} and V_{REF-}, are fully differential and define the zero to full-scale range of the input signal. The reference inputs can be connected to span the entire supply voltage range (V_{REF-} = 0V, V_{REF+} = V_{CC}) for ratiometric applications, or they can be connected to different voltages (as long as they are between ground and V_{CC}) when other input spans are required. Reducing the overall V_{REF} span to less than 5V increases the sensitivity of the converter (e.g., if V_{REF} = 2V, then 1LSB = 1.953 mV). Note, however, that linearity and offset errors become larger when lower reference voltages are used. See the Typical Performance Curves for more information. Reference voltages less than 2V are not recommended.

In most applications, V_{REF-} will simply be connected to ground, but it is often useful to have an input span that is offset from ground. This situation is easily accommodated by the reference configuration used in the ADC1061. V_{REF-} can be connected to a voltage other than ground as long as the reference for this pin is capable of sinking current. If V_{REF-} is connected to a voltage other than ground, bypass it with multiple capacitors.

Since the resistance between the two reference inputs can be as low as 400Ω, the voltage source driving the reference inputs should have low output impedance. Any noise on either reference input is a potential cause of conversion errors, so each of these pins must be supplied with a clean, low noise voltage source. Each reference pin should normally be bypassed with a 10 µF tantalum and a 0.1 µF ceramic capacitor. More bypassing may be necessary in some systems.

The choice of reference voltage source will depend on the requirements of the system. In ratiometric data acquisition systems with a power supply-referenced sensor, the reference inputs are normally connected to V_{CC} and GND, and no reference other than the power supply is necessary. In absolute measurement systems requiring 10-bit accuracy, a reference with better than 0.1% accuracy will be necessary.

The Analog Input

The ADC1061 samples the analog input voltage once every conversion cycle. When this happens, the input is briefly connected to an impedance approximately equal to 600Ω in series with 35 pF. Short-duration current spikes can therefore be observed at the analog input during normal operation. These spikes are normal and do not degrade the convertor's performance.

Note that large source impedances can slow the charging of the sampling capacitors and degrade conversion accuracy. Therefore, only signal sources with output impedances less than 500Ω should be used if rated accuracy is to be achieved at the minimum sample time. If the sampling time is increased, the source impedance can be larger. If a signal source has a high output impedance, its output should be buffered with an operational amplifier. The operational amplifier's output should be well-behaved when driving a switched 35 pF/600Ω load. Any ringing or voltage shifts at the op amp's output during the sampling period can result in conversion errors.

Correct conversion results will be obtained for input voltages greater than GND − 50 mV and less than V^+ + 50 mV. Do not allow the signal source to drive the analog input pin more than 300 mV higher than AV_{CC} and DV_{CC}, or more than 300 mV lower than GND. If the analog input pin is forced beyond these voltages, the current flowing through the pin should be limited to 5 mA or less to avoid permanent damage to the ADC1061.

Inherent Sample-and-Hold

Because the ADC1061 samples the input signal once during each conversion, it is capable of measuring relatively fast input signals without the help of an external sample-hold. In a conventional successive-approximation A/D converter, regardless of speed, the input signal must be stable

to better than ±½ LSB during each conversion cycle or significant errors will result. Consequently, even for many relatively slow input signals, the signals must be externally sampled and held constant during each conversion.

The ADC1061 can perform accurate conversions of input signals at frequencies from DC to greater than 160 kHz without the need for external sampling circuitry.

Power Supply Considerations

The ADC1061 is designed to operate from a +5V (nominal) power supply. There are two supply pins, AV_{CC} and DV_{CC}. These pins allow separate external bypass capacitors for the analog and digital portions of the circuit. To ensure accurate conversions, the two supply pins should be connected to the same voltage source, and each should be bypassed with a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor. Depending on the circuit board layout and other system considerations, more bypassing may be necessary.

It is important to ensure that none of the ADC1061's input or output pins are ever driven to a voltage more than 300 mV above AV_{CC} and DV_{CC}, or more than 300 mV below GND. If these voltage limits are exceeded, the overdrive current into or out of any pin on the ADC1061 must be limited to less than 5 mA, and no more than 20 mA of overdrive current (all overdriven pins combined) should flow. In systems with multiple power supplies, this may require careful attention to power supply sequencing. The ADC1061's power supply pins should be at the proper voltage before signals are applied to any of the other pins.

Layout and Grounding

In order to ensure fast, accurate conversions from the ADC1061, it is necessary to use appropriate circuit board layout techniques. The analog ground return path should be low-impedance and free of noise from other parts of the system. Noise from digital circuitry can be especially troublesome, so digital grounds should always be separate from analog grounds. For best performance, separate ground planes should be provided for the digital and analog parts of the system.

All bypass capacitors should be located as close to the converter as possible and should connect to the converter and to ground with short traces. The analog input should be isolated from noisy signal traces to avoid having spurious signals couple to the input. Any external component (e.g., a filter capacitor) connected across the converter's input should be connected to a very clean ground return point. Grounding the component at the wrong point will result in reduced conversion accuracy.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	11

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