DS04–21311–2aE

FUJITSU

DATA SHEET

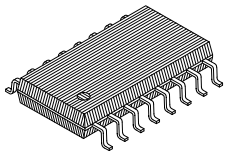
MB1518

Serial Input PLL Frequency Synthesizer With On–Chip 2.5GHz Prescaler

The Fujitsu MB1518 with an on chip 2.5 GHz dual modulus prescaler is a serial input PLL (Phase Locked Loop) frequency synthesizer with pulse swallow function. It is well suited for BS tuner, CATV system applications.

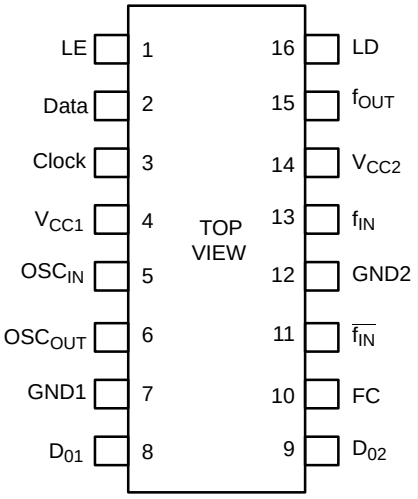
It operates supply voltage of 5.0V typ. and dissipates 16mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

- Power supply voltage: V_{CC} = 4.5 to 5.5V
- High operating frequency: f_{in} = 2.5GHz (P_{in} = –4dBm)
- 2.5GHz dual modulus prescaler: P = 512/528
- Low power supply current: I_{CC} = 16mA typ.
- Programmable reference divider : R = 512
- Programmable divider consisting of:
  Binary 5–bit swallow counter (A = 0 to 31)
  Binary 9-bit programmable counter (N = 32 to 511)
- Wide operating temperature: T_a = –40 to +85°C
- Plastic 16-pin flat package (Suffix: –PF)



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



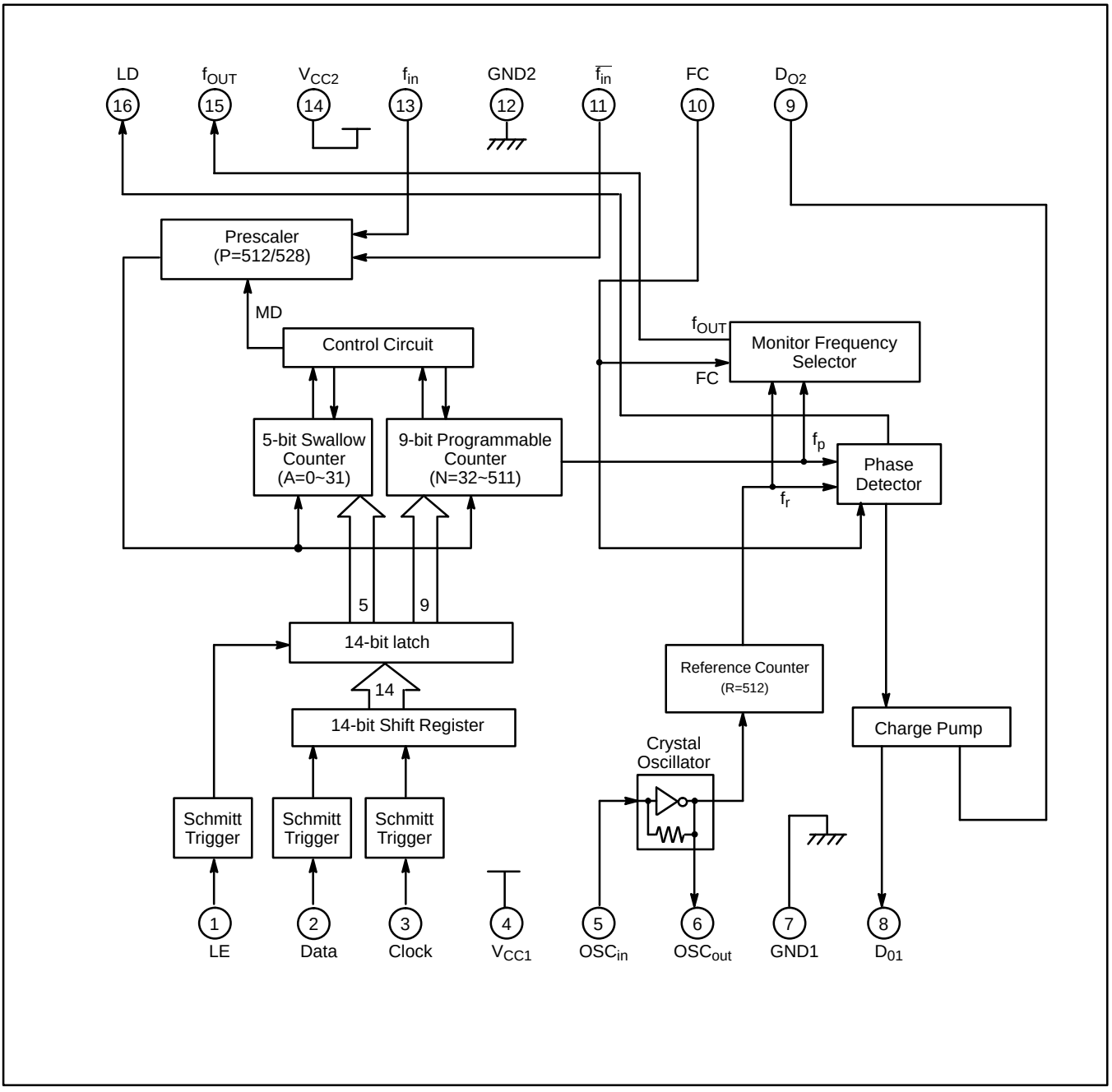
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 7.0	V
Output Voltage	V_O	0.5 to V_{CC} +0.5	V
Output Current	I_O	±10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Descriptions
1	LE	I	Load enable input pin. This pin involves a schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch.
2	Data	I	Serial data of binary code input pin. This pin involves a schmitt trigger circuit.
3	Clock	I	Clock input pin of the 14–bit shift register. This pin involves a schmitt trigger circuit. On rising edge of the clock shifts one bit of the data into the shift register.
4	V_{CC1}	–	PLL power supply voltage input pin.
5 6	OSC_{IN} OSC_{OUT}	I O	Oscillator input pin. Oscillator output pin. A crystal is connected between OSC_{IN} pin and OSC_{OUT} pin.
7	GND1	–	PLL ground pin.
8 9	D_{O1} D_{O2}	O O	Charge pump output pins. Phase characteristics can be reversed depending upon FC pin input level.
10	FC	I	Phase select input pin of the phase detector. This pin involves an internal pull up resistor. When this pin is low, characteristics of the charge pump and phase detector can be reversed. This input also selects f_{OUT} pin output level, either fr or fp. Please see on page 6.
11	$\overline{f_{in}}$	I	Complementary input pin of f_{in}. Please connect to GND through a capacitor.
12	GND2	–	Prescaler ground pin.
13	f_{in}	I	Prescaler input pin, This signal is input with AC coupled.
14	V_{CC2}	–	Prescaler power supply voltage input pin.
15	f_{OUT}	O	Monitor pin of the phase detector input. f_{OUT} pin outputs either of the programmable reference divider output frequency fr or programmable divider output frequency fp depending upon the FC pin input level. FC pin: H → fout output signal: fr FC pin: L → fout output signal: fp
16	LD	O	Phase detector output pin. Normally this pin outputs high. While the phase difference between fr and fp exists, this pin outputs low.

FUNCTIONAL DESCRIPTIONS

DIVIDE RATIO SETTING

Divide ratio can be set using the following equation:

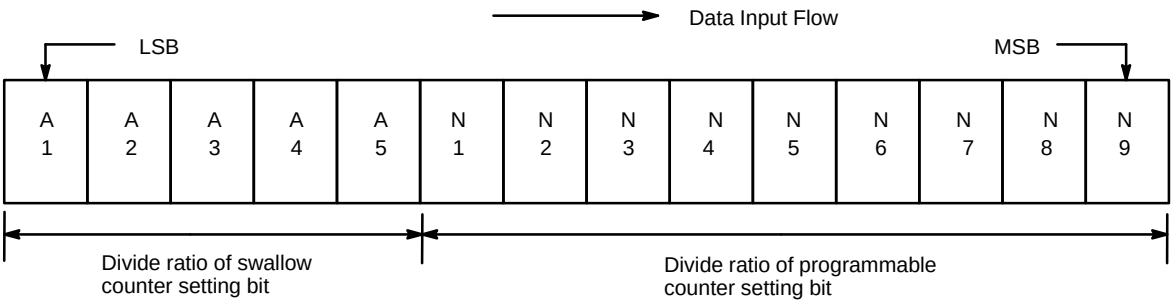
$f_{VCO} = \{(P \times N) + (16 \times A)\} \times f_{OSC} \div R$

f_{VCO}: Output frequency of an external voltage controlled oscillator (VCO)
P: Preset divide ratio of an internal dual modulus prescaler (512)
N: Preset divide ratio of binary 9-bit programmable counter (32 to 511)
A: Preset divide ratio of binary 5-bit swallow counter (0 to 31)
f_{OSC}: Reference oscillator frequency
R: Preset divide ratio of reference counter (512)

SERIAL DATA I NPUT

On rising edge of the clock shifts one bit of the data into the shift register.
When the load enable is high, the data stored in the shift register is transferred to the latch.

14 bit of serial data formit is shown below.



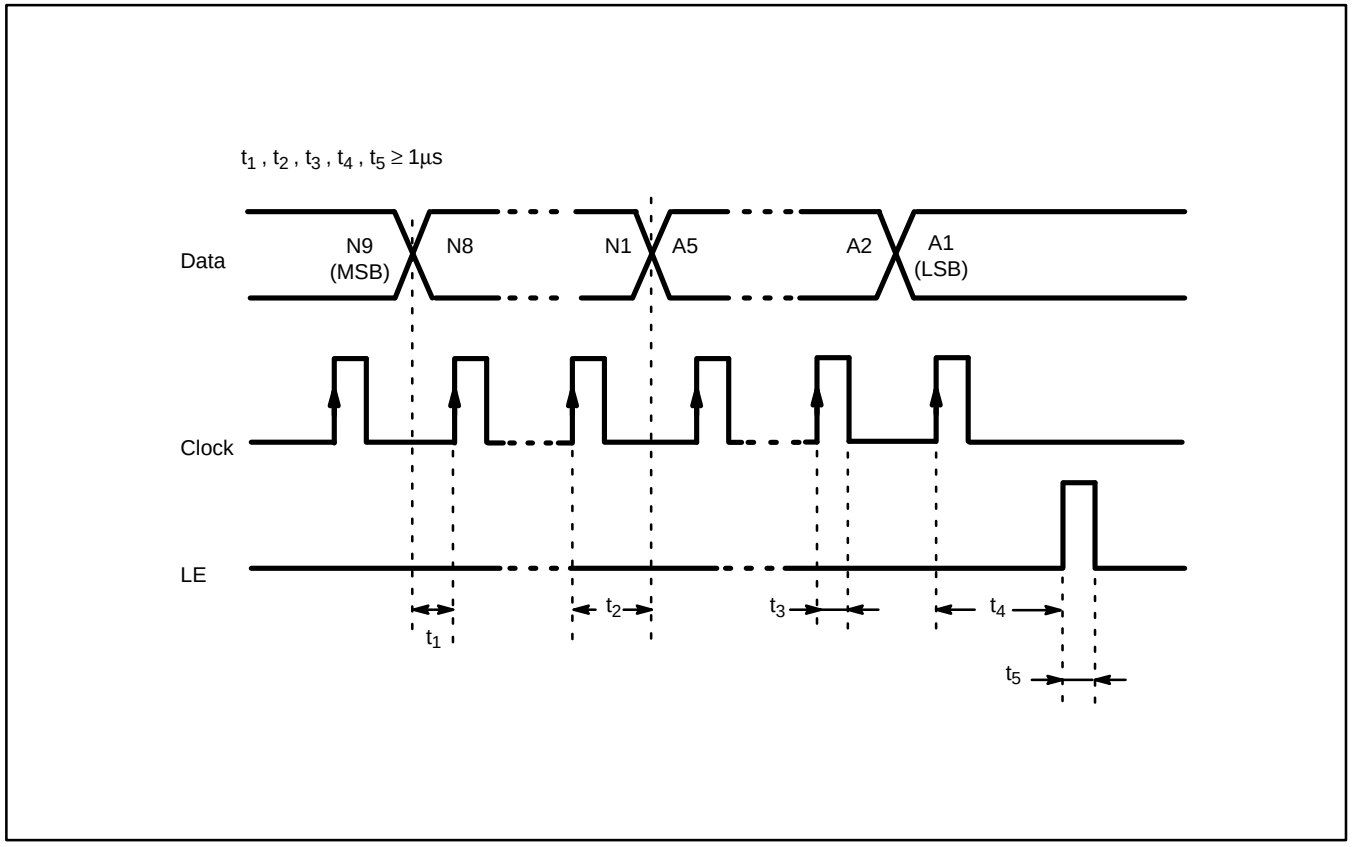
5-bit swallow counter divide ratio (A1 to A5)

Divide ratio A	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
:	:	:	:	:	:
31	1	1	1	1	1

9-bit programmable counter divide ratio (N1 to N9)

Divide ratio	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
32	0	0	0	1	0	0	0	0	0
33	0	0	0	1	0	0	0	0	1
34	0	0	0	1	0	0	0	1	0
:	:	:	:	:	:	:	:	:	:
511	1	1	1	1	1	1	1	1	1

SERIAL DATA INPUT TIMING



Note: On rising edge of the clock shifts one bit of the data into the shift register.
When LE is high, the data stored the shift register is transferred into the latch.

PHASE DETECTOR CHARACTERISTICS

FC pin selects the phase of the phase detector. Phase characteristics (chage pump output) can be reversed depending upon the FC pin input level. Monitor pin (fout) output level is selected by the FC pin input level as well.

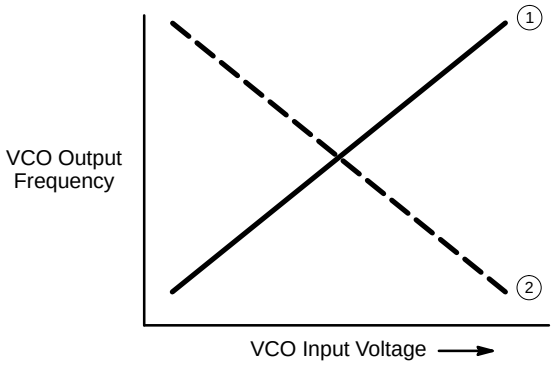
	FC = H (or open)		FC = L	
	D_{01} , D_{02}	fout	D_{01} , D_{02}	fout
fr > fp	H	Outputs programmable reference divider output frequency fr.	L	Outputs programmable divider output frequency fp.
fr = fp	Z		Z	
fr < fp	L		H	

Note:
Z: High-impedance

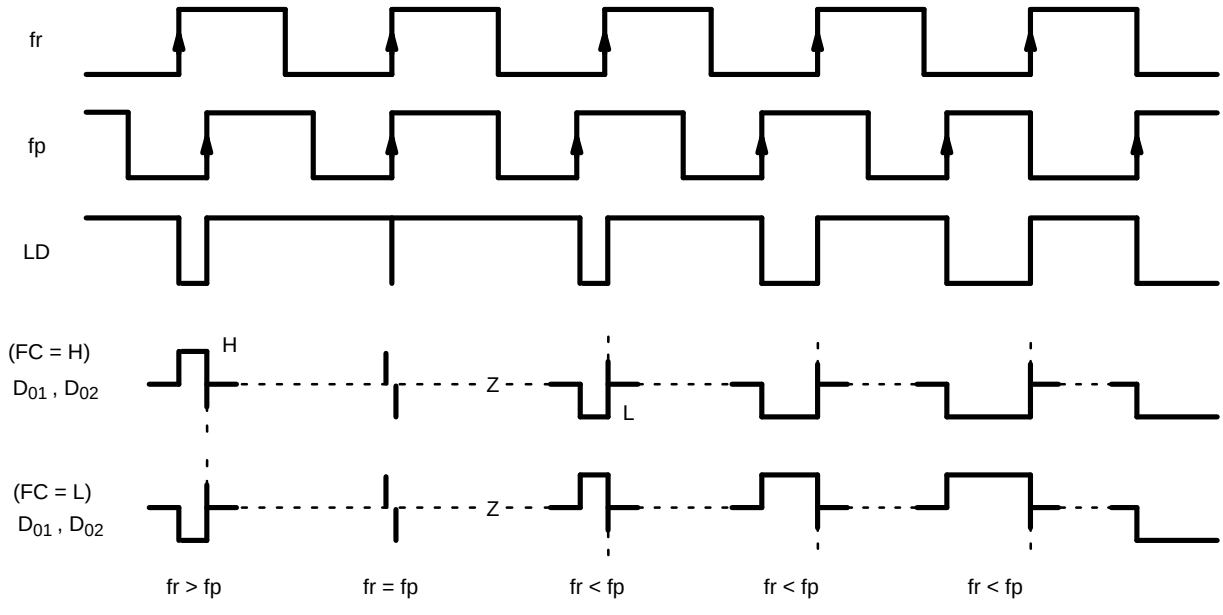
Depending upon the VCO polarity, FC pin should be set accordingly.

When VCO polarity is like 1,
FC should be set high or open.
When VCO polarity is like 2,
FC should be set low.

VCO POLARITY



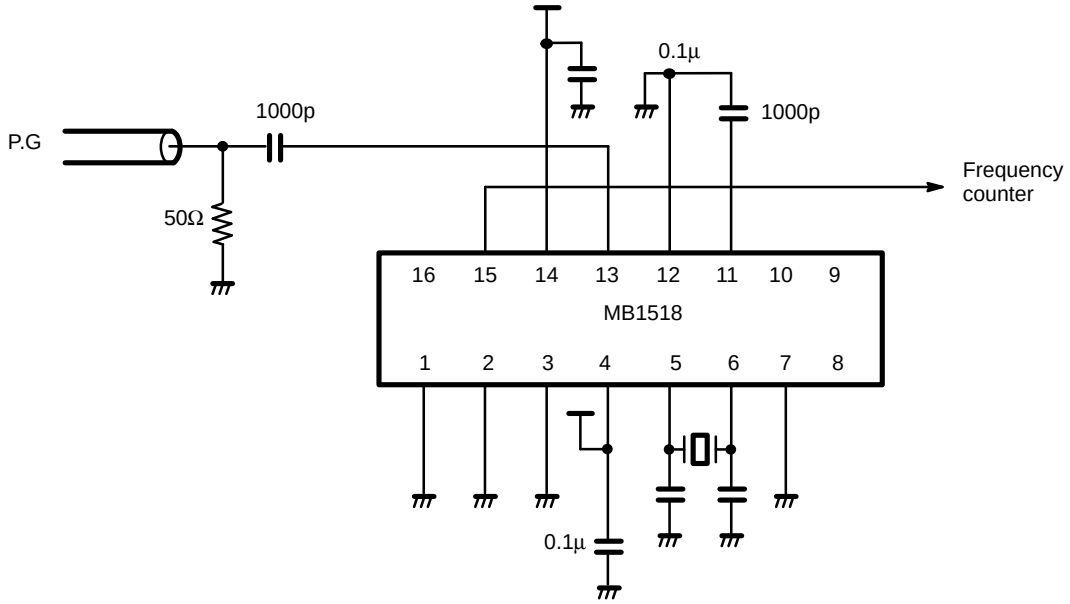
PHASE DETECTOR WAVEFORM



Note: Phase difference detection range : -2π to $+2\pi$

Spike shape depends on the charge pump characteristics.
The spike is output to diminish the dead band.

TEST CIRCUIT (FOR PRESCALER INPUT SENSITIVITY)



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_I	GND	–	V_{CC}	V
Operating Temperature	T_a	–40	–	+85	°C

HANDLING PRECAUTIONS

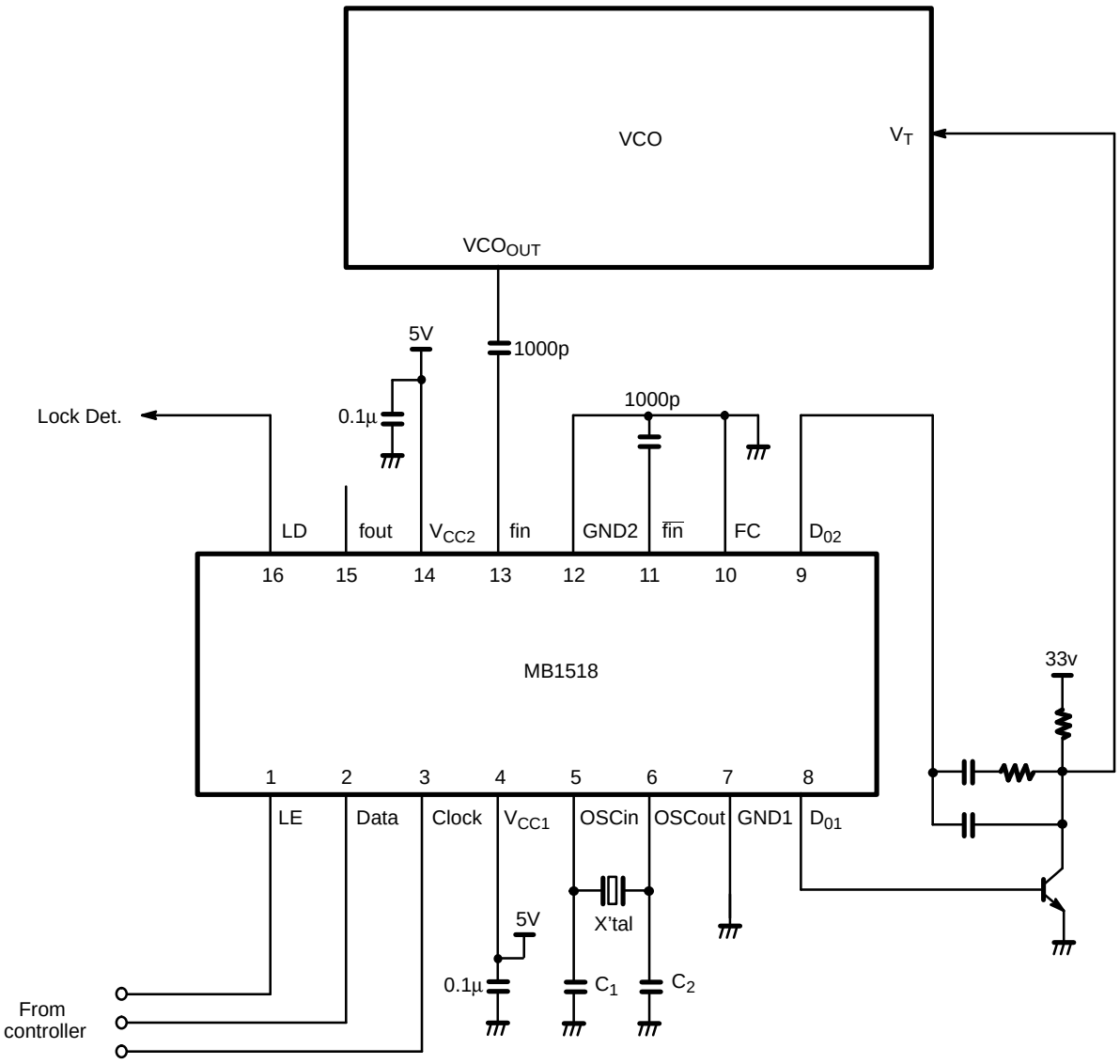
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC}	Note1	–	16.0	–	mA
Operating Frequency	f_{in}	f_{in}	Note2	10	–	2500	MHz
	OSC_{IN}	f_{OSC}	–	–	4	10	
Input Sensitivity	f_{in}	Pfin	2300 to 2500MHz	–4	–	6	dBm
			1900 to 2300MHz	–7	–	6	
			10 to 1900MHz	–10	–	6	
	OSC_{IN}	V_{OSC}	–	0.5	–	–	V_{PP}
High–level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}	–	V_{CC}x0.7+0.4	–	–	V
Low-level Input Voltage		V_{IL}	–	–	–	V_{CC}x0.3–0.4	
High–level Input Current	Data, Clock, LE	I_{IH}	–	–	1.0	–	µA
Low-level Input Current		I_{IL}	–	–	–1.0	–	
	FC	I_{ILFC}	–	–	–60	–	
Input Current	OSC_{IN}	I_{IOSC}	–	–	±50	–	
High–level Output Voltage	Except D_O	V_{OH}	V_{CC} = 5.0V	4.4	–	–	V
Low-level Output Voltage		V_{OL}	–	–	–	0.4	
High–impedance Cutoff Current	D_{01},D_{02}	I_{OFF}	–	–	–	1.1	µA
High-level Output Current	Except D_O	I_{OH}	–	–1.0	–	–	mA
Low-level Output Current		I_{OL}	–	1.0	–	–	

Note1: f_{in}=2.5GHz, OSC_{IN}=4.0MHz, V_{cc}=5.0V. Input pins are grounded and output pins are open.
Note2: AC coupling. Minimum operating frequency is measured with a capacitor 1000pF.

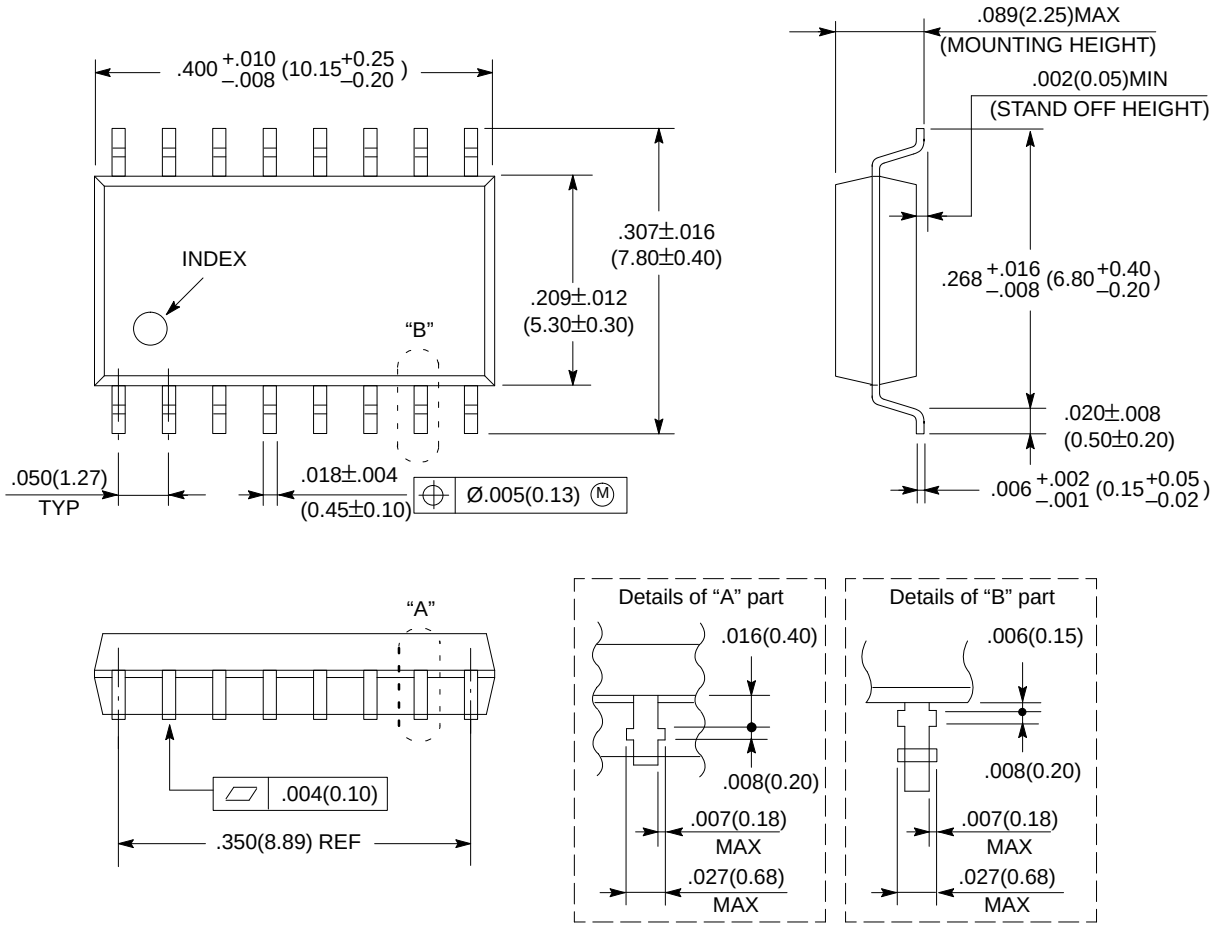
MB1518 APPLICATION CIRCUIT



C_1, C_2 : depends on the crystal oscillator.
FC : with internal pull up resistor.

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



Dimensions in
inches (millimeters)

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