

- **1.4-k Ω Pullup Resistors Integrated on All Open-Drain Outputs Eliminate the Need for Discrete Resistors**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Designed for the IEEE Std 1284-I (Level 1 Type) and IEEE Std 1284-II (Level 2 Type) Electrical Specifications**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin-Shrink Small-Outline (DGG) Packages**

description/ordering information

The SN74LVC161284 is designed for 3-V to 3.6-V V_{CC} operation. This device provides asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

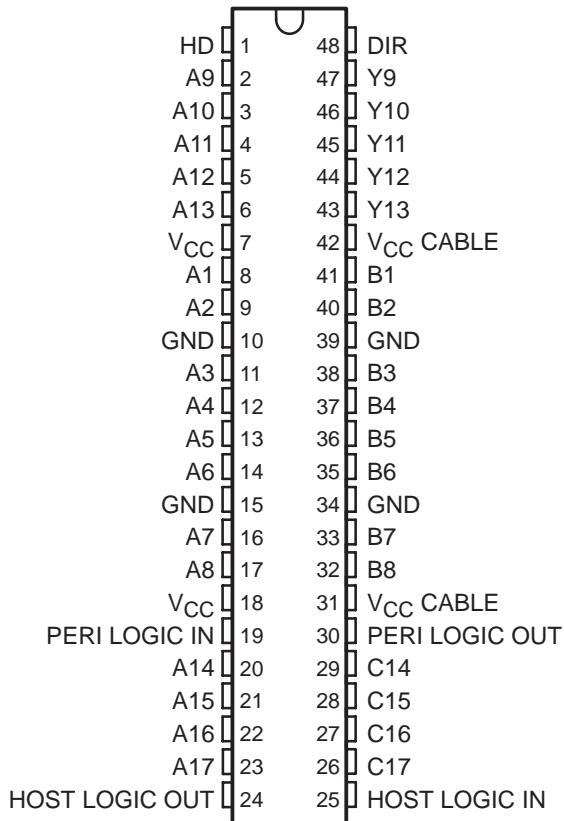
This device has eight bidirectional bits; data can flow in the A-to-B direction when DIR is high and in the B-to-A direction when DIR is low. This device also has five drivers, which drive the cable side, and four receivers. The SN74LVC161284 has one receiver dedicated to the HOST LOGIC line and a driver to drive the PERI LOGIC line.

The output drive mode is determined by the high-drive (HD) control pin. When HD is high, the outputs are in a totem-pole configuration, and in an open-drain configuration when HD is low. This meets the drive requirements as specified in the IEEE Std 1284-I (level 1 type) and IEEE Std 1284-II (level 2 type) parallel peripheral-interface specifications. Except for HOST LOGIC IN and PERI LOGIC OUT, all cable-side pins have a 1.4-k Ω integrated pullup resistor. The pullup resistor is switched off if the associated output driver is in the low state or if the output voltage is above V_{CC} CABLE. If V_{CC} CABLE is off, PERI LOGIC OUT is set to low.

The device has two supply voltages. V_{CC} is designed for 3-V to 3.6-V operation. V_{CC} CABLE supplies the inputs and output buffers of the cable side only and is designed for 3-V to 3.6-V and for 4.7-V to 5.5-V operation. Even when V_{CC} CABLE is 3 V to 3.6 V, the cable-side I/O pins are 5-V tolerant.

The SN74LVC161284 is characterized for operation from 0°C to 70°C.

DGG OR DL PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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description/ordering information (continued)

ORDERING INFORMATION

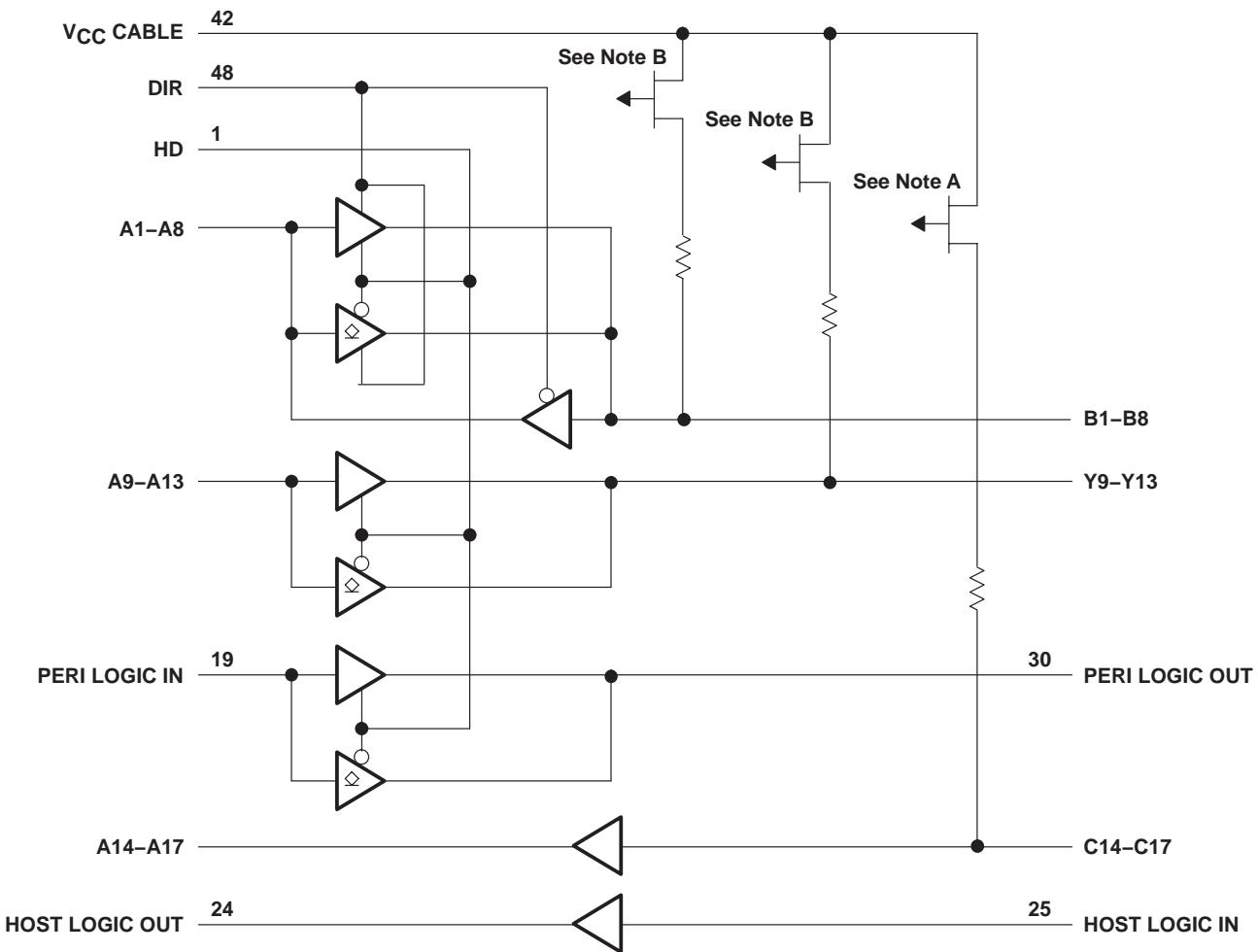
| TA | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|-------------|-------------|---------------|-----------------------|------------------|
| 0°C to 70°C | TSSOP – DGG | Tape and reel | SN74LVC161284DGGR | PACKAGE PREVIEW |
| | SSOP – DL | Tape | SN74LVC161284DL | LVC161284 |
| | | Tape and reel | SN74LVC161284DLR | |
| | TSSOP – DGG | Tape and reel | 74LVC161284DGGRG4 | PACKAGE PREVIEW |
| | SSOP – DL | Tape | 74LVC161284DLRE4 | LVC161284 |
| | | Tape and reel | 74LVC161284DLRG4 | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

| INPUTS | | OUTPUT | MODE |
|--------|----|------------|---|
| DIR | HD | | |
| L | L | Open drain | A9–A13 to Y9–Y13 and PERI LOGIC IN to PERI LOGIC OUT |
| | | Totem pole | B1–B8 to A1–A8 and C14–C17 to A14–A17 |
| L | H | Totem pole | B1–B8 to A1–A8, A9–A13 to Y9–Y13, PERI LOGIC IN to PERI LOGIC OUT, and C14–C17 to A14–A17 |
| H | L | Open drain | A1–A8 to B1–B8, A9–A13 to Y9–Y13, and PERI LOGIC IN to PERI LOGIC OUT |
| | | Totem pole | C14–C17 to A14–A17 |
| H | H | Totem pole | A1–A8 to B1–B8, A9–A13 to Y9–Y13, C14–C17 to A14–A17, and PERI LOGIC IN to PERI LOGIC OUT |

logic diagram



NOTES: A. The PMOS transistor prevents backdriving current from the signal pins to VCC CABLE when VCC CABLE is open or at GND.
B. The PMOS transistors prevent backdriving current from the signal pins to VCC CABLE when VCC CABLE is open or at GND. The PMOS transistor is turned off when the associated driver is in the low state.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | | |
|--|-------|----------------------------|
| Supply voltage range: V_{CC} CABLE | | -0.5 V to 7 V |
| V_{CC} | | -0.5 V to 4.6 V |
| Input and output voltage range, V_I and V_O : Cable side (see Notes 1 and 2) | | -2 V to 7 V |
| Peripheral side (see Note 1) | | -0.5 V to V_{CC} + 0.5 V |
| Input clamp current, I_{IK} ($V_I < 0$) | | -20 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | | -50 mA |
| Continuous output current, I_O : Except PERI LOGIC OUT | | ±50 mA |
| PERI LOGIC OUT | | ±100 mA |
| Continuous current through each V_{CC} or GND | | ±200 mA |
| Output high sink current, I_{SK} ($V_O = 5.5$ V and V_{CC} CABLE = 3 V) | | 65 mA |
| Package thermal impedance, θ_{JA} (see Note 3): DGG package | | 89°C/W |
| DL package | | 94°C/W |
| Storage temperature range, T_{stg} | | -65°C to 150°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The ac input voltage pulse duration is limited to 40 ns if the amplitude is greater than -0.5 V.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

| | | MIN | MAX | UNIT |
|----------------|---|--------|----------|------|
| V_{CC} CABLE | Supply voltage for the cable side, V_{CC} CABLE $\geq V_{CC}$ | 3 | 5.5 | V |
| V_{CC} | Supply voltage | 3 | 3.6 | V |
| V_{IH} | A, B, DIR, and HD | 2 | | V |
| | C14–C17 | 2.3 | | |
| | HOST LOGIC IN | 2.6 | | |
| | PERI LOGIC IN | 2 | | |
| V_{IL} | A, B, DIR, and HD | 0.8 | | V |
| | C14–C17 | 0.8 | | |
| | HOST LOGIC IN | 1.6 | | |
| | PERI LOGIC IN | 0.8 | | |
| V_I | Peripheral side | 0 | V_{CC} | V |
| | Cable side | 0 | 5.5 | |
| V_O | Open-drain output voltage | HD low | 0 | 5.5 |
| I_{OH} | HD high, B and Y outputs | -14 | | mA |
| | A outputs and HOST LOGIC OUT | -4 | | |
| | PERI LOGIC OUT | -0.5 | | |
| I_{OL} | B and Y outputs | 14 | | mA |
| | A outputs and HOST LOGIC OUT | 4 | | |
| | PERI LOGIC OUT | 84 | | |
| T_A | Operating free-air temperature | 0 | 70 | °C |

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range,
 V_{CC} CABLE = 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | TYP† | MAX | UNIT |
|--------------|--|--|----------|------|----------|------------|----------|
| ΔV_t | Input hysteresis | $V_{thH} - V_{thL}$ for all inputs except the C inputs and HOST LOGIC IN | 3.3 V | 0.4 | | | V |
| | | $V_{thH} - V_{thL}$ for the HOST LOGIC IN | 3.3 V | 0.2 | | | |
| | | $V_{thH} - V_{thL}$ for the C inputs | 3.3 V | 0.8 | | | |
| V_{OH} | HD high, B and Y outputs | $I_{OH} = -14$ mA | 3 V | 2.23 | | | V |
| | | | 3.3 V‡ | 2.4 | | | |
| | HD high, A outputs, and HOST LOGIC OUT | $I_{OH} = -4$ mA | 3 V | 2.4 | | | |
| | | $I_{OH} = -50$ μ A | 3 V | 2.8 | | | |
| | PERI LOGIC OUT | $I_{OH} = -0.5$ mA | 3.15 V | 3.1 | | | |
| | | | 3.3 V‡ | 4.5 | | | |
| V_{OL} | B and Y outputs | $I_{OL} = 14$ mA | 3 V | | 0.77 | | V |
| | | $I_{OL} = 50$ μ A | 3 V | | 0.2 | | |
| | A outputs and HOST LOGIC OUT | $I_{OL} = 4$ mA | 3 V | | 0.4 | | |
| | | $I_{OL} = 84$ mA | 3 V | | 0.8 | | |
| I_I | C inputs | $V_I = V_{CC}$ | 3.6 V§ | | 50 | μ A | mA |
| | | $V_I = GND$ (pullup resistors) | 3.6 V§ | | -3.5 | | |
| | All inputs except the B or C inputs | $V_I = V_{CC}$ or GND | 3.6 V | | ± 1 | μ A | |
| I_{OZ} | B outputs | $V_O = V_{CC}$ | 3.6 V | | 20 | μ A | mA |
| | | $V_O = GND$ (pullup resistors) | 3.6 V§ | | -3.5 | | |
| | A1–A8 | $V_O = V_{CC}$ or GND | 3.6 V | | ± 20 | μ A | |
| | Open-drain Y outputs | $V_O = GND$ (pullup resistors) | 3.6 V§ | | -3.5 | | |
| I_{off} | Leakage to GND, B and Y outputs | | 0 V | | 100 | | μ A |
| | Leakage to V_{CC} , B and Y outputs | | | | 10 | | |
| $I_{CC}¶$ | $V_I = V_{CC}$, $I_O = 0$ | | 3.6 V | | 0.8 | | mA |
| | $V_I = GND$ (12 \times pullup) | | 3.6 V | | 45 | | |
| C_i | Control inputs | $V_I = V_{CC}$ or GND | 3.3 V | 3 | 4 | pF | |
| C_{io} | All inputs | $V_O = V_{CC}$ or GND | 3.3 V | 7 | 15 | pF | |
| Z_O | Cable side | $I_{OH} = -35$ mA | 3.3 V | | 45 | | Ω |
| R pullup | Cable side | $V_O = 0$ V (in Hi Z) | 3.3 V | 1.15 | 1.65 | k Ω | |

† Typical values are measured at $V_{CC} = 3.3$ V, V_{CC} CABLE = 5 V, and $T_A = 25^\circ$ C.

‡ V_{CC} CABLE = 4.7 V

§ V_{CC} CABLE = 3.6 V

¶ A maximum current of 170 μ A per pin is added to I_{CC} if the pullup resistor pin is above V_{CC} .

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 1 and 2)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | MIN | TYP† | MAX | UNIT |
|------------------------|------------|--------------------|--------------------------|------|------|------|------|
| t_{PLH} | Totem pole | A or B | B or A | 1 | 40 | ns | ns |
| t_{PHL} | | | | 1 | 40 | | |
| t_{slew} | Totem pole | Cable-side outputs | | 0.05 | 0.4 | V/ns | |
| t_{en} | Totem pole | HD | B, Y, and PERI LOGIC OUT | 1 | 25 | ns | |
| t_{dis} | Totem pole | HD | B, Y, and PERI LOGIC OUT | 1 | 25 | ns | |
| $t_{en} - t_{dis}$ | | | | 1 | 10 | ns | |
| t_{en} | | DIR | A | 1 | 50 | ns | |
| t_{dis} | | DIR | A | 1 | 15 | ns | ns |
| | | | B | 1 | 50 | | |
| t_r, t_f | Open drain | A | B or Y | | 120 | ns | |
| $t_{sk(o)}^{\ddagger}$ | | A or B | B or A | 2.5 | 10 | ns | |

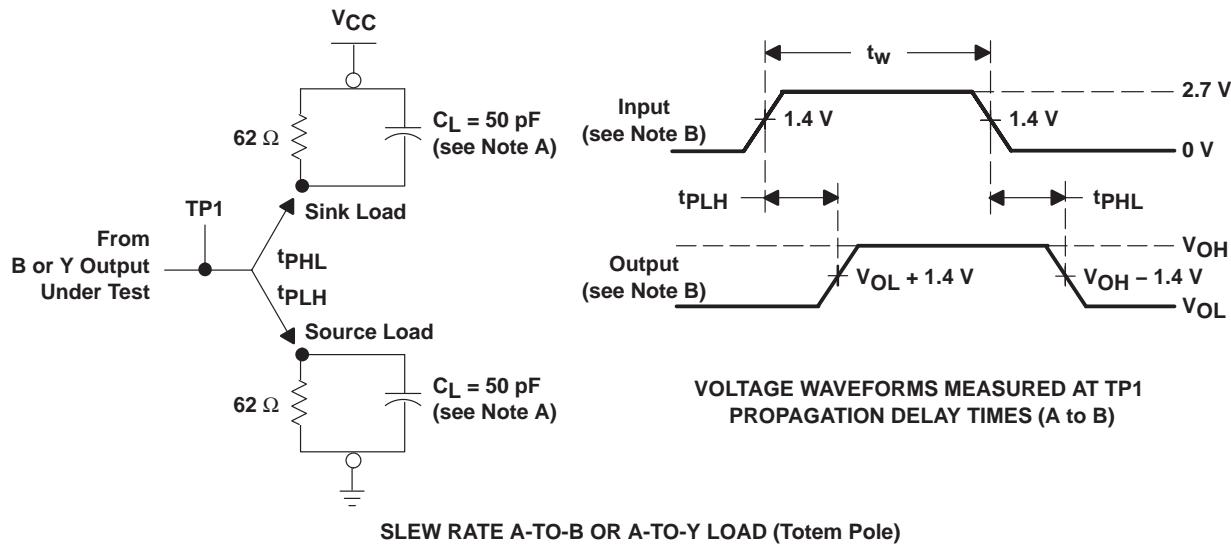
† Typical values are measured at $V_{CC} = 3.3$ V, $V_{CC\ CABLE} = 5$ V, and $T_A = 25^\circ\text{C}$.

‡ Skew is measured at $1/2 (V_{OH} + V_{OL})$ for signals switching in the same direction.

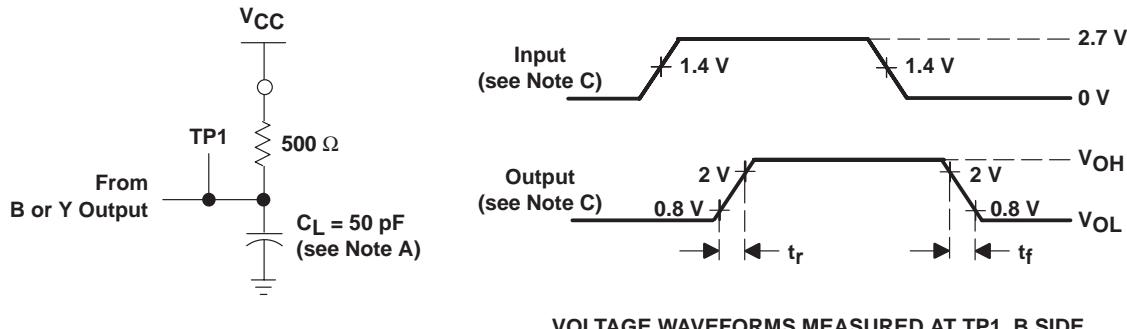
operating characteristics, $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | TYP | UNIT | |
|-----------|-------------------------------|-----------------|-----------------------------|------|----|
| C_{pd} | Power dissipation capacitance | Outputs enabled | $C_L = 0$, $f = 10$ MHz | 45 | pF |

PARAMETER MEASUREMENT INFORMATION



SLEW RATE A-TO-B OR A-TO-Y LOAD (Totem Pole)



A-TO-B LOAD OR A-TO-Y LOAD (Open Drain)

NOTES:

- C_L includes probe and jig capacitance.
- Input rise and fall times are 3 ns, 150 ns < pulse duration < 10 μ s for both low-to-high and high-to-low transitions. Slew rate is measured between 0.4 V and 0.9 V for the rising edge and between 2.4 V and 1.9 V for the falling edge.
- Input rise and fall times are 3 ns. Rise and fall times (open drain) < 120 ns.
- The outputs are measured one at a time, with one transition per measurement.

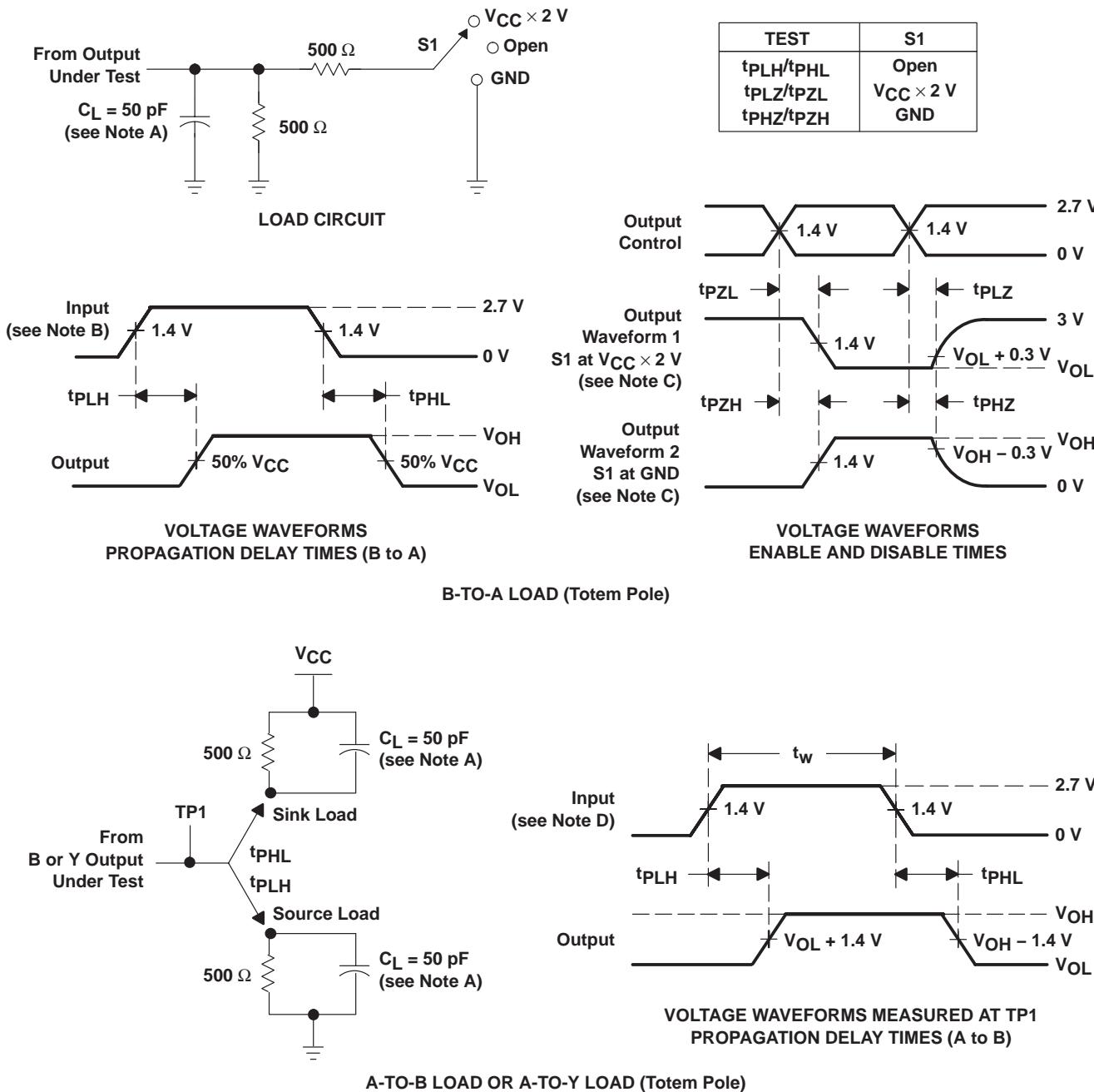
Figure 1. Load Circuits and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



NOTES:

- A. C_L includes probe and jig capacitance.
- B. Input rise and fall times are 3 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. Input rise and fall times are 3 ns. Pulse duration is $150 \text{ ns} < t_W < 10 \mu\text{s}$.
- E. The outputs are measured one at a time, with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 74LVC161284DGGRG4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74LVC161284DLRG4 | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC161284DGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC161284DL | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC161284DLG4 | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC161284DLR | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

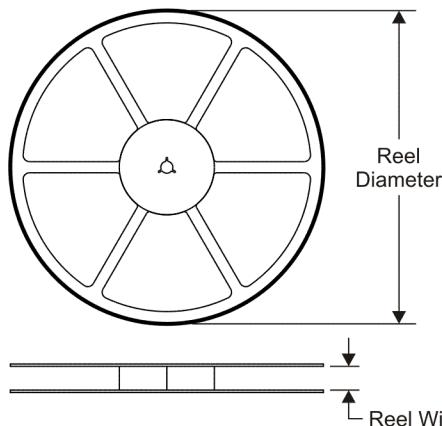
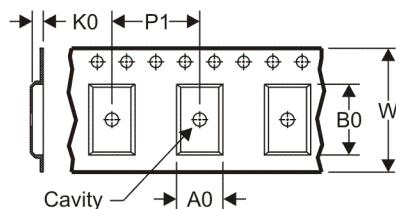
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

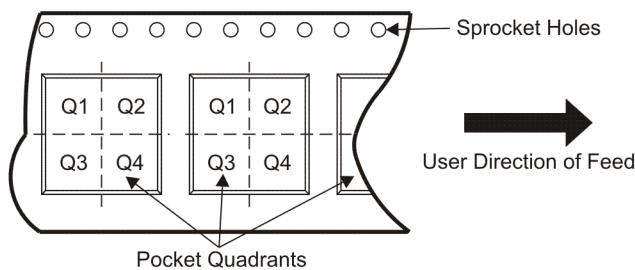
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


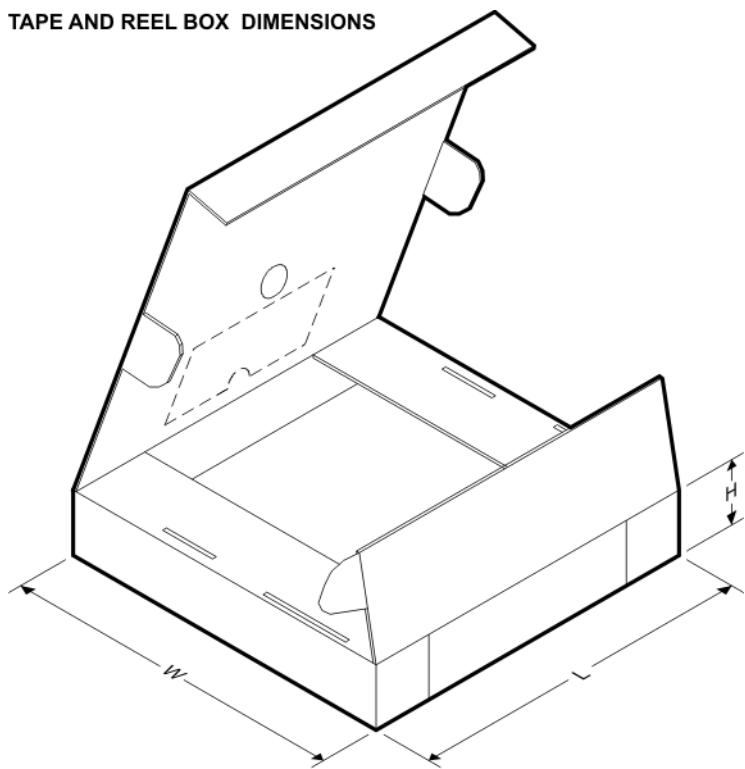
| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC161284DGGR | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 15.8 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74LVC161284DLR | SSOP | DL | 48 | 1000 | 330.0 | 32.4 | 11.35 | 16.2 | 3.1 | 16.0 | 32.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



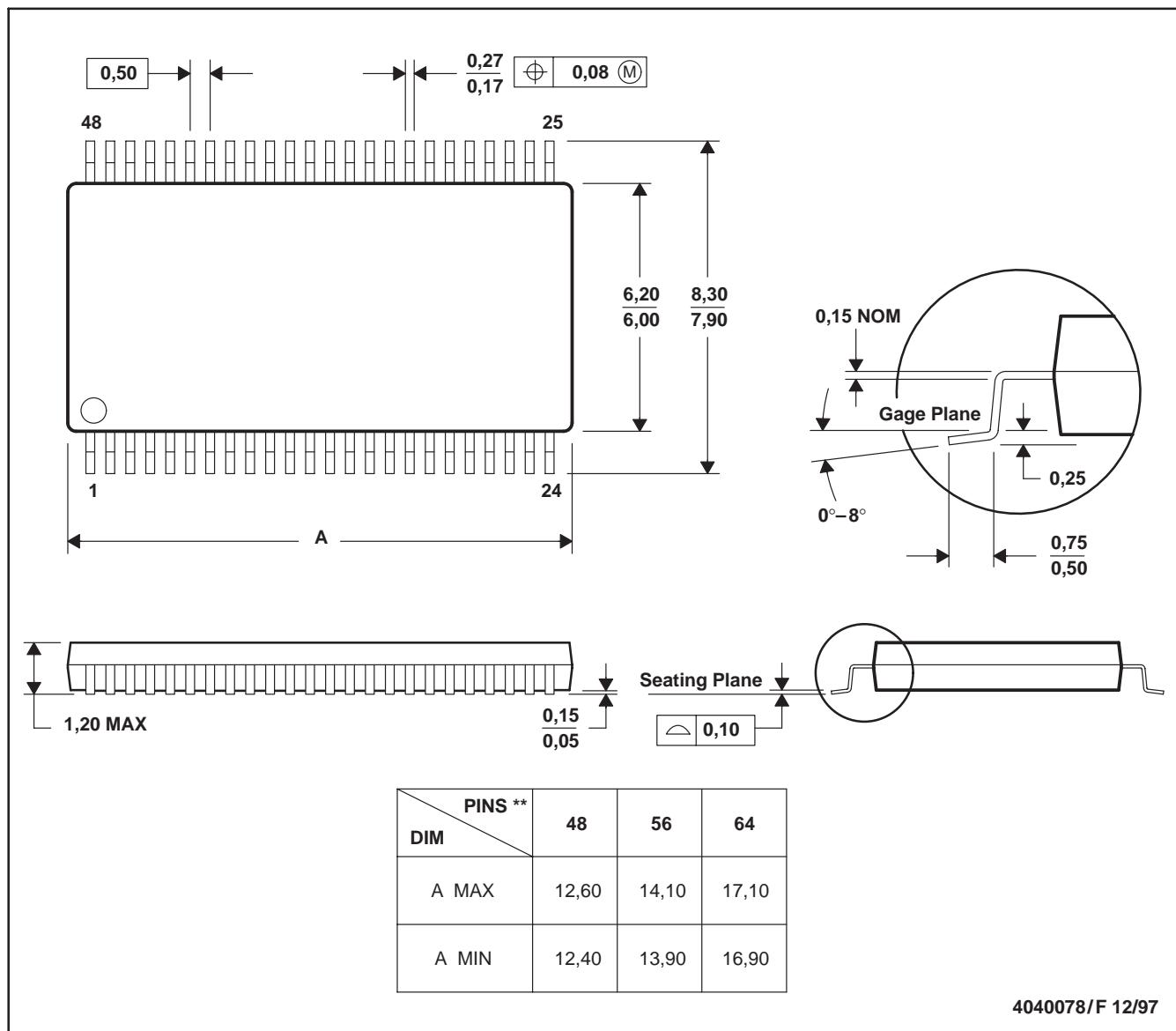
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC161284DGGR | TSSOP | DGG | 48 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74LVC161284DLR | SSOP | DL | 48 | 1000 | 346.0 | 346.0 | 49.0 |

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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