PRELIMINARY

Am29040™

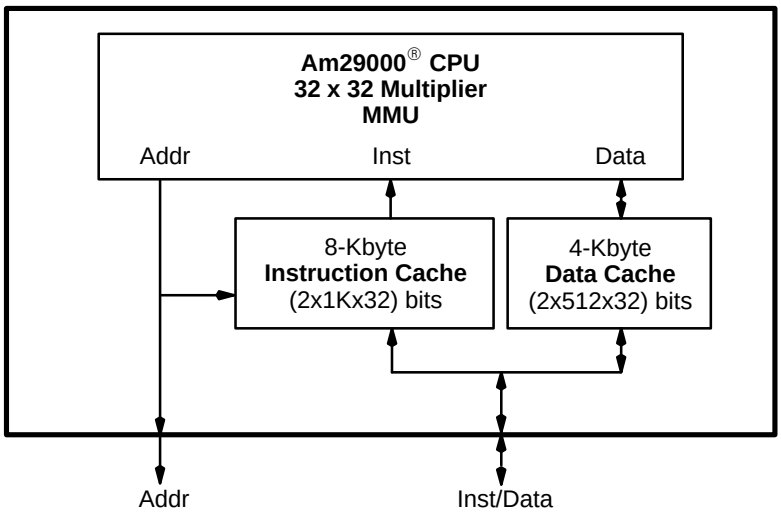
High-Performance RISC Microprocessor with Instruction and Data Caches

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Full 32-bit architecture
- 66.8 VAX MIPS sustained at 50 MHz
- 4-Kbyte, two-way set-associative data cache
- 8-Kbyte, two-way set-associative instruction cache
- Two cycle 32-bit multiplier for fast integer math; three-cycle Multiply Accumulate (MAC) function
- 32-entry on-chip Memory Management Unit with dual Translation Look-Aside Buffers
- Multiprocessor support
- Instruction/data parity on external bus with MMU control of parity checking on page basis
- Data cache control on page basis
- MMU-programmable 16- or 32-bit data bus width on page basis
- Streamlined system interface for simplified, high-frequency operation
- 33-, 40-, and 50-MHz CPU operating frequencies
- Scalable Clocking™ feature with optional clock doubling
- Digital delay-locked loop (DLL) feature for accurate clocking control
- 3.3-V operation with 5-V-tolerant I/O
- Low-power Snooze and Sleep modes
- Fully static
- 8-, 16-, or 32-bit ROM interface
- Burst-mode and page-mode access support
- Pin and bus compatibility with Am29030™ and Am29035™ microprocessors
- Binary compatibility with all 29K™ Family microprocessors and microcontrollers
- CMOS technology/TTL-compatible
- 192 general-purpose registers
- Fully pipelined
- Three-address instruction architecture
- 4-Gbyte virtual address space with demand paging
- On-chip timer facility
- Hardware instruction and data breakpoints for advanced debugging support
- Traceable Cache™ instruction and data cache tracing feature
- IEEE Std 1149.1-1990 (JTAG) compliant Standard Test Access Port and Boundary Scan Architecture implementation

Am29040 MICROPROCESSOR BLOCK DIAGRAM



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GENERAL DESCRIPTION

The Am29040™ RISC microprocessor is a high-performance, general-purpose 32-bit microprocessor implemented in CMOS technology. Designed to extend the price/performance of the 29K Family, the Am29040 microprocessor provides an easy upgrade path for Am29035 and Am29030 microprocessor-based products that require enhanced integer performance. The on-chip data and instruction caches, hardware multiplier, enhanced MMU, and speed upgrades of the Am29040 microprocessor provide the embedded systems designer with increasing levels of performance and software compatibility throughout a range of products.

The Am29040 microprocessor was designed to meet the common requirements of network and color printer applications and other embedded applications such as RAID disk controllers, local area network (LAN) intelligent hubs, multimedia controllers, and interactive TV. High-speed telecommunications and networking applications such as central office switches, low-end PBXs, and wireless LANs will benefit from the data parity, high throughput, the enhanced MMU, and the high-speed features of the Am29040 microprocessor.

High-performance integer applications, especially those that share the bus with other intelligent peripherals, are strong candidates for Am29040 microprocessor-based designs. Coupled with hardware and software development tools from AMD and the AMD Fusion29K® partners, the Am29040 microprocessor provides the embedded systems designer with the cost and performance edge required in today's marketplace. For a complete description of the technical features, programming interface, and instruction set, please refer to the *Am29040 Microprocessor User's Manual* (order #18458).

The Am29040 microprocessor is available in a 145-lead pin grid array (PGA) package and a 144-pin plastic quad flat pack (PQFP) package. The PGA package has 117 signal pins, 26 power and ground pins, 1 alignment/ground pin, and 1 reserved pin. The PQFP package has 117 signal pins, 26 power and ground pins, and 1 reserved pin.

CUSTOMER SERVICE

AMD's customer service network includes U.S. offices, international offices, and a customer training center. Expert technical assistance is available from AMD's worldwide staff of field application engineers and factory support staff.

Hotline, E-mail, and Bulletin Board Support

For answers to technical questions, AMD provides a toll-free number for direct access to our engineering support staff. For overseas customers, the easiest way to reach the engineering support staff with your questions is via fax with a short description of your question. AMD 29K Family customers also receive technical support through electronic mail. This worldwide service is available to 29K Family product users via the international Internet e-mail service. Also available is the AMD bulletin board service, which provides the latest 29K Family product information, including technical information and data on upcoming product releases.

Engineering Support Staff

(800) 292-9263, ext. 2	toll-free for U.S.
0031-11-1163	toll-free for Japan
(512) 602-4118	direct dial worldwide
44-(0)256-811101	U.K. and Europe hotline
(512) 602-5031	fax
epd.support@amd.com	e-mail

Bulletin Board

(800) 292-9263, ext. 1	toll-free for U.S.
(512) 602-7604	direct dial worldwide

Documentation and Literature

A simple phone call gets you free 29K Family information, such as data books, user's manuals, data sheets, application notes, the Fusion29K Partner Solutions Catalog and Newsletter, and other literature. Internationally, contact your local AMD sales office for complete 29K Family literature.

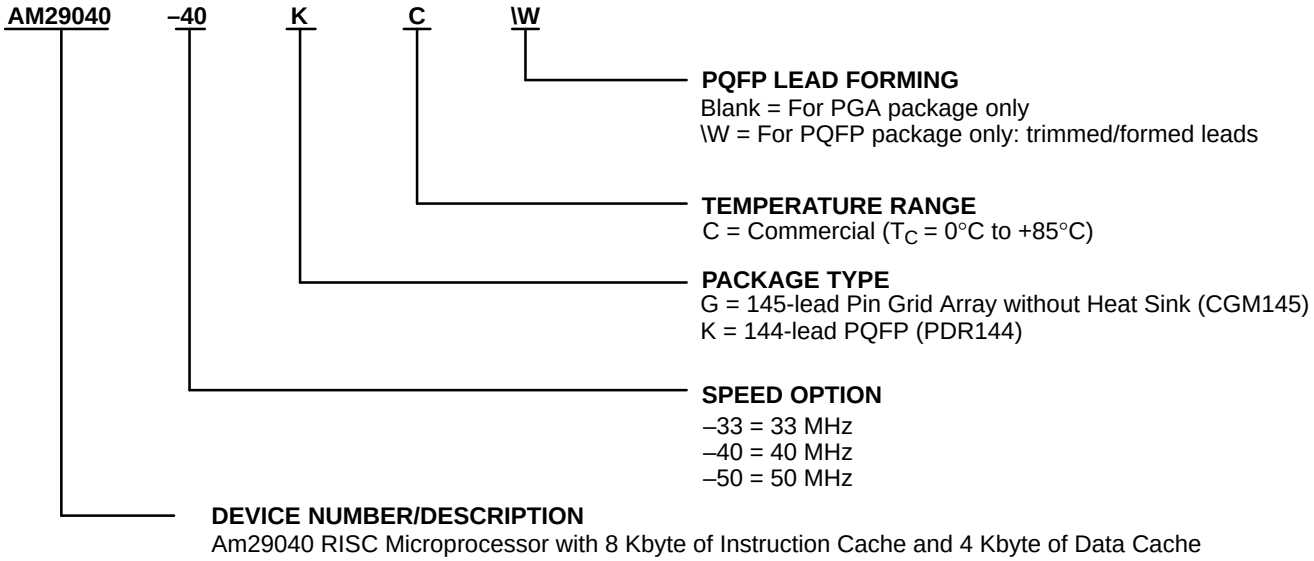
Literature Request

(800) 292-9263, ext. 3	toll-free for U.S.
(512) 602-5651	direct dial worldwide
(512) 602-7639	fax for U.S.
(800) 222-9323, option 1	AMD Facts-On-Demand™ fax information service toll-free for U.S.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM29040–33 AM29040–40 AM29040–50	GC
AM29040–33 AM29040–40 AM29040–50	KC\W

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

RELATED AMD PRODUCTS

29K Family Devices

Product	Description
Am29000®	32-bit RISC microprocessor
Am29005™	Low-cost 32-bit RISC microprocessor with no MMU and no branch target cache
Am29030™	32-bit RISC microprocessor with 8-Kbyte instruction cache
Am29035™	32-bit RISC microprocessor with 4-Kbyte instruction cache
Am29050™	32-bit RISC microprocessor with on-chip floating point
Am29200™	32-bit RISC microcontroller
Am29202™	Low-cost 32-bit RISC microcontroller with IEEE-1284-compliant parallel interface
Am29205™	Low-cost 32-bit RISC microcontroller
Am29240™	32-bit RISC microcontroller with 4-Kbyte instruction cache and 2-Kbyte data cache
Am29245™	Low-cost 32-bit RISC microcontroller with 4-Kbyte instruction cache
Am29243™	32-bit data RISC microcontroller with instruction and data caches and DRAM parity

29K FAMILY DEVELOPMENT SUPPORT PRODUCTS

Contact your local AMD representative for information on the complete set of development support tools. The following software and hardware development products are available on several hosts:

- Optimizing compilers for common high-level languages
- Assembler and utility packages
- Source- and assembly-level software debuggers
- Target-resident development monitors
- Simulators
- Demonstration and evaluation boards

THIRD-PARTY DEVELOPMENT SUPPORT PRODUCTS

The Fusion29K Program of Partnerships for Application Solutions provides the user with a vast array of products designed to meet critical time-to-market needs. Products and solutions available from the AMD Fusion29K Partners include

- Silicon products
- Emulators
- Hardware and software debuggers
- Modeling/simulation tools
- Software development tools
- Real-time operating systems (RTOS)
- Application-specific hardware and software
- Board-level products
- Manufacturing and prototyping support
- Custom support
- Training

KEY FEATURES AND BENEFITS

The Am29040 microprocessor extends the family of two-bus RISC processors based on AMD's 29K architecture, providing powerful performance upgrades to the Am29030 and Am29035 microprocessors. The product designer can choose from among several different design strategies to gain significant cost and performance improvements.

- **Upgrading to maximal performance**—For example, the clock-doubling feature on a 50-MHz Am29040 microprocessor can be configured to deliver up to twice the performance of a 25-MHz Am29030 microprocessor at a small increase in system cost, keeping the external bus speed and memory system the same.
- **Upgrading to minimize system cost**—For example, the clock-doubling feature on a 40-MHz Am29040 microprocessor can be combined with a reduction in external bus speed to deliver up to 77% more performance than a 25-MHz Am29030 microprocessor, at similar or less system cost (by reducing the cost of the memory system).

Specific performance enhancements include an on-chip data cache, a two-cycle hardware multiplier, an enhanced MMU, speed upgrades, and multiprocessing features. General system enhancements include on-chip support for parity generation and checking, low-power Snooze and Sleep modes, and expanded clocking control. Debug and test enhancements include hardware instruction and data breakpoints, as well as instruction and data cache tracing.

On-Chip Caches

The Am29040 microprocessor incorporates an 8-Kbyte, two-way set-associative instruction cache that supplies most processor instructions without wait states at the internal processor frequency. For best performance, the instruction cache supports critical-word-first reloading with fetch-through, so that the processor receives the required instruction and the pipeline restarts with minimum delay. The instruction cache has a valid bit per word to minimize reload overhead and pipeline stalls. All instruction cache array elements are visible to software for testing and preload.

The Am29040 microprocessor also incorporates a 4-Kbyte, two-way set-associative data cache. Cacheable and noncacheable regions are specified by the MMU. The data cache is physically addressed and operates in the write-back stage of the processor pipeline, so that loaded data is available to the second instruction following the load without causing a pipeline stall.

The data cache uses a copy-back policy with no-write allocation. This reduces the amount of time the processor waits on data that is not in the cache. As an option, regions of memory can use a write-through policy, as controlled by the MMU. A cache consistency protocol facilitates the implementation of multiprocessing systems and of input/output or DMA to cacheable memory. Byte, half-word, and word reads and writes are supported. All data cache array elements are visible to software for testing and preload.

Two-Cycle Multiplier

The Am29040 microprocessor incorporates a full combinatorial multiplier that accepts two 32-bit input operands and produces a 32-bit result in two cycles. High-performance multiplication benefits imaging, signal processing, and state modeling applications.

Scalable Clocking Technology with Expanded Clocking Control

The Am29040 microprocessor offers expanded clocking control features that aid in the design of low-cost, high-frequency designs. These features include a full or double-speed clocking option and a highly precise clock control mechanism.

Clock doubling allows the processor to run at twice the frequency of the external bus. For example, the interface can operate at 25 MHz, while the processor operates at 50 MHz. This feature allows the use of slower, lower-cost memory without significant degradation of processor performance. A 40-MHz processor could be combined with a 20-MHz memory system with only a slight loss in performance relative to a full-speed bus. Another advantage is that system performance can be upgraded by simply replacing the processor with a higher-speed processor. For example, a processor can be replaced with a faster processor while utilizing the existing memory system, running at half-speed if necessary.

The Am29040 microprocessor uses an extremely precise digital version of a phase-locked loop to control frequency multiplication and phase generation for the input clock. This allows the processor to use oscillators with duty cycles of 30/70 to 70/30. Relaxed timing specifications reduce the cost and complexity of the external system design.

High-frequency operation is further simplified through the use of a hardwired wait state, which is enforced during the initial cycle of all simple data accesses and the initial cycle of a burst-mode access. The main benefit of this approach is that the address and data pins are not required to change state during the same cycle. This reduces electrical noise and provides great benefits for high-frequency designs.

Parity

The Am29040 microprocessor provides byte parity checking and generation on the instruction/data bus. When parity is supplied by the system, the processor checks for valid parity during the cycle after the data is received, and parity is checked only for those bytes actually involved in the transfer. The Am29040 microprocessor allows parity errors on instruction and data accesses to be differentiated from one another.

Enhanced Memory Management Unit

The Am29040 microprocessor provides an enhanced memory-management unit (MMU) for translating virtual addresses into physical addresses. The page size for translation ranges from 1 Kbyte to 16 Mbyte in powers of four. The Am29040 microprocessor has dual 16-entry TLBs, each capable of mapping pages of different size.

In addition to the traditional functions, the Am29040 microprocessor's MMU includes several features that enhance the performance of the entire system.

- **Parity Checking**—The MMU allows the designer to define which parts of memory are checked for parity.
- **Data Cacheability by Page**—Though the data cache uses a copy-back policy for most blocks, individual virtual pages can be marked as write-through by the MMU. The MMU also allows pages to be marked as noncacheable, so that all accesses to the page are performed on the external bus.
- **Programmable Bus Sizing**—Using the MMU, the Am29040 processor's instruction/data bus can be dynamically programmed to be either 16 or 32 bits wide for data transfers. This enables the Am29040 microprocessor to write either 16-bit or 32-bit devices. The processor automatically performs multiple 16-bit writes when writing more than 16 bits to a 16-bit external device.

  This unique feature provides a flexible interface to low-cost memory, as well as a convenient, flexible upgrade path. For example, a system can start with a 16-bit memory design and can subsequently improve performance by migrating to a 32-bit memory design. Of particular advantage is the ability to add memory in half-megabyte increments. This provides significant cost savings for applications that do not require larger memory upgrades.

Low-Power Snooze and Sleep Modes

Within the wait mode, the Am29040 microprocessor offers two special standby modes for low power dissipation: Snooze mode and Sleep mode. The Snooze mode has slightly higher power dissipation than Sleep mode, but is invoked automatically without external hardware, whereas Sleep mode requires external hardware to gate off clocks.

Because the processor's internal clocks are disabled, the power dissipated in Snooze mode is only that associated with internal leakage, trap and interrupt synchronization, and on-chip clock generation. Minimum power dissipation is achieved in Sleep mode by holding the input clock High or Low. In this case, the power dissipated is only that associated with internal leakage. Both Snooze and Sleep modes can be used by product designers interested in gaining the U.S. Environmental Protection Agency's "Energy Star" certification.

Narrow Read Interface

The Am29040 microprocessor can be connected to 8-, 16-, or 32-bit memories. If the data size accessed is larger than that supported by memory, the processor automatically generates the necessary sequencing to perform multiple reads.

This ability to perform narrow reads is particularly useful for a ROM interface. Using narrow reads, the processor can execute a bootstrap program from a small boot ROM to download the application program into RAM. This not only allows the use of low-cost ROMs, it also conserves board space and allows easy revision of application code.

Streamlined System Interface

The Am29040 microprocessor employs a streamlined, two-bus external interface, which comprises an address bus and an instruction/data bus. The large on-chip instruction and data caches of the Am29040 microprocessor satisfy the instruction and data bandwidth requirements. This allows the use of lower-performance and lower-cost memory, provides a reduction in the memory-system parts count, and reduces the board area required for the memory system. In addition, the simplified design requirements reduce development costs.

Pin, Bus, and Binary Compatibility

Compatibility within a processor family is critical for achieving a rational, easy upgrade path. The Am29040 microprocessor provides compatibility on several levels. The processors are pin, bus, and binary compatible with the Am29030 and Am29035 processors. Pin and bus compatibility ensures a convenient upgrade path, without hardware or software redesign, for embedded applications. In addition, the processors are binary compatible with the existing members of the 29K family (the Am29000, Am29005, and Am29050 microprocessors, and the Am29200, Am29202, Am29205, Am29240, Am29243, and Am29245 microcontrollers).

Wide Range of Price/Performance Points

To reduce design costs and time-to-market, one basic system design can be used as the foundation for an entire product line. Using AMD's two-bus processors, the Am29030, Am29035, and Am29040 microprocessors, numerous implementations of a product at various price/performance levels can be derived with minimum time, effort, and cost.

The Am29040 microprocessor allows the product designer to significantly expand the performance range of a product line through its on-chip caches, extended MMU, hardware multiplier, and speed upgrades. Processors can be upgraded without hardware and software redesign and combined with high-performance or mid-performance memory. The narrow read interface accommodates numerous ROM configurations. In addition, programmable bus sizing allows Am29040 microprocessor-based systems to support memory upgrades in half-megabyte increments. This provides significant cost savings for applications that do not require larger memory upgrades.

Complete Development and Support Environment

A complete development and support environment is vital for reducing a product's time-to-market. Advanced Micro Devices has created a standard development environment for the 29K Family of processors. In addition, the Fusion29K program's third-party support organization provides the most comprehensive customer/partner program in the embedded processor market.

Advanced Micro Devices offers a complete set of hardware and software tools for design, integration, debugging, and benchmarking. These tools, which are available now for the 29K Family, include the following:

- Software development kit, including the High C® 29K optimizing C compiler with assembler, linker, ANSI library functions, 29K Family architectural simulator, and MiniMON29K® debug monitor
- XRAY29K™ source-level debugger
- A complete family of demonstration and development boards

In addition, Advanced Micro Devices has developed a standard host interface (HIF) specification for operating system services, the Universal Debug Interface (UDI) for seamless connection of debuggers to ICEs and target hardware, and extensions for the UNIX common object file format (COFF).

This support is augmented by an engineering hotline, an on-line bulletin board, and field application engineers.

Debugging and Testing

The Am29040 microprocessor provides debugging and testing features at both the software and hardware levels.

Software debugging is facilitated by the instruction trace facility and instruction breakpoints. Instruction tracing is accomplished by forcing the processor to trap after each instruction has been executed. Instruction breakpoints are implemented by the HALT instruction or by a software trap.

The Am29040 microprocessor provides two hardware instruction breakpoints and one hardware data breakpoint that can suspend execution of the current program on a specified instruction or data access. Suspension either forces a trace trap or forces a halt if the system is under emulator control.

The processor provides several additional features to assist system debugging and testing.

- **Test/Development Interface**—This interface is composed of a group of pins that indicate the state of the processor and control the operation of the processor.
- **Traceable Cache Feature**—This feature permits a hardware-development system to track accesses to the on-chip caches, permitting a high level of visibility into processor operation.
- **IEEE Std 1149.1-1990 (JTAG) Compliant Standard Test Access Port and Boundary-Scan Architecture**—This feature provides a scan interface for testing processor and system hardware in a production environment. It contains extensions that allow a hardware-development system to control and observe the processor without interposing hardware between the processor and system.

PERFORMANCE OVERVIEW

The Am29040 microprocessor provides a significant margin of performance over other processors in its class, since the majority of processor features were defined for the maximum achievable performance at a reasonable cost. This section describes the features of the Am29040 microprocessor from the point of view of system performance.

Instruction Timing

The Am29040 microprocessor uses an arithmetic/logic unit, a field shift unit, and a prioritizer to execute most instructions. Each of these is organized to operate on 32-bit operands and provide a 32-bit result.

The performance degradation of load and store operations is minimized in the Am29040 microprocessor by overlapping them with instruction execution, by taking advantage of pipelining, by using the on-chip data cache, and by organizing the flow of external data into the processor so that the impact of external accesses is minimized.

Pipelining

Instruction operations are overlapped with instruction fetch, instruction decode, operand fetch, and result write-back to the register file. Pipeline forwarding logic detects pipeline dependencies and routes data as required, avoiding delays that might arise from these dependencies.

Pipeline interlocks are implemented by processor hardware. Except for a few special cases, it is not necessary to rearrange programs to avoid pipeline dependencies, although this is sometimes desirable for performance.

On-Chip Instruction and Data Caches

On-chip instruction and data caches satisfy most processor fetches without wait states, even when the processor operates at twice the system frequency. The caches are pipelined for best performance. The reload policies minimize the amount of time spent waiting for reload while optimizing the benefit of locality of reference.

Burst-Mode and Page-Mode Memories

The Am29040 microprocessor directly supports burst-mode memories. The burst-mode memory supplies instructions at the maximum bandwidth, without the complexity of an external cache or the performance degradation due to cache misses.

The processor can also use the page-mode capability of common DRAMs to improve the access time in cases where page-mode accesses can be used. This is particularly useful in very low-cost systems with 16-bit-wide DRAMs, where the DRAM must be accessed twice for each 32-bit operand.

Instruction Set Overview

All 29K Family members employ a three-address instruction set architecture. The compiler or assembly-language programmer is given complete freedom to allocate register usage. There are 192 general-purpose registers, allowing the retention of intermediate calculations and avoiding needless data destruction. Instruction operands can be contained in any of the general-purpose registers, and the results can be stored into any of the general-purpose registers.

The Am29040 microprocessor instruction set contains 117 instructions that are divided into nine classes. These classes are integer arithmetic, compare, logical, shift, data movement, constant, floating point, branch, and miscellaneous. The floating-point instructions are not executed directly, but are emulated by trap handlers.

All directly implemented instructions are capable of executing in one processor cycle, with the exception of interrupt returns, loads, stores, and integer multiplies.

Data Formats

The Am29040 microprocessor defines a word as 32 bits of data, a half-word as 16 bits, and a byte as 8 bits. The hardware provides direct support for word-integer (signed and unsigned), word-logical, word-Boolean, half-word integer (signed and unsigned), and byte data (signed and unsigned).

Word-Boolean data is based on the value contained in the most significant bit of the word. The values TRUE and FALSE are represented by the most significant bit values 1 and 0, respectively.

Other data formats, such as character strings, are supported by instruction sequences. Floating-point formats (single and double precision) are defined for the processors; however, there is no direct hardware support for these formats in the Am29040 microprocessor.

Protection

The Am29040 microprocessor offers two mutually exclusive modes of execution, the User and Supervisor modes, that restrict or permit accesses to certain processor registers and external storage locations.

Memory access protection is provided by the MMU. Four protection bits determine whether or not an access is permitted to the page associated with the entry. For the same virtual page, the access authority of programs executing in supervisor mode can be different from the authority of programs executing in user mode.

The register file can be configured to restrict accesses to Supervisor-mode programs on a bank-by-bank basis.

Memory Management

Two 16-entry Translation Look-Aside Buffers (TLBs) perform virtual-to-physical address translation. A number of enhancements improve the performance of address translation:

- **Pipelining**—The operation of the TLBs is pipelined with other processor operations.
- **Task Identifiers**—Task identifiers allow TLB entries to be matched to different processes, so that TLB invalidation is not required during task switches.
- **Least-Recently Used Hardware**—This hardware allows immediate selection of a TLB entry to be replaced.
- **Software Reload**—Software reload allows the operating system to use a page-mapping scheme that is best matched to its environment. One of Paged-segmented, one-level-page mapping, two-level-page mapping, or any other user-defined page-mapping scheme can be supported. Because Am29040 microprocessor instructions execute at an average rate of nearly one instruction per cycle, software reload has performance approaching that of hardware TLB reload without imposing restrictions on the system designer.
- **Dual-TLB Configuration**—This configuration allows system architects to configure one TLB to map most of the system and configure the other TLB to map the exceptions (noncacheable data areas, for example).

Interrupts and Traps

When the Am29040 microprocessor takes an interrupt or trap, operation continues from a shadow set of state registers while the interrupted program state registers are frozen. This eliminates the need to save interrupted program state in many cases. This lightweight interrupt and trap facility greatly improves the performance of temporary interruptions such as TLB reload or other simple operating-system calls that require no saving of state information.

In cases where the processor state must be saved, the saving and restoring of state information is under the control of software. The methods and data structures used to handle interrupts—and the amount of state saved—can be tailored to the needs of a particular system.

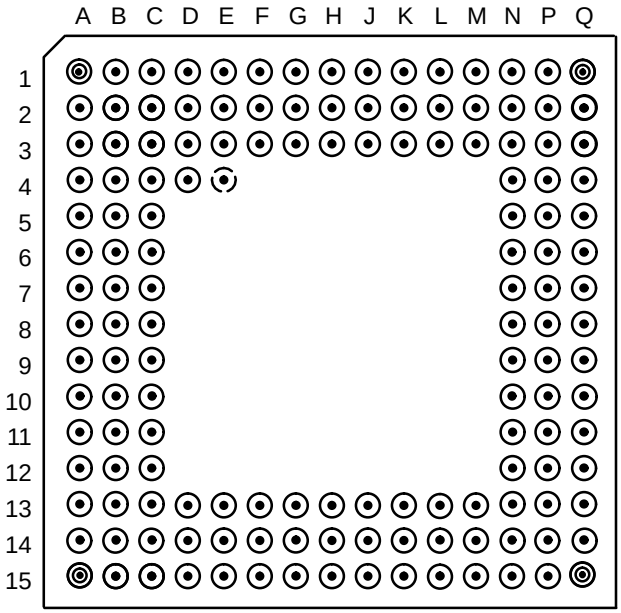
Interrupts and traps are dispatched through a 256-entry vector table that directs the processor to a routine that handles a given interrupt or trap. The vector table can be relocated in memory by the modification of a processor register. There can be multiple vector tables in the system, though only one is active at any given time.

The vector table is a table of pointers to the interrupt and trap handlers, requiring only 1 Kbyte of memory. This structure requires that the processors perform a vector fetch every time an interrupt or trap is taken. The vector fetch requires at least three cycles, in addition to the number of cycles required for the basic memory access.

CONNECTION DIAGRAMS

145-Lead PGA

Bottom View



Note:

Pinout observed from pin side of package (pins facing viewer).

Pin Number E–4 is defined for emulator access and is not a physical pin on the package (see the Am29040 Microprocessors User's Manual, order #18458, Signal Description section).

PGA PIN DESIGNATIONS
(Sorted by Pin Number)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A-1	ID4	**C-8**	GND	**H-14**	MEMCLK	**N-12**	V_{CC}
A-2	ID0	**C-9**	V_{CC}	**H-15**	$\overline{DIV2}$	**N-13**	A1
A-3	$\overline{TRST}$	**C-10**	GND	**J-1**	ID21	**N-14**	$\overline{ERLYA}$
A-4	TDI	**C-11**	V_{CC}	**J-2**	ID22	**N-15**	$\overline{ERR}$
A-5	TCK	**C-12**	STAT1	**J-3**	GND	**P-1**	ID31
A-6	$\overline{TEST}$	**C-13**	$\overline{WBC}$	**J-13**	INCLK	**P-2**	A30
A-7	I/$\overline{D}$	**C-14**	$\overline{HIT}$	**J-14**	CLKDRV	**P-3**	A27
A-8	IO/$\overline{MEM}$	**C-15**	$\overline{INTR}$0	**J-15**	$\overline{BREQ}$	**P-4**	A24
A-9	$\overline{BWE}$0	**D-1**	ID12	**K-1**	ID23	**P-5**	A22
A-10	$\overline{BWE}$2	**D-2**	ID11	**K-2**	ID24	**P-6**	A20
A-11	SUP/$\overline{US}$	**D-3**	ID9	**K-3**	V_{CC}	**P-7**	A18
A-12	OPT0	**D-4** ♦	GND	**K-13**	GND	**P-8**	A15
A-13	OPT2	**D-13**	$\overline{DI}$	**K-14**	$\overline{REQ}$	**P-9**	A13
A-14	MPGM1	**D-14**	$\overline{INTR}$1	**K-15**	$\overline{BURST}$	**P-10**	A10
A-15	STAT2	**D-15**	$\overline{INTR}$2	**L-1**	ID25	**P-11**	A8
B-1	ID7	**E-1**	ID14	**L-2**	ID26	**P-12**	A6
B-2	ID6	**E-2**	ID13	**L-3**	V_{CC}	**P-13**	A4
B-3	ID3	**E-3**	GND	**L-13**	V_{CC}	**P-14**	A2
B-4	ID1	**E-13**	GND	**L-14**	$\overline{BGRT}$	**P-15**	A0
B-5	TDO	**E-14**	$\overline{INTR}$3	**L-15**	$\overline{PGMODE}$	**Q-1**	A31
B-6	TMS	**E-15**	$\overline{TRAP}$1	**M-1**	ID27	**Q-2**	A29
B-7	R/$\overline{W}$	**F-1**	ID16	**M-2**	ID28	**Q-3**	A25
B-8	$\overline{WARN}$	**F-2**	ID15	**M-3**	IDP2	**Q-4**	A23
B-9	$\overline{BWE}$1	**F-3**	IDP1	**M-13**	GND	**Q-5**	A21
B-10	$\overline{BWE}$3	**F-13**	V_{CC}	**M-14**	$\overline{RDN}$	**Q-6**	A19
B-11	$\overline{LOCK}$	**F-14**	$\overline{RESET}$	**M-15**	$\overline{RDY}$	**Q-7**	A17
B-12	OPT1	**F-15**	$\overline{TRAP}$0	**N-1**	ID29	**Q-8**	A16
B-13	MPGM0	**G-1**	ID18	**N-2**	ID30	**Q-9**	A14
B-14	STAT0	**G-2**	ID17	**N-3**	IDP3	**Q-10**	A12
B-15	No Connect	**G-3**	V_{CC}	**N-4**	A28	**Q-11**	A11
C-1	ID10	**G-13**	V_{CC}	**N-5**	A26	**Q-12**	A9
C-2	ID8	**G-14**	CNTL0	**N-6**	GND	**Q-13**	A7
C-3	IDP0	**G-15**	CNTL1	**N-7**	V_{CC}	**Q-14**	A5
C-4	ID5	**H-1**	ID20	**N-8**	GND	**Q-15**	A3
C-5	ID2	**H-2**	ID19	**N-9**	GND		
C-6	V_{CC}	**H-3**	GND	**N-10**	GND		
C-7	GND	**H-13**	GND	**N-11**	V_{CC}		

Notes:

♦ *Pin Number D-4 is the alignment/ground pin and must be electrically connected to ground.*

Pin Number E-4 is defined for emulator access and is not a physical pin on the package. (See Am29040 Microprocessor User's Manual, Signal Description section.)

PGA PIN DESIGNATIONS
(Sorted by Pin Name)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A0	P-15	**$\overline{\text{BWE2}}$**	A-10	**ID11**	D-2	**OPT1**	B-12
A1	N-13	**$\overline{\text{BWE3}}$**	B-10	**ID12**	D-1	**OPT2**	A-13
A2	P-14	**CLKDRV**	J-14	**ID13**	E-2	**$\overline{\text{PGMODE}}$**	L-15
A3	Q-15	**CNTL0**	G-14	**ID14**	E-1	**$\overline{\text{RDN}}$**	M-14
A4	P-13	**CNTL1**	G-15	**ID15**	F-2	**$\overline{\text{RDY}}$**	M-15
A5	Q-14	**$\overline{\text{DI}}$**	D-13	**ID16**	F-1	**$\overline{\text{RESET}}$**	F-14
A6	P-12	**$\overline{\text{DIV2}}$**	H-15	**ID17**	G-2	**$\overline{\text{REQ}}$**	K-14
A7	Q-13	**$\overline{\text{ERLYA}}$**	N-14	**ID18**	G-1	**R/$\overline{\text{W}}$**	B-7
A8	P-11	**$\overline{\text{ERR}}$**	N-15	**ID19**	H-2	**STAT0**	B-14
A9	Q-12	**GND**	C-7	**ID20**	H-1	**STAT1**	C-12
A10	P-10	**GND**	C-8	**ID21**	J-1	**STAT2**	A-15
A11	Q-11	**GND**	C-10	**ID22**	J-2	**SUP/$\overline{\text{US}}$**	A-11
A12	Q-10	**GND**	D-4 ♦	**ID23**	K-1	**TCK**	A-5
A13	P-9	**GND**	E-3	**ID24**	K-2	**TDI**	A-4
A14	Q-9	**GND**	E-13	**ID25**	L-1	**TDO**	B-5
A15	P-8	**GND**	H-3	**ID26**	L-2	**$\overline{\text{TEST}}$**	A-6
A16	Q-8	**GND**	H-13	**ID27**	M-1	**TMS**	B-6
A17	Q-7	**GND**	J-3	**ID28**	M-2	**$\overline{\text{TRAP0}}$**	F-15
A18	P-7	**GND**	K-13	**ID29**	N-1	**$\overline{\text{TRAP1}}$**	E-15
A19	Q-6	**GND**	M-13	**ID30**	N-2	**$\overline{\text{TRST}}$**	A-3
A20	P-6	**GND**	N-6	**ID31**	P-1	**V_{CC}**	C-6
A21	Q-5	**GND**	N-8	**IDP0**	C-3	**V_{CC}**	C-9
A22	P-5	**GND**	N-9	**IDP1**	F-3	**V_{CC}**	C-11
A23	Q-4	**GND**	N-10	**IDP2**	M-3	**V_{CC}**	F-13
A24	P-4	**$\overline{\text{HIT}}$**	C-14	**IDP3**	N-3	**V_{CC}**	G-3
A25	Q-3	**I/$\overline{\text{D}}$**	A-7	**INCLK**	J-13	**V_{CC}**	G-13
A26	N-5	**ID0**	A-2	**$\overline{\text{INTR0}}$**	C-15	**V_{CC}**	K-3
A27	P-3	**ID1**	B-4	**$\overline{\text{INTR1}}$**	D-14	**V_{CC}**	L-3
A28	N-4	**ID2**	C-5	**$\overline{\text{INTR2}}$**	D-15	**V_{CC}**	L-13
A29	Q-2	**ID3**	B-3	**$\overline{\text{INTR3}}$**	E-14	**V_{CC}**	N-7
A30	P-2	**ID4**	A-1	**IO/$\overline{\text{MEM}}$**	A-8	**V_{CC}**	N-11
A31	Q-1	**ID5**	C-4	**$\overline{\text{LOCK}}$**	B-11	**V_{CC}**	N-12
$\overline{\text{BGRT}}$	L-14	**ID6**	B-2	**MEMCLK**	H-14	**$\overline{\text{WARN}}$**	B-8
$\overline{\text{BREQ}}$	J-15	**ID7**	B-1	**MPGM0**	B-13	**$\overline{\text{WBC}}$**	C-13
$\overline{\text{BURST}}$	K-15	**ID8**	C-2	**MPGM1**	A-14		
$\overline{\text{BWE0}}$	A-9	**ID9**	D-3	**No Connect**	B-15		
$\overline{\text{BWE1}}$	B-9	**ID10**	C-1	**OPT0**	A-12		

Notes:

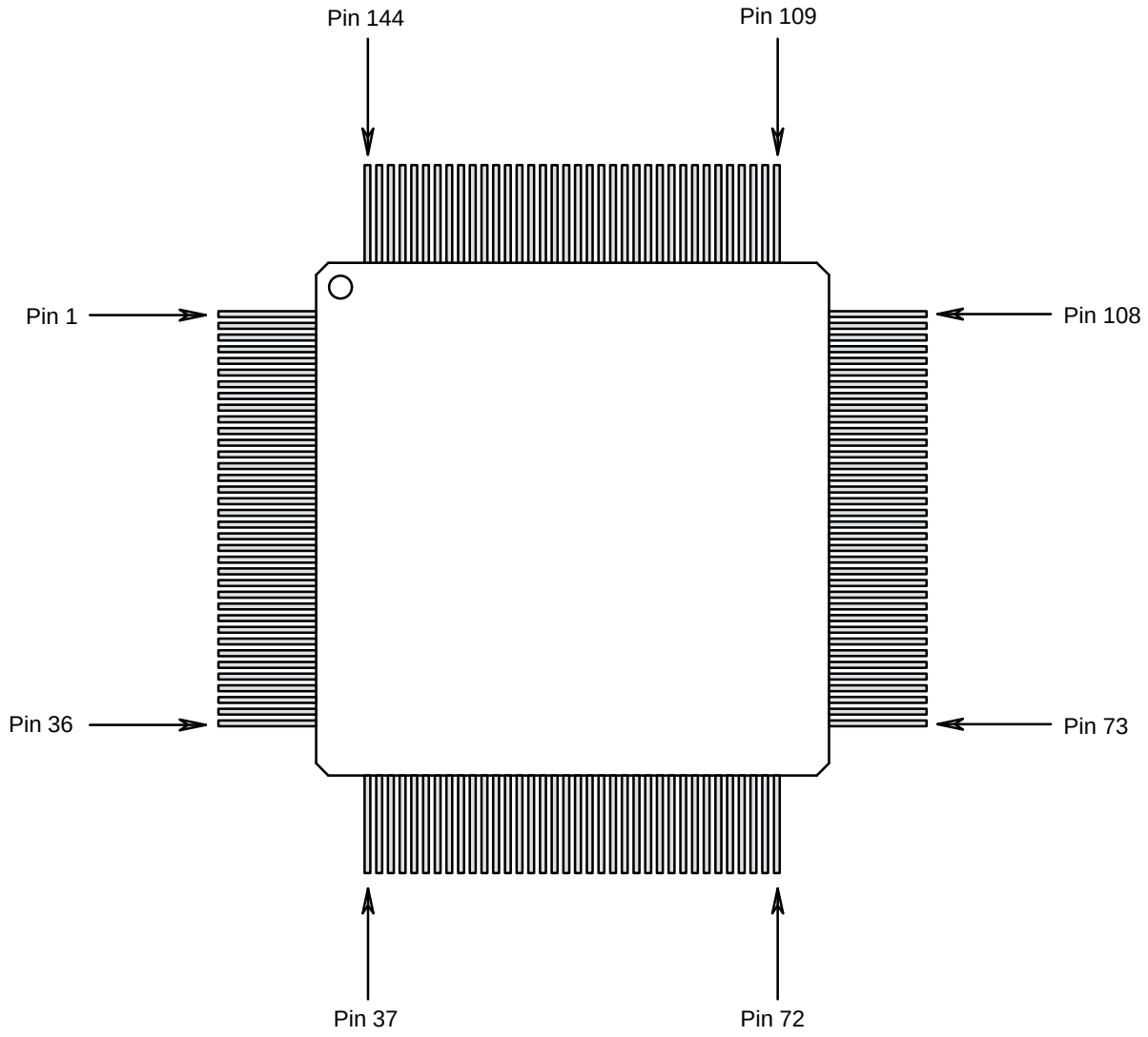
♦ *Pin Number D-4 is the alignment/ground pin and must be electrically connected to ground.*

Pin Number E-4 is defined for emulator access and is not a physical pin on the package. (See Am29040 Microprocessor User's Manual, Signal Description section.)

CONNECTION DIAGRAMS (continued)

144-Lead PQFP

Top View



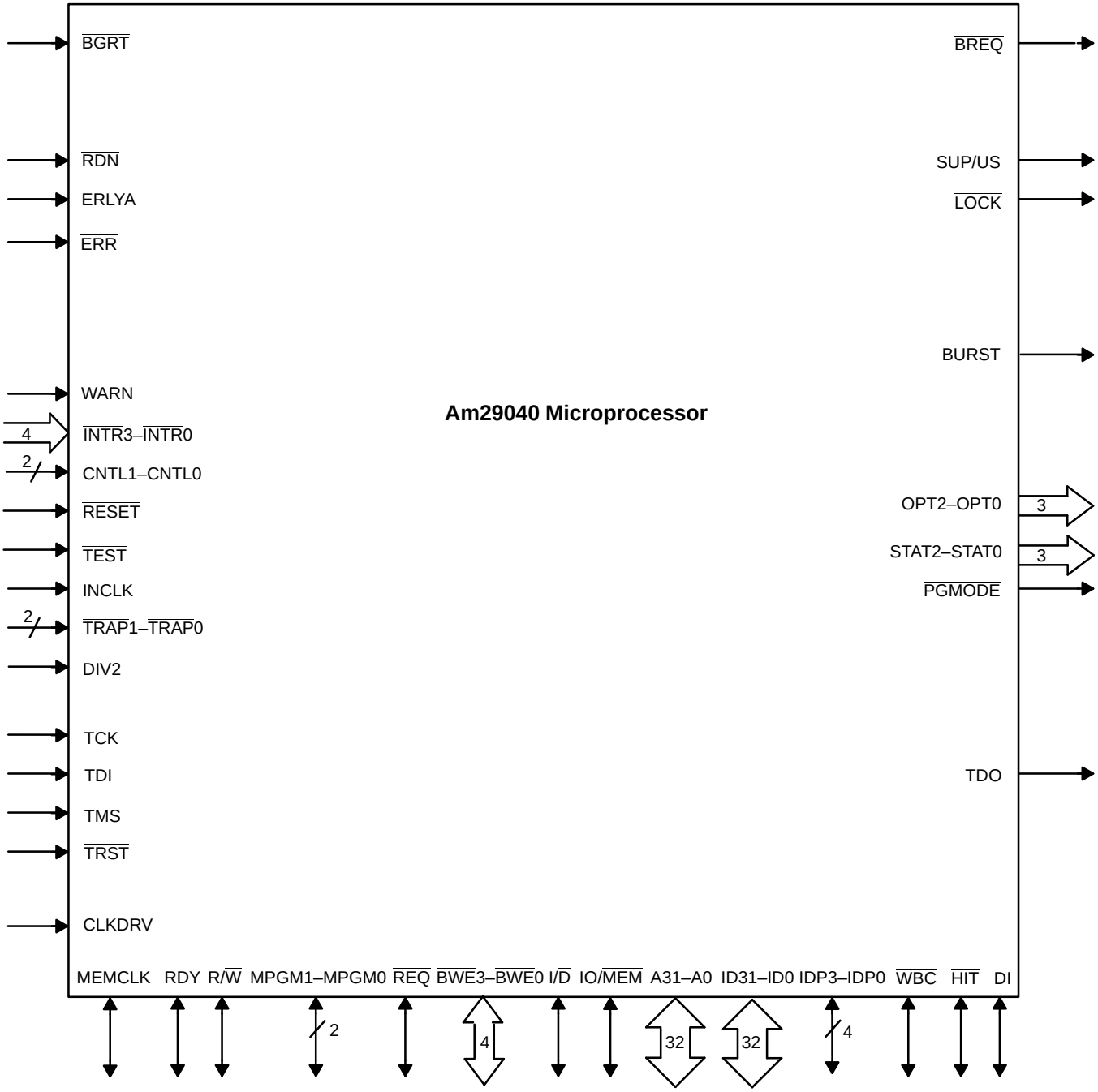
PQFP PIN DESIGNATIONS
(Sorted by Pin Number)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	**37**	V_{CC}	**73**	V_{CC}	**109**	A1
2	GND	**38**	GND	**74**	GND	**110**	A0
3	No Connect	**39**	ID5	**75**	A29	**111**	$\overline{\text{ERLYA}}$
4	STAT2	**40**	ID6	**76**	A28	**112**	$\overline{\text{ERR}}$
5	STAT1	**41**	ID7	**77**	A27	**113**	$\overline{\text{RDN}}$
6	STAT0	**42**	ID8	**78**	A26	**114**	$\overline{\text{RDY}}$
7	MPGM1	**43**	ID9	**79**	A25	**115**	$\overline{\text{BGRT}}$
8	MPGM0	**44**	ID10	**80**	A24	**116**	GND
9	OPT2	**45**	ID11	**81**	A23	**117**	V_{CC}
10	OPT1	**46**	ID12	**82**	A22	**118**	$\overline{\text{PGMODE}}$
11	OPT0	**47**	ID13	**83**	A21	**119**	$\overline{\text{BURST}}$
12	$\overline{\text{LOCK}}$	**48**	ID14	**84**	A20	**120**	$\overline{\text{REQ}}$
13	SUP/$\overline{\text{US}}$	**49**	ID15	**85**	A19	**121**	$\overline{\text{BREQ}}$
14	$\overline{\text{BWE}}$3	**50**	V_{CC}	**86**	A18	**122**	GND
15	$\overline{\text{BWE}}$2	**51**	GND	**87**	A17	**123**	INCLK
16	$\overline{\text{BWE}}$1	**52**	ID16	**88**	A16	**124**	V_{CC}
17	$\overline{\text{BWE}}$0	**53**	ID17	**89**	IDP2	**125**	CLKDRV
18	V_{CC}	**54**	ID18	**90**	GND	**126**	MEMCLK
19	GND	**55**	ID19	**91**	V_{CC}	**127**	GND
20	$\overline{\text{WARN}}$	**56**	ID20	**92**	IDP3	**128**	V_{CC}
21	IO/$\overline{\text{MEM}}$	**57**	ID21	**93**	A15	**129**	IDP0
22	I/$\overline{\text{D}}$	**58**	ID22	**94**	A14	**130**	$\overline{\text{DIV2}}$
23	GND	**59**	ID23	**95**	A13	**131**	CNTL0
24	V_{CC}	**60**	GND	**96**	A12	**132**	CNTL1
25	R/$\overline{\text{W}}$	**61**	V_{CC}	**97**	A11	**133**	V_{CC}
26	$\overline{\text{TEST}}$	**62**	IDP1	**98**	A10	**134**	GND
27	TCK	**63**	ID24	**99**	A9	**135**	$\overline{\text{RESET}}$
28	TMS	**64**	ID25	**100**	A8	**136**	$\overline{\text{TRAP}}$0
29	TDI	**65**	ID26	**101**	A7	**137**	$\overline{\text{TRAP}}$1
30	TDO	**66**	ID27	**102**	A6	**138**	$\overline{\text{INTR}}$3
31	$\overline{\text{TRST}}$	**67**	ID28	**103**	A5	**139**	$\overline{\text{INTR}}$2
32	ID0	**68**	ID29	**104**	A4	**140**	$\overline{\text{INTR}}$1
33	ID1	**69**	ID30	**105**	A3	**141**	$\overline{\text{INTR}}$0
34	ID2	**70**	ID31	**106**	A2	**142**	$\overline{\text{DI}}$
35	ID3	**71**	A31	**107**	GND	**143**	$\overline{\text{HIT}}$
36	ID4	**72**	A30	**108**	V_{CC}	**144**	$\overline{\text{WBC}}$

PQFP PIN DESIGNATIONS
(Sorted by Pin Name)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A0	110	$\overline{\text{BWE1}}$	16	ID11	45	OPT0	11
A1	109	$\overline{\text{BWE2}}$	15	ID12	46	OPT1	10
A2	106	$\overline{\text{BWE3}}$	14	ID13	47	OPT2	9
A3	105	CLKDRV	125	ID14	48	$\overline{\text{PGMODE}}$	118
A4	104	CNTL0	131	ID15	49	$\overline{\text{RDN}}$	113
A5	103	CNTL1	132	ID16	52	$\overline{\text{RDY}}$	114
A6	102	$\overline{\text{DI}}$	142	ID17	53	$\overline{\text{RESET}}$	135
A7	101	$\overline{\text{DIV2}}$	130	ID18	54	$\overline{\text{REQ}}$	120
A8	100	$\overline{\text{ERLYA}}$	111	ID19	55	R/$\overline{\text{W}}$	25
A9	99	$\overline{\text{ERR}}$	112	ID20	56	STAT0	6
A10	98	GND	2	ID21	57	STAT1	5
A11	97	GND	19	ID22	58	STAT2	4
A12	96	GND	23	ID23	59	SUP/$\overline{\text{US}}$	13
A13	95	GND	38	ID24	63	TCK	27
A14	94	GND	51	ID25	64	TDI	29
A15	93	GND	60	ID26	65	TDO	30
A16	88	GND	74	ID27	66	$\overline{\text{TEST}}$	26
A17	87	GND	90	ID28	67	TMS	28
A18	86	GND	107	ID29	68	$\overline{\text{TRAP0}}$	136
A19	85	GND	116	ID30	69	$\overline{\text{TRAP1}}$	137
A20	84	GND	122	ID31	70	$\overline{\text{TRST}}$	31
A21	83	GND	127	IDP0	129	V_{CC}	1
A22	82	GND	134	IDP1	62	V_{CC}	18
A23	81	$\overline{\text{HIT}}$	143	IDP2	89	V_{CC}	24
A24	80	I/$\overline{\text{D}}$	22	IDP3	92	V_{CC}	37
A25	79	ID0	32	INCLK	123	V_{CC}	50
A26	78	ID1	33	$\overline{\text{INTR0}}$	141	V_{CC}	61
A27	77	ID2	34	$\overline{\text{INTR1}}$	140	V_{CC}	73
A28	76	ID3	35	$\overline{\text{INTR2}}$	139	V_{CC}	91
A29	75	ID4	36	$\overline{\text{INTR3}}$	138	V_{CC}	108
A30	72	ID5	39	IO/$\overline{\text{MEM}}$	21	V_{CC}	117
A31	71	ID6	40	$\overline{\text{LOCK}}$	12	V_{CC}	124
$\overline{\text{BGRT}}$	115	ID7	41	MEMCLK	126	V_{CC}	128
$\overline{\text{BREQ}}$	121	ID8	42	MPGM0	8	V_{CC}	133
$\overline{\text{BURST}}$	119	ID9	43	MPGM1	7	$\overline{\text{WARN}}$	20
$\overline{\text{BWE0}}$	17	ID10	44	No Connect	3	$\overline{\text{WBC}}$	144

LOGIC SYMBOL



PIN DESCRIPTIONS

Note: Certain outputs are described in the following section as being three-state or bidirectional. However, all outputs can be placed in a high-impedance state by the Test mode. The three-state and bidirectional terminology in this section is for those outputs that are disabled when an external device is granted the bus.

A31–A0

Address Bus (bidirectional, synchronous)

The address bus transfers the byte address for all accesses, including burst-mode accesses.

$\overline{\text{BREQ}}$

Bus Request (output, synchronous)

This output indicates that the processor needs to perform an external access.

$\overline{\text{BGRT}}$

Bus Grant (input, synchronous)

This input signals the processor that it has control of the external bus. This signal can be asserted even when $\overline{\text{BREQ}}$ is not active, in which case the processor still has control of the bus. The processor drives $\overline{\text{REQ}}$ High when granted an unrequested bus.

$\overline{\text{BWE}}$3–$\overline{\text{BWE}}$0

Byte Write Enables (bidirectional, synchronous)

These signals are asserted during an external write to indicate which bytes should be written. An assertion of $\overline{\text{BWE}}$3 indicates that the most significant byte (corresponding to ID31–ID24) should be written, and so on.

$\overline{\text{BURST}}$

Burst Request (three-state output, synchronous)

This signal indicates a burst-mode access. The addresses for burst-mode accesses appear on the address bus. The $\overline{\text{BURST}}$ signal is provided to aid the implementation of high-bandwidth transfers by informing the external system that the processor can complete an access as often as every cycle after the first cycle.

CLKDRV

Enable MEMCLK Drive (input)

This pin determines whether MEMCLK is an output (CLKDRV High) or an input (CLKDRV Low). The CLKDRV pin is the same physical pin as PWRCLK on the Am29030 microprocessor, and it performs the same function as PWRCLK except that it is a logic pin rather than a power-supply pin.

CNTL1–CNTL0

CPU Control (inputs, asynchronous)

These inputs specify the processor mode: Load Test Instruction, Step, Halt, or Normal.

$\overline{\text{DI}}$

Data Intervention (bidirectional, synchronous)

This output is driven by a bus slave that is the owner of data being requested by the bus master. Because it is asserted on a read of cacheable data, and because the data cache is block-oriented, the intervening device drives an entire block of data.

$\overline{\text{DIV2}}$

Divide Clock By 2 (input)

On the Am29040 microprocessor, MEMCLK is used as the frequency reference for the processor and is always half of INCLK. If $\overline{\text{DIV2}}$ is High, the processor's operating frequency is the same as the MEMCLK frequency. If $\overline{\text{DIV2}}$ is Low, the processor's operating frequency is double the MEMCLK frequency. Note that $\overline{\text{DIV2}}$ on the Am29040 microprocessor operates differently than $\overline{\text{DIV2}}$ on the Am29030 microprocessor, since the clocking scheme is different.

$\overline{\text{ERLYA}}$

Early Address (input, synchronous)

The $\overline{\text{ERLYA}}$ input is used to request the early transmission of burst-mode addresses for interleaved memories. Note that this functionality is different from how $\overline{\text{ERLYA}}$ operates on the Am29030 microprocessor.

$\overline{\text{ERR}}$

Error (input, synchronous)

This input indicates that an error occurred during the current access. For a read, the processor ignores the instruction/data bus. For a store, the access is terminated. In either case, a Data Access Exception or Instruction Access Exception trap can occur. The processor ignores this signal if there is no pending access. This signal cannot end an access; it is sampled only when the $\overline{\text{RDY}}$ input is active.

$\overline{\text{HIT}}$

Hit (bidirectional, synchronous)

This output is driven by a bus slave to indicate that the slave has a cached copy of the data. It is driven for any access—read or write—that hits in the slave's data cache.

I/$\overline{\text{D}}$

Instruction or Data Access (bidirectional, synchronous)

This signal is High during an access to indicate that the access is for an instruction or Low to indicate that the access is for data.

ID31–ID0

Instruction/Data Bus (bidirectional, synchronous)

The instruction/data bus transfers instructions to, and data to and from, the processor.

IDP3–IDP0

Instruction/Data Bus Parity (bidirectional, synchronous)

These are byte parity bits for the instruction/data bus. IDP3 is the parity bit for ID31–24, IDP2 is the parity bit for ID 23–16, IDP1 is the parity bit for ID15–ID8, and IPD0 is the parity bit for ID7–ID0. If parity checking is enabled, the processor drives IDP3–IDP0 with valid parity during writes and expects IDP3–IDP0 to be driven with valid parity during reads of either instructions or data.

INCLK

Input Clock (input)

This is an oscillator input at twice the MEMCLK frequency. It is used only to generate MEMCLK, and is used only if MEMCLK is an output. If MEMCLK is an input, INCLK is unused and can be left disconnected. Note that INCLK on the Am29040 microprocessor operates differently than INCLK on the Am29030 microprocessor.

$\overline{\text{INTR3}}$–$\overline{\text{INTR0}}$

Interrupt Requests (inputs, asynchronous)

These inputs generate prioritized interrupt requests. The interrupt caused by $\overline{\text{INTR0}}$ has the highest priority, and the interrupt caused by $\overline{\text{INTR3}}$ has the lowest priority. The interrupt requests are masked in prioritized order by the Interrupt Mask field in the Current Processor Status Register.

IO/$\overline{\text{MEM}}$

Input/Output or Memory Access (bidirectional, synchronous)

For a data access, this signal indicates whether the access is to the input/output (I/O) address space (High) or the instruction/data memory address space (Low).

$\overline{\text{LOCK}}$

Lock (three-state output, synchronous)

This output allows the implementation of various bus and device interlocks. It can be active only for the duration of an access or for an extended period of time under control of the Lock bit in the Current Processor Status Register. The processor does not relinquish the bus (in response to $\overline{\text{BGRT}}$) when $\overline{\text{LOCK}}$ is active.

MEMCLK

Memory Clock (input/output)

MEMCLK is either a clock output or an input from an external clock generator, as determined by the CLKDRV pin.

MEMCLK is used as the frequency reference for the processor. Note that MEMCLK on the Am29040 microprocessor operates differently than MEMCLK on the Am29030 microprocessor.

If the $\overline{\text{DIV2}}$ pin is High, the processor frequency is the frequency of MEMCLK. If $\overline{\text{DIV2}}$ is Low, the processor frequency is twice the frequency of MEMCLK and is achieved by frequency doubling.

MPGM1–MPGM0

MMU Programmable (bidirectional, synchronous)

These outputs reflect the value of the two PGM bits in the Translation Look-Aside Buffer entry associated with the access. If no address translation is performed, these signals are both Low.

OPT2–OPT0

Option Control (three-state outputs, synchronous)

These outputs reflect the value of the OPT field of load and store instructions.

$\overline{\text{PGMODE}}$

Page-Mode Access (three-state output, synchronous)

This indicates that the address for an access is in the same page-mode block as the address for the previous access.

$\overline{\text{RDN}}$

Read Narrow (input, synchronous)

This input indicates that the accessed memory is an 8- or 16-bit device attached to ID31–ID24 or to ID31–ID16, respectively. This signal can be asserted for any read access—though it is probably most useful for ROM accesses—and causes the processor to perform additional read accesses to obtain the remainder of a word or half-word, if required. This signal is ignored on a write access.

The $\overline{\text{RDN}}$ signal is sampled when $\overline{\text{RESET}}$ is asserted. The level of $\overline{\text{RDN}}$ during the four cycles before the deassertion of $\overline{\text{RESET}}$ determines whether a narrow access is 8 or 16 bits wide. If $\overline{\text{RDN}}$ is Low in each of these cycles, a narrow access is 16 bits wide. If $\overline{\text{RDN}}$ is High, a narrow access is 8 bits wide. The width of the narrow access is undefined if $\overline{\text{RDN}}$ changes in the four cycles before $\overline{\text{RESET}}$ is deasserted.

$\overline{\text{RDY}}$

Ready (bidirectional, synchronous)

For a read, this input indicates that a valid instruction or data word is on the instruction/data bus. For a write, it indicates that the write is complete and that the data no longer needs to be driven on the instruction/data bus. The processor ignores this signal for the first cycle of a

simple access and for the first cycle of a burst-mode access (all other burst-mode cycles are not subject to this restriction).

$\overline{\text{REQ}}$

Request (bidirectional, synchronous)

This signal requests an access. When $\overline{\text{REQ}}$ is Low, the address for the access appears on the address bus. This signal is precharged and then maintained by a weak internal pullup when the bus is granted to another master, to prevent spurious requests.

$\overline{\text{RESET}}$

Reset (input, asynchronous)

This input places the processor in the Reset mode.

R/$\overline{\text{W}}$

Read/Write (bidirectional, synchronous)

This signal indicates whether data is being transferred from the processor to the external system (Low), or from the external system to the processor (High).

STAT2–STAT0

CPU Status (outputs, synchronous)

These outputs indicate the state of the processor's execution stage on the previous cycle.

SUP/$\overline{\text{US}}$

Supervisor/User Mode (three-state output, synchronous)

This output indicates the program mode for an access. If the access is performed under Supervisor mode, SUP/$\overline{\text{US}}$ is High. If the access is performed under User mode, SUP/$\overline{\text{US}}$ is Low.

$\overline{\text{TEST}}$

Test Mode (input, asynchronous)

When this input is active, the processor is in Test mode. All outputs and bidirectional lines are forced to the high-impedance state.

$\overline{\text{TRAP}}$1–$\overline{\text{TRAP}}$0

Trap Requests (inputs, asynchronous)

These inputs generate prioritized trap requests. The trap caused by $\overline{\text{TRAP}}$0 has the highest priority.

$\overline{\text{WARN}}$

Warn (input, asynchronous, edge-sensitive)

A High-to-Low transition on this input causes a non-maskable $\overline{\text{WARN}}$ trap to occur. This trap bypasses the normal trap vector fetch sequence and is useful in situations where the vector fetch might not work (e.g., when data memory is faulty).

$\overline{\text{WBC}}$

Write Broadcast (bidirectional, synchronous)

This output is asserted by a bus master to indicate a write broadcast. A write broadcast is performed to notify other agents of a modification to a shared cache block. The write need not be performed in the main memory.

JTAG INTERFACE PINS

The following pins are included as part of the IEEE 1149.1–1990 compliant Standard Test Access Port.

TCK

Test Clock Input (input, asynchronous)

This input clocks the Test Access Port.

TDI

Test Data Input (input, synchronous to TCK)

This signal supplies data to the test logic from an external source. It is sampled on the rising edge of TCK.

TDO

Test Data Output (three-state output, synchronous to TCK)

This output supplies data from the test logic to an external destination. It changes on the falling edge of TCK.

TMS

Test Mode Select (input, synchronous to TCK)

This input controls the operation of the Test Access Port.

$\overline{\text{TRST}}$

Test Reset Input (input, asynchronous)

This input asynchronously resets the Test Access Port. The reset places the test logic in a state such that it does not cause an output driver to be enabled. The $\overline{\text{TRST}}$ input must be asserted in conjunction with the $\overline{\text{RESET}}$ input for correct processor initialization.

SPECIAL PINS

$\overline{\text{EMACC}}$

Emulator Access (output, synchronous)

The $\overline{\text{EMACC}}$ pin is defined for use with hardware development systems (emulators). This pin does not exist on any package, and this definition is provided solely for the purposes of standardizing its location.

The $\overline{\text{EMACC}}$ output indicates the current access is generated by an emulator. If $\overline{\text{EMACC}}$ is Low, the access is emulator specific and the external system must not respond to the access. If $\overline{\text{EMACC}}$ is High, the access is directed to the external system.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C
Voltage on any Pin
with Respect to GND . . . . . –0.5 to 5.5 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C) . . . . . 0°C to +85°C
Supply Voltage (V_{CC}) . . . . . +3.0 to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL Operating Range

Parameter Symbol	Parameter Description	Test Conditions	Preliminary		
			Min	Max	Unit
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	5.5	V
$V_{ILINCLK}$	INCLK Input Low Voltage		–0.5	0.8	V
$V_{IHINCLK}$	INCLK Input High Voltage		2.0	5.5	V
$V_{ILMEMCLK}$	MEMCLK Input Low Voltage		–0.5	0.8	V
$V_{IHMEMCLK}$	MEMCLK Input High Voltage		V_{CC} –0.8	5.5	V
V_{OL}	Output Low Voltage for all outputs except MEMCLK	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage for all outputs except MEMCLK	I_{OH} = –400 µA	2.4		V
I_{LI}	Input Leakage Current	0.45 V ≤ V_{IN} ≤ V_{CC} –0.45 V		±10	µA
I_{LO}	Output Leakage Current	0.45 V ≤ V_{OUT} ≤ V_{CC} –0.4 V		±10	µA
I_{CCOP}	Operating Power Supply Current	Outputs Floating; Holding $\overline{RESET}$ active with externally supplied MEMCLK. V_{CC} = 3.3 V		10	mA/MHz
V_{OLC}	MEMCLK Output Low Voltage	I_{OLC} = 20 mA		0.6	V
V_{OHC}	MEMCLK Output High Voltage	I_{OHC} = –20 mA	V_{CC} –0.6		V
I_{OSGND}	MEMCLK GND Short Circuit Current	V_{CC} = 3.3 V	60		mA
I_{OSVCC}	MEMCLK V_{CC} Short Circuit Current	V_{CC} = 3.3 V	60		mA
I_{CCSTB}	Standby Power Supply Current	Snooze mode Sleep mode		20 5	mA

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Preliminary		
			Min	Max	Unit
C_{IN}	Input Capacitance	fC = 10 MHz		15	pF
C_{INCLK}	INCLK Input Capacitance			20	pF
C_{MEMCLK}	MEMCLK Capacitance			20	pF
C_{OUT}	Output Capacitance			20	pF
$C_{I/O}$	I/O Pin Capacitance			20	pF

Note:

Limits guaranteed by characterization.

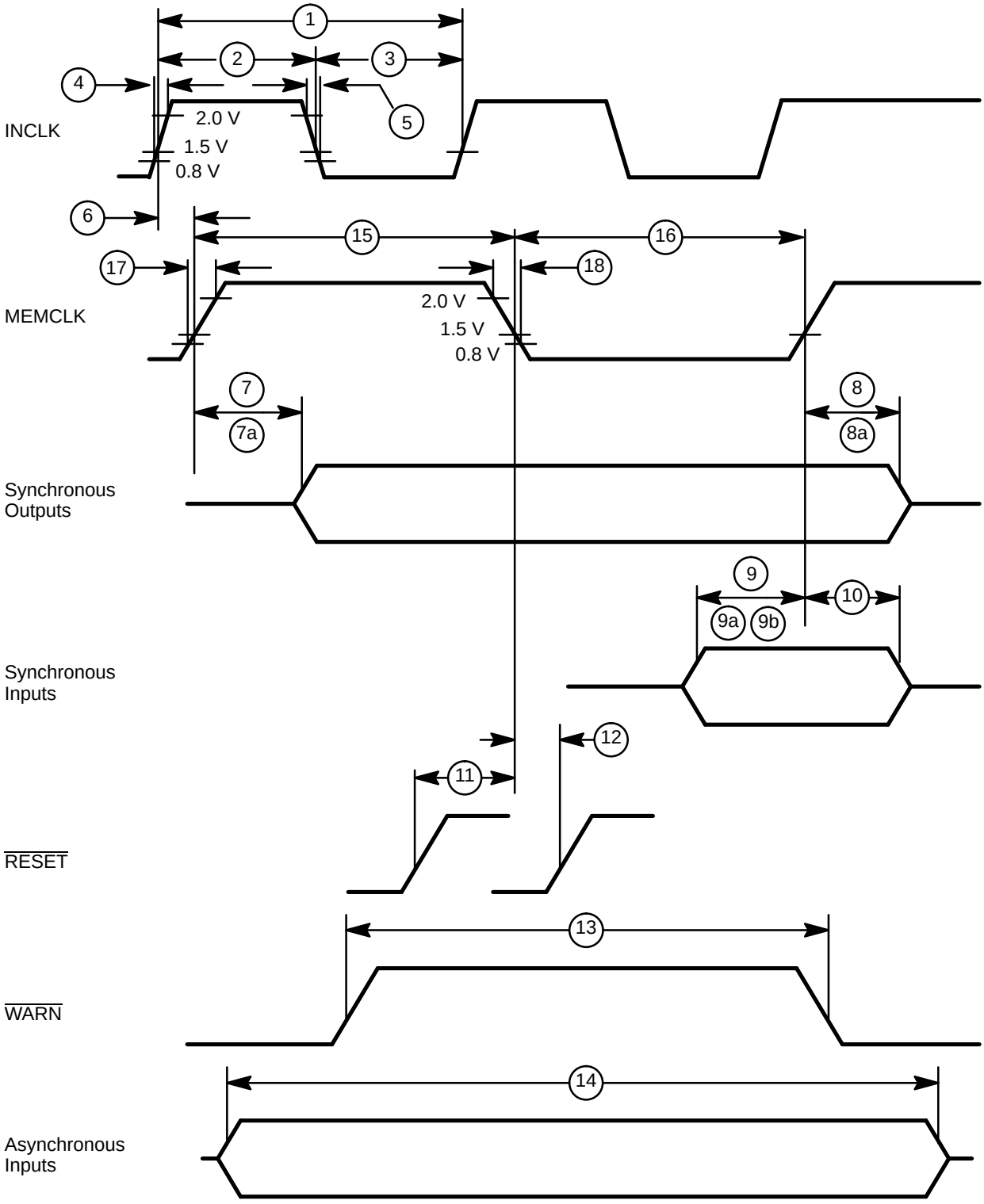
SWITCHING CHARACTERISTICS over COMMERCIAL Operating Range

No.	Parameter Description	Test Conditions (Note 1)	Preliminary						Unit
			50MHz [2]		40 MHz [2]		33 MHz [2]		
			Min	Max	Min	Max	Min	Max	
1	INCLK Period (T) (Normal Operation)	Notes 2, 7	20	50	25	50	15	25	ns
2	INCLK High Time (Maximum Frequency)		7	13	9	16	5	10	ns
3	INCLK Low Time (Maximum Frequency)		7	13	9	16	5	10	ns
4	INCLK Rise Time		0	3	0	4	0	6	ns
5	INCLK Fall Time		0	3	0	4	0	6	ns
6	MEMCLK Delay from INCLK	Notes 3, 4	0	6	0	7	0	6	ns
7	Synchronous Output Valid Delay	Note 6	1	12	1	14	1	12	ns
7a	Synchronous Output Valid Delay for ID31–ID0	Note 6	1	16	1	18	1	16	ns
8	Synchronous Output Invalid Delay		1	12	1	14	1	12	ns
8a	Synchronous Output Invalid Delay for ID31–ID0		1	16	1	18	1	16	ns
9	Synchronous Input Setup Time		12		14		12		ns
9a	Synchronous Input Setup Time for ID31–ID0		6		8		6		ns
9b	Synchronous Input Setup Time for $\overline{RDY}$, $\overline{ERR}$, and $\overline{RDN}$		16		16		16		ns
10	Synchronous Input Hold Time		0		0		0		ns
11	Setup Time for Synchronous $\overline{RESET}$ Deassertion			2		2		2	ns
12	Hold Time for Synchronous $\overline{RESET}$ Deassertion			5		5		5	ns
13	$\overline{WARN}$ High Time	Note 5	4T		4T		4T		ns
14	Asynchronous Input Pulse Width	Note 5	T + 10		T + 10		T + 10		ns
15	MEMCLK High Time (Note 5)	MEMCLK Input MEMCLK Output	14 T/2 – 3	26 T/2 + 3	18 T/2 – 3	32 T/2 + 3	11 T/2 – 3	19 T/2 + 3	ns
16	MEMCLK Low Time (Note 5)	MEMCLK Input MEMCLK Output	14 T/2 – 3	26 T/2 + 3	18 T/2 – 3	32 T/2 + 3	11 T/2 – 3	19 T/2 + 3	ns
17	MEMCLK Rise Time	MEMCLK Input MEMCLK Output	0 0	5 5	0 0	5 5	0 0	5 5	ns
18	MEMCLK Fall Time	MEMCLK Input MEMCLK Output	0 0	5 5	0 0	5 5	0 0	5 5	ns

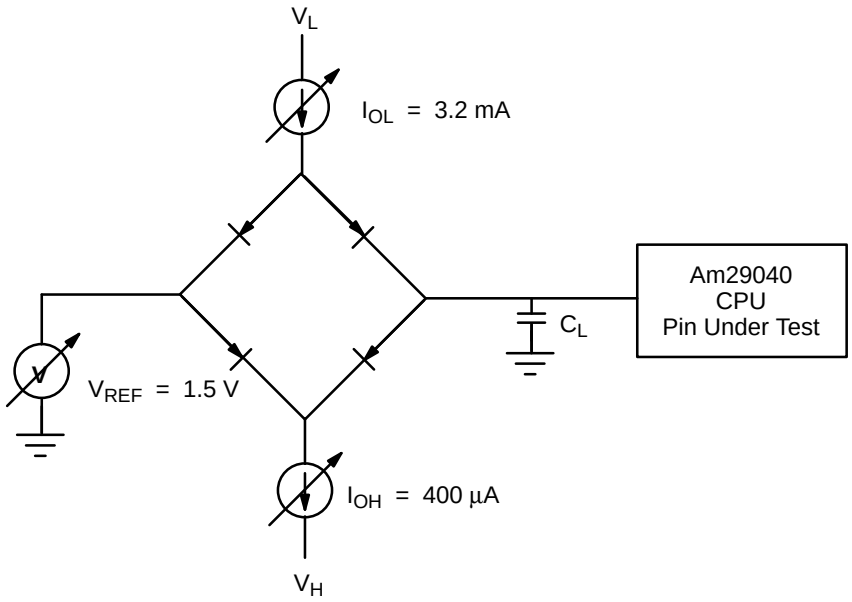
Notes:

1. *Test conditions: All inputs/outputs are TTL compatible for V_{IH}, V_{IL}, V_{OH}, and V_{OL} unless otherwise noted. All output timing specifications are for 80 pF of loading. All setup, hold, and delay times are measured relative to MEMCLK unless otherwise noted. All input Low levels must be driven to 0.45 V and all input High levels must be driven to 2.4 V except INCLK.*
2. *Maximum bus frequency is 25 MHz for a 50-MHz processor (T=40 ns), 20 MHz for a 40-MHz processor (T=50 ns), and 33 MHz for a 33-MHz processor (T=30 ns).*
3. *MEMCLK as an input is always at CMOS levels.*
4. *MEMCLK can drive an external load of 100 pF.*
5. *The parameter T is the actual period of MEMCLK, regardless of the processor frequency rating.*
6. *All output valid delays are measured with V_{OL}=1.0 V and V_{OH}=2.0 V.*
7. *Does not apply to Snooze or Sleep modes.*

SWITCHING WAVEFORMS



SWITCHING TEST CIRCUIT



Note:
C_L is guaranteed to 80 pF.

THERMAL CHARACTERISTICS

The Am29040 microprocessor is specified for operation with case temperature ranges for a commercial temperature device. Case temperature is measured at the top center of the package as shown in Figure 2.

The various temperatures and thermal resistances can be determined using the equations shown in Figure 3 along with information given in Table 1. (The variable *P* is power in watts.)

Allowable ambient temperature curves for various airflows are given in Figure 4 through Figure 6. These graphs assume a maximum V_{CC} and a maximum power supply current equal to I_{CCOP}. All calculations made using this information should guarantee that the operating case temperature does not exceed the maximum case temperature. Since P is a function of operating frequency, calculations can also be made to determine the ambient temperature at various operating speeds.

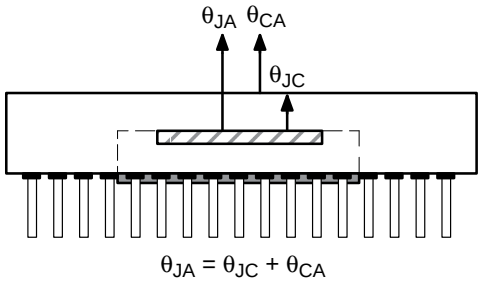


Figure 1. PGA Package Thermal Resistance — °C/Watt

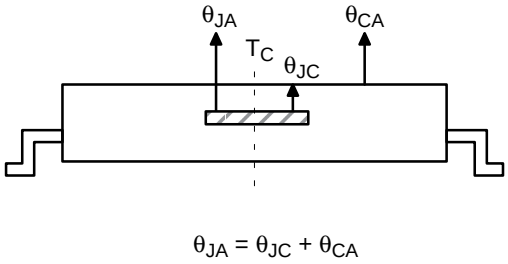


Figure 2. PQFP Package Thermal Resistance — °C/Watt

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$
$$P = I_{CCOP} \cdot freq \cdot V_{CC}$$
$$T_J = T_C + P \cdot \theta_{JC}$$
$$T_J = T_A + P \cdot \theta_{JA}$$
$$T_C = T_J - P \cdot \theta_{JC}$$
$$T_C = T_A + P \cdot \theta_{CA}$$
$$T_A = T_J - P \cdot \theta_{JA}$$
$$T_A = T_C - P \cdot \theta_{CA}$$

Figure 3. Thermal Characteristics Equations

Table 1. Thermal Characteristics (°C/Watt) Surface Mounted

		Airflow—ft./min. (m/s)				
PGA Package		**0 (0)**	**200 (1.01)**	**400 (2.03)**	**600 (3.04)**	**800 (4.06)**
θ_{JA}	Junction-to-Ambient	24	20	15	13	11
θ_{JC1}	Junction-to-Case	2	2	2	2	2
θ_{CA}	Case-to-Ambient	22	18	13	11	9
PQFP Package						
θ_{JA}	Junction-to-Ambient	36	28	25	23	21
θ_{JC}	Junction-to-Case	6.5	6.5	6.5	6.5	6.5
θ_{CA}	Case-to-Ambient	29.5	21.5	18.5	16.5	14.5

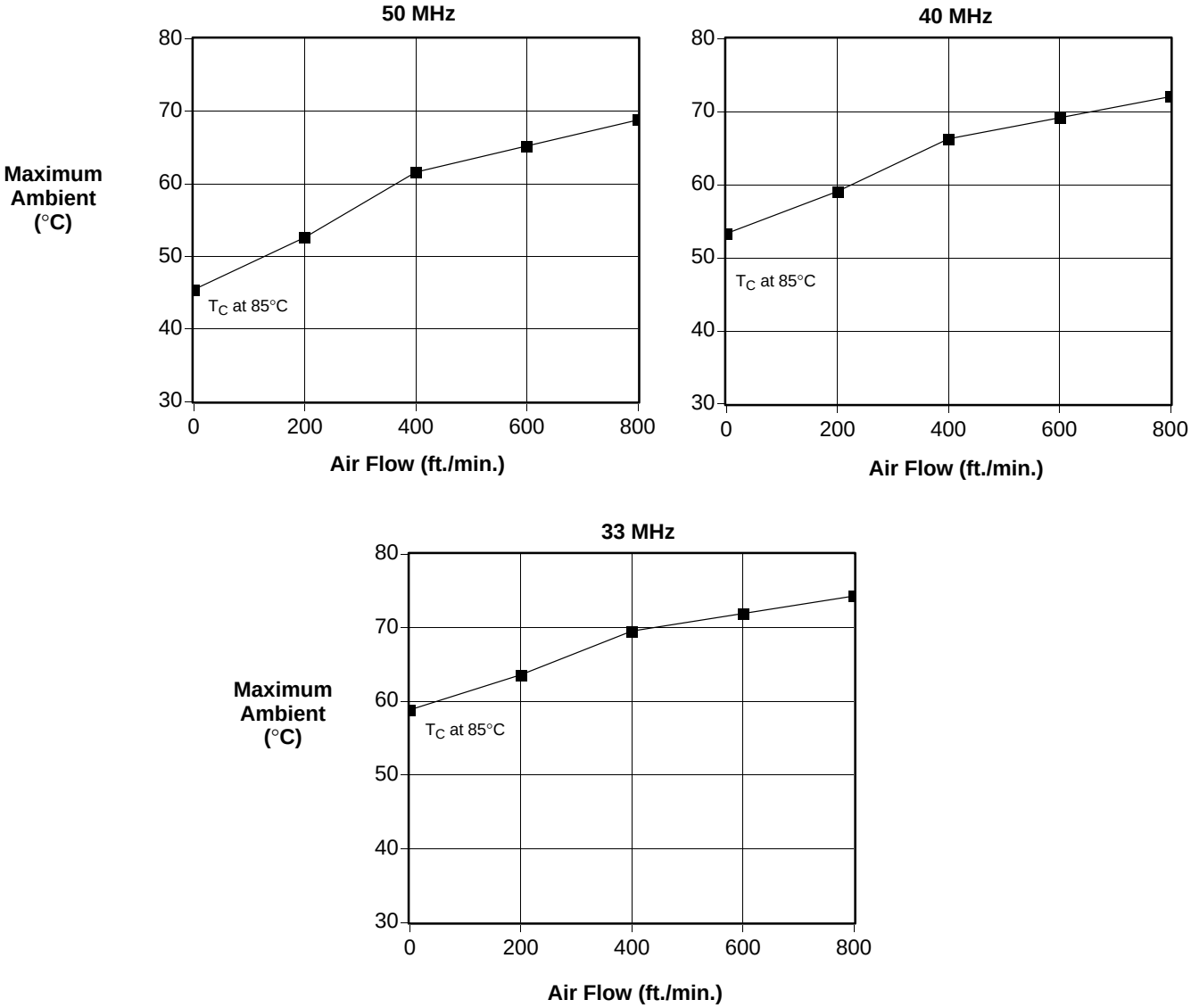


Figure 4. PGA Package—Maximum Allowable Ambient Temperature
(Data Sheet Limit, $I_{CCOPmax}$, V_{CC}=+3.6 V, Average Thermal Impedance)

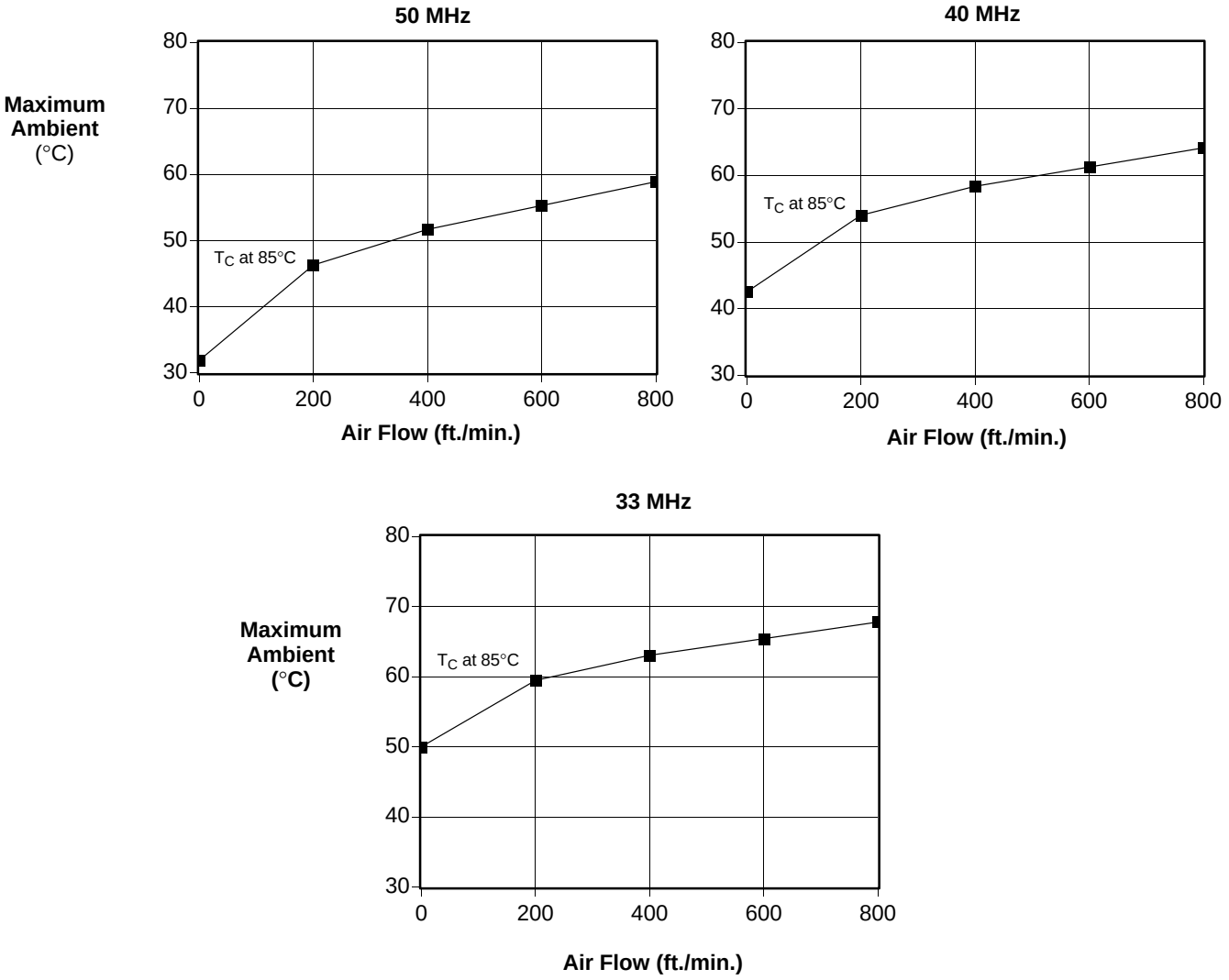


Figure 5. PQFP Package—Maximum Allowable Ambient Temperature
(Data Sheet Limit, $I_{CCOPmax}$, V_{CC}=+3.6 V, Average Thermal Impedance)

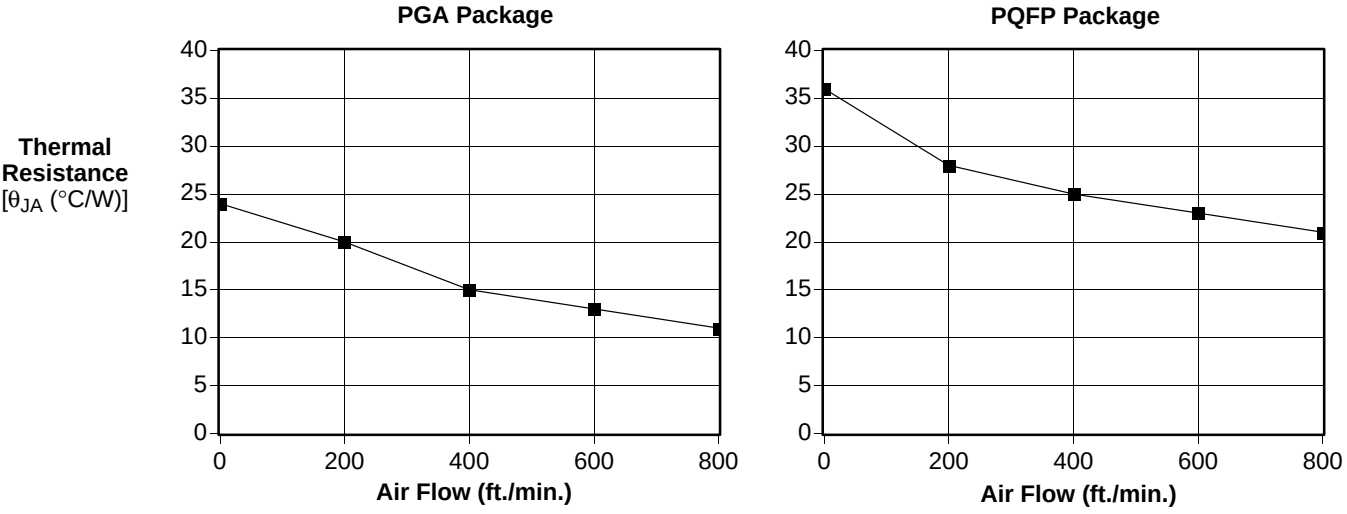
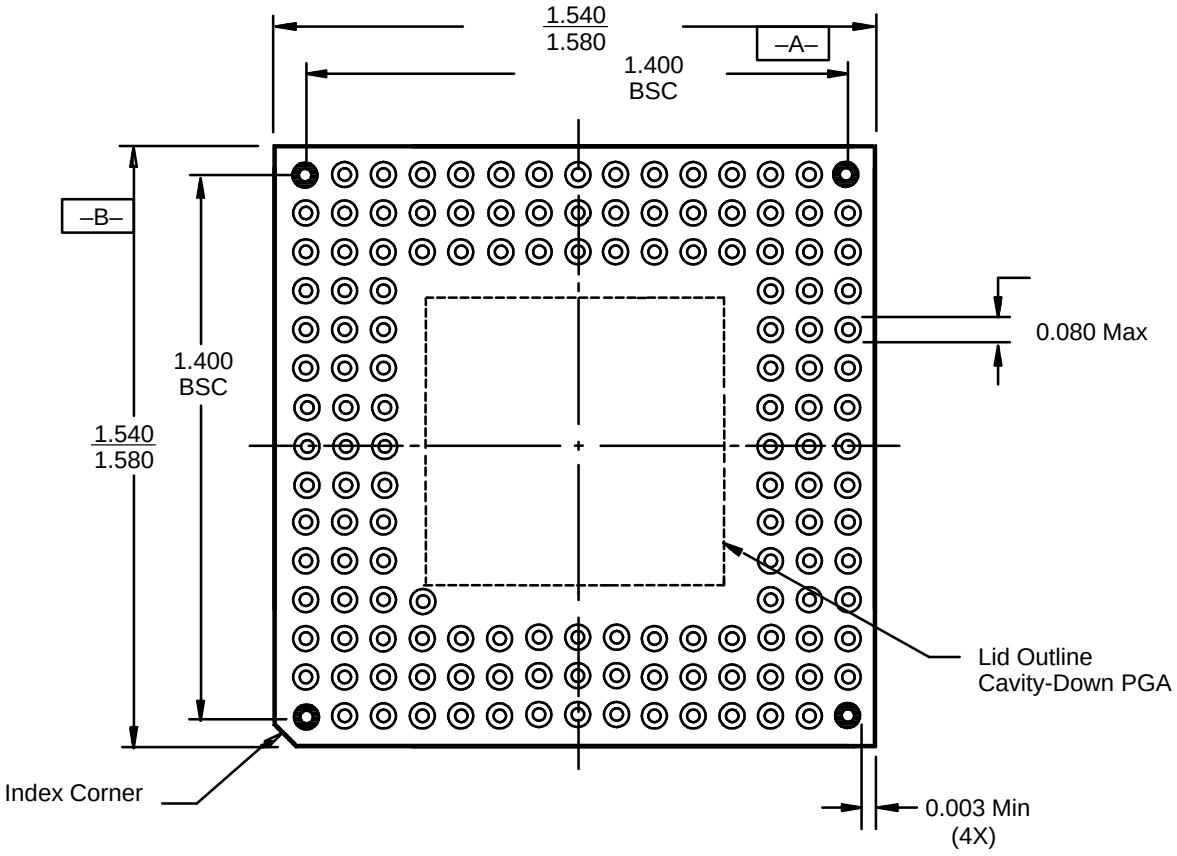


Figure 6. Thermal Impedance

PHYSICAL DIMENSIONS
CGM 145
Pin Grid Array



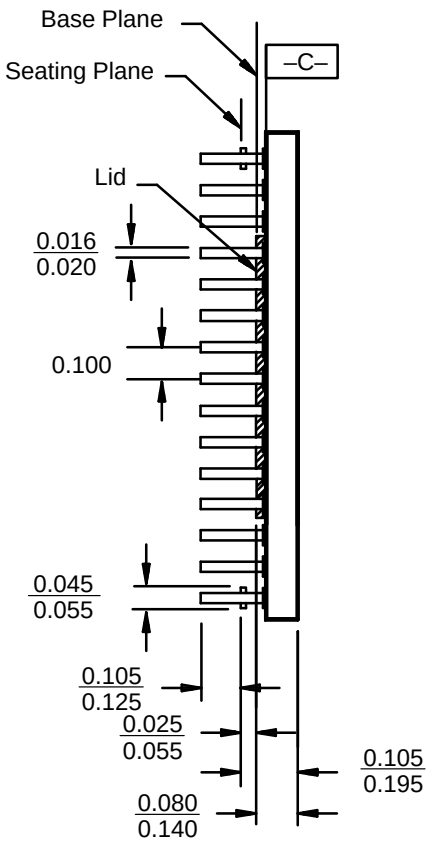
Bottom View

cgm145
5–30–95

Notes:

All dimensions are in inches unless otherwise noted. BSC is an ANSI standard for Basic Space Centering.
Not to scale. For reference only.

CGM 145 (continued)



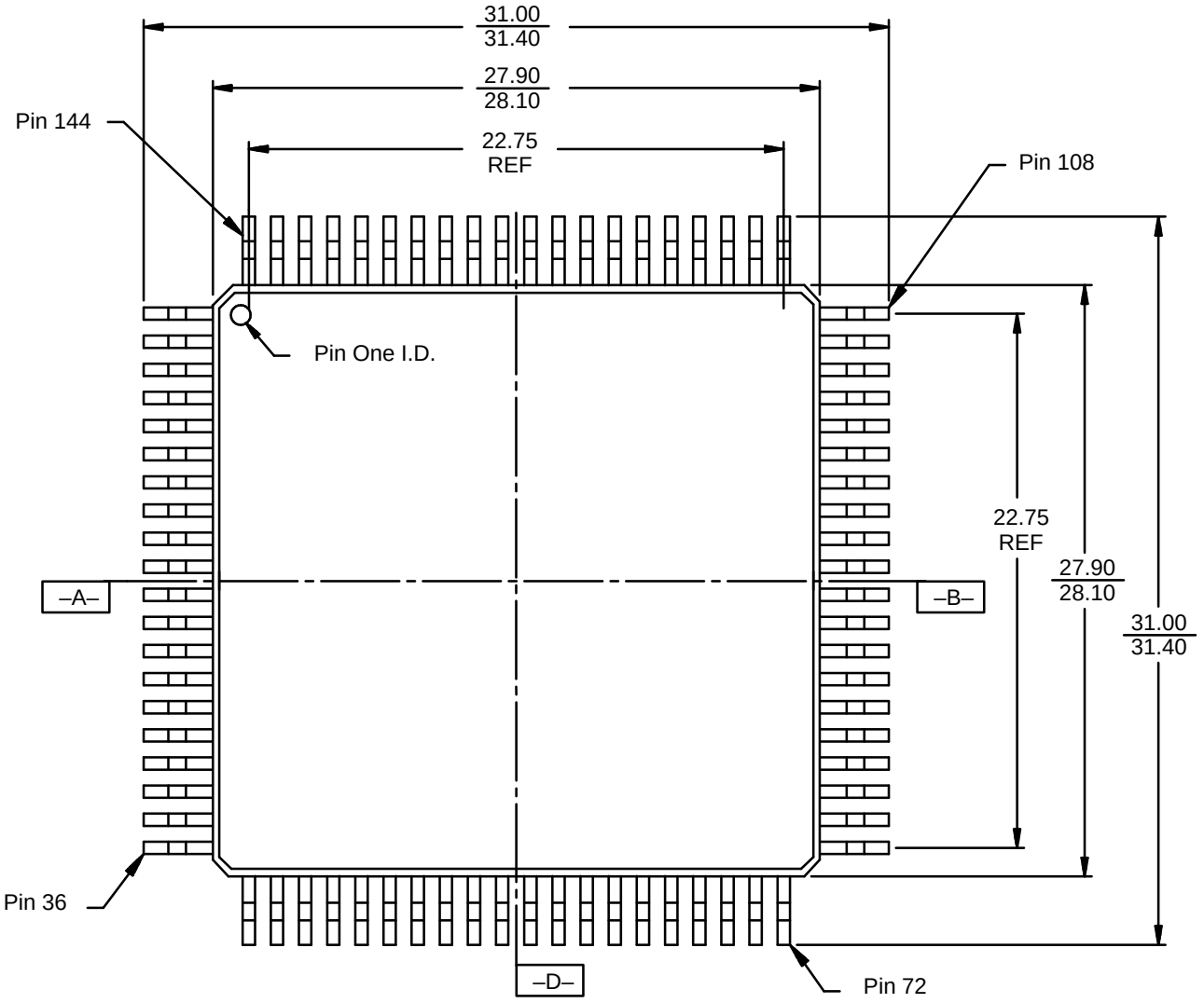
Side View

cgm145
5–30–95

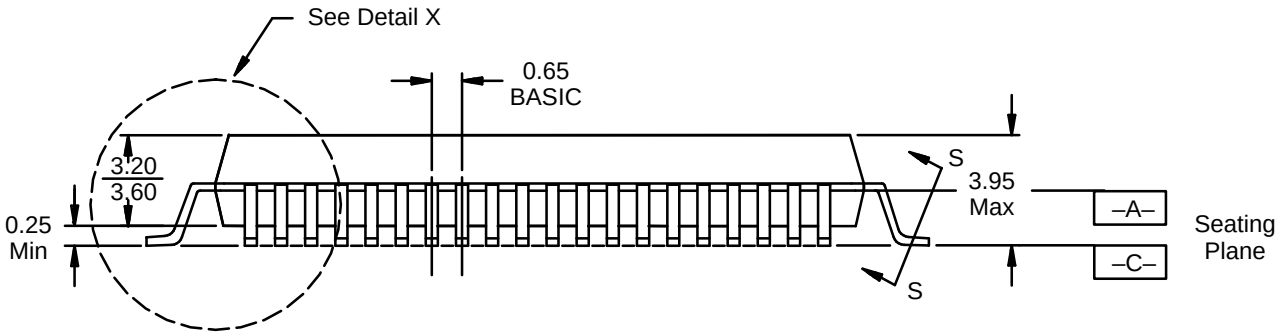
Notes:

All dimensions are in inches unless otherwise noted. BSC is an ANSI standard for Basic Space Centering.
Not to scale. For reference only.

PDR 144, Trimmed and Formed Plastic Quad Flat Pack



Top View



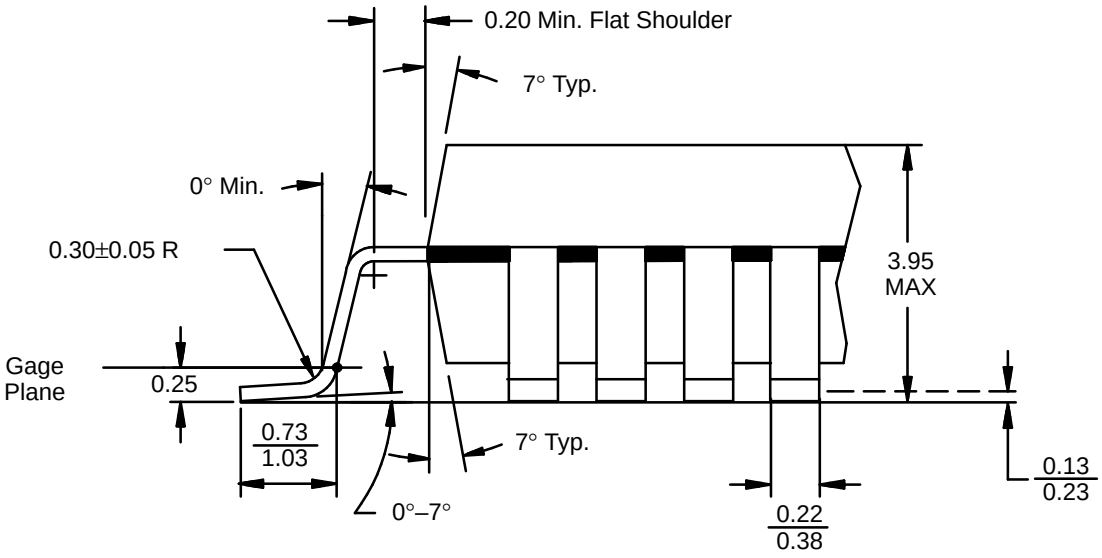
Side View

pqr144
4–15–94

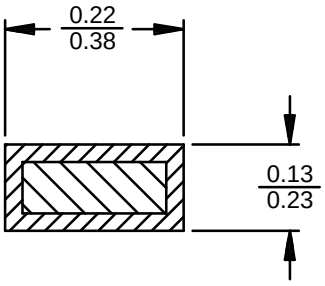
Notes:

All measurements are in millimeters unless otherwise noted. Not to scale. For reference only.

PDR 144 (continued)



Detail X



Section S–S

pqr144
4–15–94

Notes:

Not to scale. For reference only.