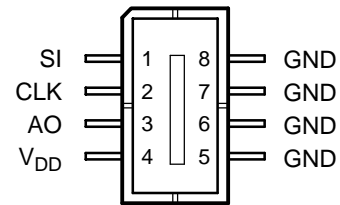**TEXAS ADVANCED OPTOELECTRONIC SOLUTIONS™**

- **Optical Glass Window**
- **128 × 1 Sensor-Element Organization**
- **400 Dots-Per-Inch (DPI) Sensor Pitch**
- **High Linearity and Uniformity for 256 Gray-Scale (8-Bit) Applications**
- **Output Referenced to Ground**
- **Low Image Lag . . . 0.5% Typ**
- **Operation to 2 MHz**
- **Single 5-V Supply**

(TOP VIEW)

SI	1	8	GND
CLK	2	7	GND
AO	3	6	GND
V_{DD}	4	5	GND

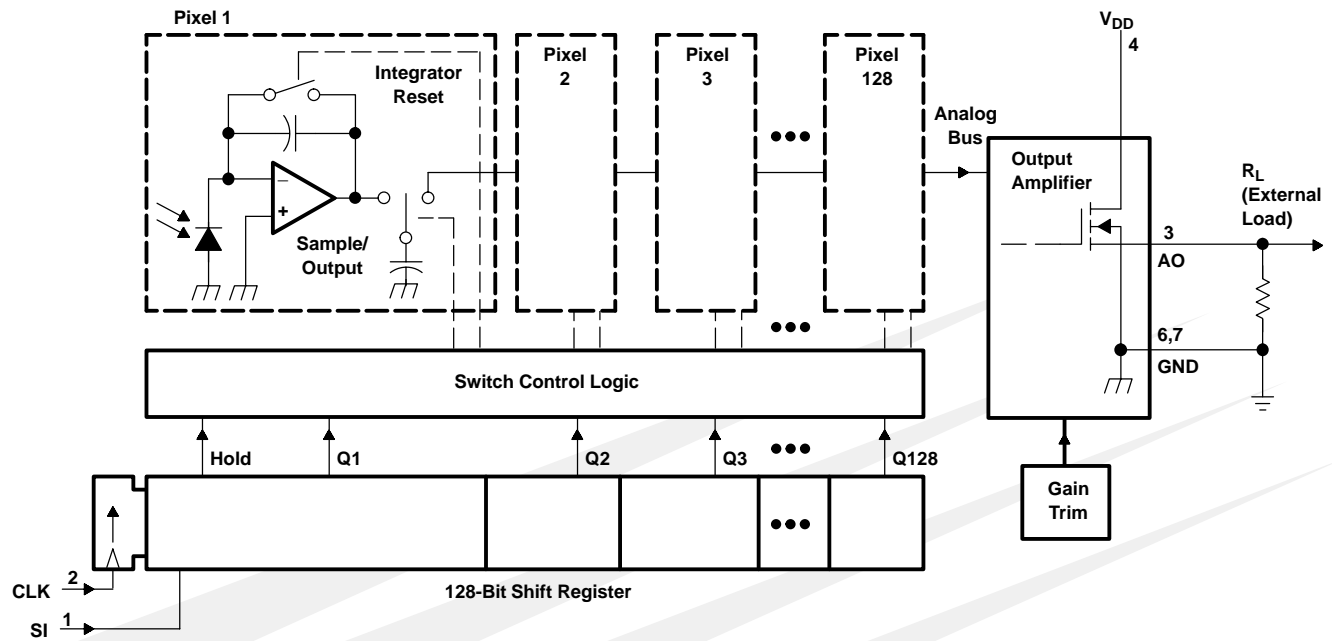## Description

The TSLW1401 linear sensor array consists of a 128 × 1 array of photodiodes, associated charge amplifier circuitry, and a pixel data-hold function that provides simultaneous-integration start and stop times for all pixels. The pixels measure 63.5 µm (H) by 55.5 µm (W) with 63.5-µm center-to-center spacing and 8-µm spacing between pixels. Operation is simplified by internal control logic that requires only a serial-input (SI) signal and a clock.

Functional Block Diagram

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800 Jupiter Road, Suite 205 • Plano, TX 75074 • (972) 673-0759

Terminal Functions

TERMINAL		DESCRIPTION
NAME	**NO.**	
AO	3	Analog output.
CLK	2	Clock. The clock controls charge transfer, pixel output, and reset.
GND	5,6,7,8	Ground (substrate). All voltages are referenced to the substrate.
SI	1	Serial input. SI defines the start of the data-out sequence.
V_{DD}	4	Supply voltage. Supply voltage for both analog and digital circuits.

Detailed Description

The sensor consists of 128 photodiodes arranged in a linear array. Light energy impinging on a photodiode generates photocurrent, which is integrated by the active integration circuitry associated with that pixel.

During the integration period, a sampling capacitor connects to the output of the integrator through an analog switch. The amount of charge accumulated at each pixel is directly proportional to the light intensity and the integration time.

The output and reset of the integrators is controlled by a 128-bit shift register and reset logic. An output cycle is initiated by clocking in a logic 1 on SI. For proper operation, after meeting the minimum hold time condition, SI must go low before the next rising edge of the clock. An internal signal, called Hold, is generated from the rising edge of SI and transmitted to analog switches in the pixel circuit. This causes all 128 sampling capacitors to be disconnected from their respective integrators and starts an integrator reset period. As the SI pulse is clocked through the shift register, the charge stored on the sampling capacitors is sequentially connected to a charge-coupled output amplifier that generates a voltage on analog output AO. Simultaneously, during the first 18 clock cycles, all pixel integrators are reset, and the next integration cycle begins on the 19th clock. On the 129th clock rising edge, the SI pulse is clocked out of the shift register and the analog output AO assumes a high impedance state. Note that this 129th clock pulse is required to terminate the output of the 128th pixel, and return the internal logic to a known state. A subsequent SI pulse may be presented as early as the 130th clock pulse, thereby initiating another pixel output cycle.

AO is driven by a source follower that requires an external pulldown resistor. When the output is not in the output phase, it is in a high-impedance state. The output is nominally 0 V for no light input and 2 V for a nominal white-level output.

The voltage developed at analog output (AO) is given by:

$$V_{out} = V_{drk} + (R_e)(E_e)(t_{int})$$

where:

V_{out} is the analog output voltage for white condition
V_{drk} is the analog output voltage for dark condition
R_e is the device responsivity for a given wavelength of light given in V/(μJ/cm^2)
E_e is the incident irradiance in μW/cm^2
t_{int} is integration time in seconds

The TSL1401 is intended for use in a wide variety of applications, including: image scanning, mark and code reading, optical character recognition (OCR) and contact imaging, edge detection and positioning, and optical linear and rotary encoding.

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Absolute Maximum Ratings†

Supply voltage range, V_{DD} . . . . −0.3 V to 6 V
Input voltage range, V_I . . . . −0.3 V to V_{DD} + 0.3V
Input clamp current, I_{IK} ($V_I < 0$) or ($V_I > V_{DD}$) . . . . −20 mA to 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) . . . . −25 mA to 25 mA
Voltage range applied to any output in the high impedance or power-off state, V_O . . . −0.3 V to V_{DD} + 0.3 V
Continuous output current, I_O (V_O = 0 to V_{DD}) . . . . −25 mA to 25 mA
Continuous current through V_{DD} or GND . . . . −40 mA to 40 mA
Analog output current range, I_O . . . . −25 mA to 25 mA
Operating free-air temperature range, T_A . . . . −25°C to 115°C
Storage temperature range, T_{stg} . . . . −40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions (see Figure 1 and Figure 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	5	5.5	V
Input voltage, V_I	0		V_{DD}	V
High-level input voltage, V_{IH}	2		V_{DD}	V
Low-level input voltage, V_{IL}	0		0.8	V
Wavelength of light source, λ	400		1000	nm
Clock frequency, f_{clock}	5		2000	kHz
Sensor integration time, t_{int}	0.0645		100	ms
Setup time, serial input, $t_{su(SI)}$	20			ns
Hold time, serial input, $t_{h(SI)}$ (see Note 1)	0			ns
Operating free-air temperature, T_A	−25		115	°C

NOTE 1: SI must go low before the rising edge of the next clock pulse.

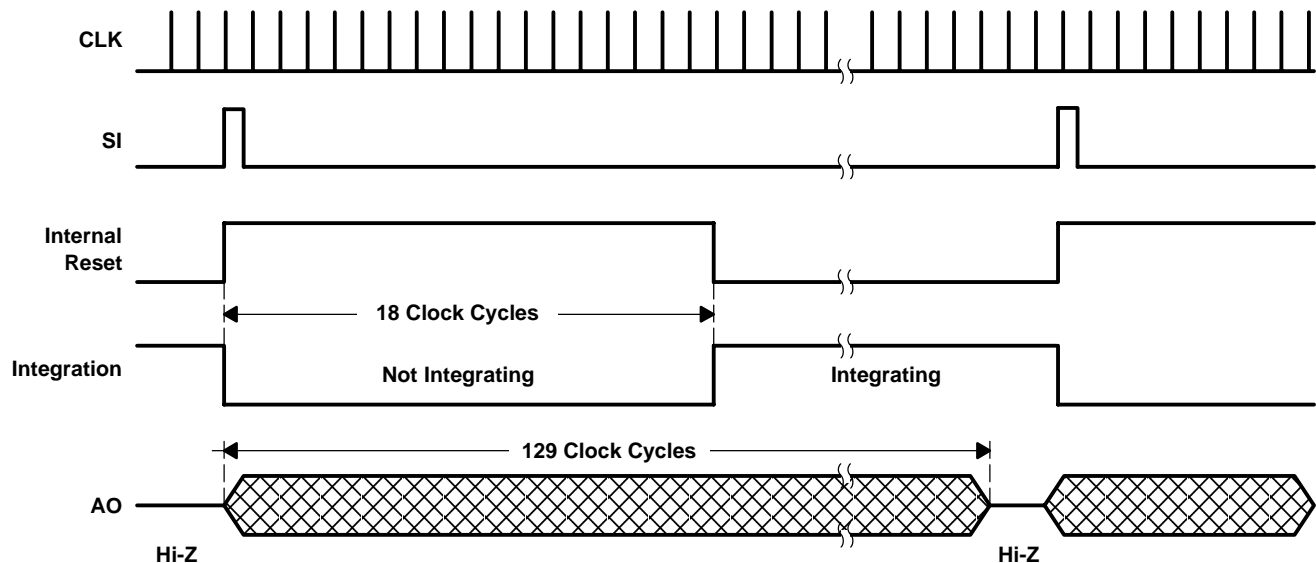
Figure 1. Timing Waveforms

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TSLW1401
EXTENDED TEMPERATURE
128 × 1 LINEAR SENSOR ARRAY WITH HOLD

TAOS024A – JUNE 2001

Electrical Characteristics at f_{clock} = 1 MHz, V_{DD} = 5 V, T_A = 25°C, λ_p = 565 nm, t_{int} = 5 ms, R_L = 330 Ω, E_e = 15 μW/cm² (unless otherwise noted) (see Note 2)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{out}	Analog output voltage (white, average over 128 pixels)	E_e = 15 μW/cm², t_{int} = 5 ms,	λ_p = 565 nm see Note 2	1.6	2	2.4	V
V_{drk}	Analog output voltage (dark, average over 128 pixels)			0	0.1	0.2	V
PRNU	Pixel response nonuniformity	See Notes 3 & 4	λ_p = 565 nm		±4%	±7.5%	
	Nonlinearity of analog output voltage	See Note 4			±0.4%		FS
	Output noise voltage	See Note 5			1		mVrms
R_e	Responsivity			19	25	32	V/ (μJ/cm²)
V_{sat}	Analog output saturation voltage			3	3.5		V
SE	Saturation exposure	See Note 6	λ_p = 565 nm	88	136		nJ/cm²
DSNU	Dark signal nonuniformity	All pixels	See Note 7		0.08	0.120	V
		All except pixel 1	See Note 7		0.017	0.035	
IL	Image lag	See Note 8			0.5%		
I_{DD}	Supply current				2.5	4	mA
I_{IH}	High-level input current	$V_I = V_{DD}$				1	μA
I_{IL}	Low-level input current	$V_I = 0$				1	μA
C_i	Input capacitance					5	pF

NOTES: 2. The array is uniformly illuminated with a diffused LED source having a peak wavelength of 565 nm.
3. PRNU is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test when the array is uniformly illuminated at the white irradiance level. PRNU includes DSNU.
4. Nonlinearity is defined as the maximum deviation from a best-fit straight line over the dark-to-white irradiance levels, as a percent of analog output voltage (white).
5. RMS noise is the standard deviation of a single-pixel output under constant illumination as observed over a 5-second period.
6. Minimum saturation exposure is calculated using the minimum V_{sat}, the maximum V_{drk}, and the maximum R_e.
7. DSNU is the difference between the maximum and minimum output voltage in the absence of illumination.
8. Image lag is a residual signal left in a pixel from a previous exposure. It is defined as a percent of white-level signal remaining after a pixel is exposed to a white condition followed by a dark condition:

$$IL = \frac{V_{out\,(IL)} - V_{drk}}{V_{out\,(white)} - V_{drk}} \times 100$$

Timing Requirements (see Figure 1 and Figure 2)

		MIN	NOM	MAX	UNIT
$t_{su(SI)}$	Setup time, serial input (see Note 9)	20			ns
$t_{h(SI)}$	Hold time, serial input (see Note 9 and Note 10)	0			ns
t_w	Pulse duration, clock high or low	50			ns
t_r, t_f	Input transition (rise and fall) time	0		500	ns

NOTES: 9. Input pulses have the following characteristics: t_r = 6 ns, t_f = 6 ns.
10. SI must go low before the rising edge of the next clock pulse.

Dynamic Characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_s	Analog output settling time to ±1%	R_L = 330 Ω, C_L = 50 pF		350		ns

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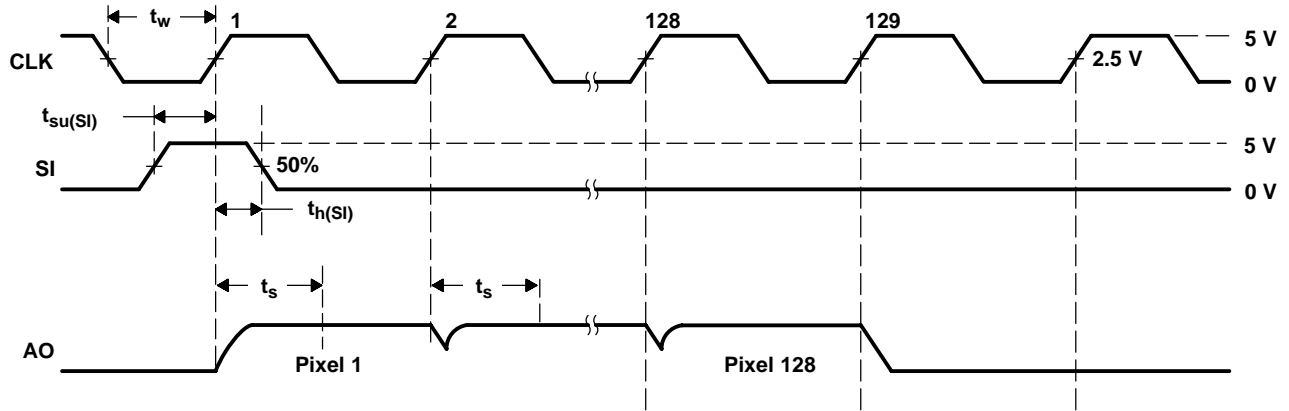
Figure 2. Operational Waveforms

TYPICAL CHARACTERISTICS
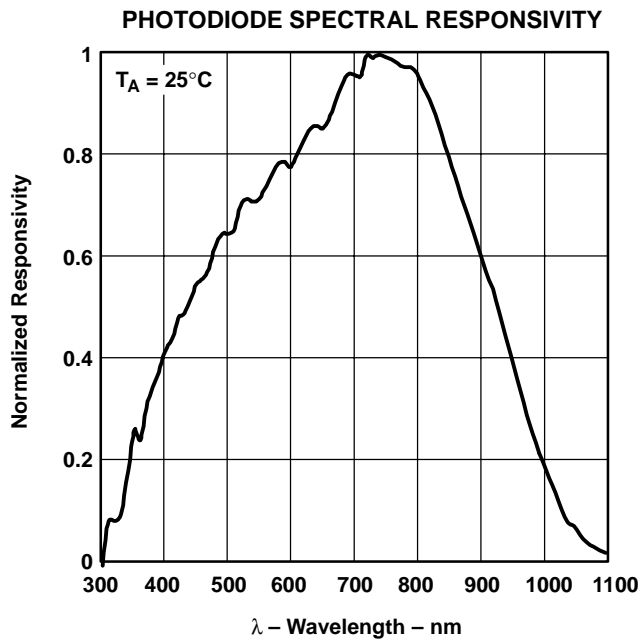
PHOTODIODE SPECTRAL RESPONSIVITY

Figure 3

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TYPICAL CHARACTERISTICS

DARK SIGNAL NONUNIFORMITY
vs
FREE-AIR TEMPERATURE

Figure 4

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

Figure 5

ANALOG OUTPUT SATURATION VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 6

AVERAGE ANALOG OUTPUT VOLTAGE, WHITE
vs
FREE-AIR TEMPERATURE

V_{DD} = 5 V
λ = 400 nm to 660 nm

Figure 7

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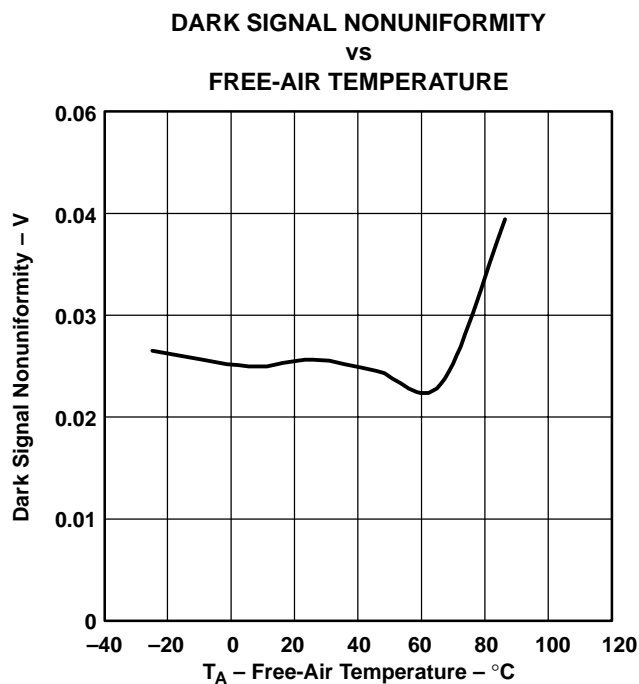
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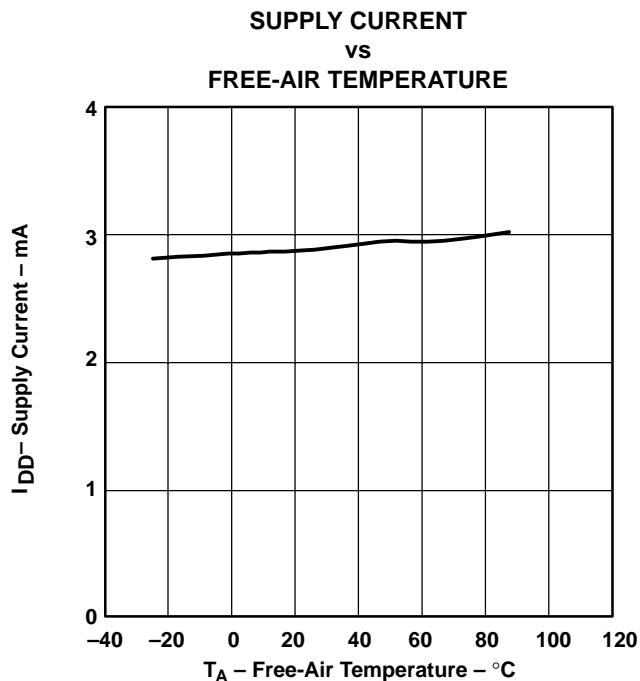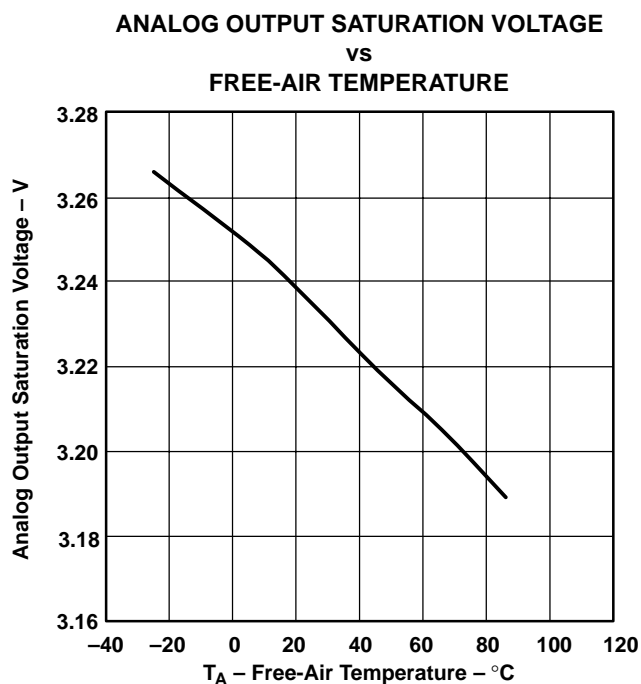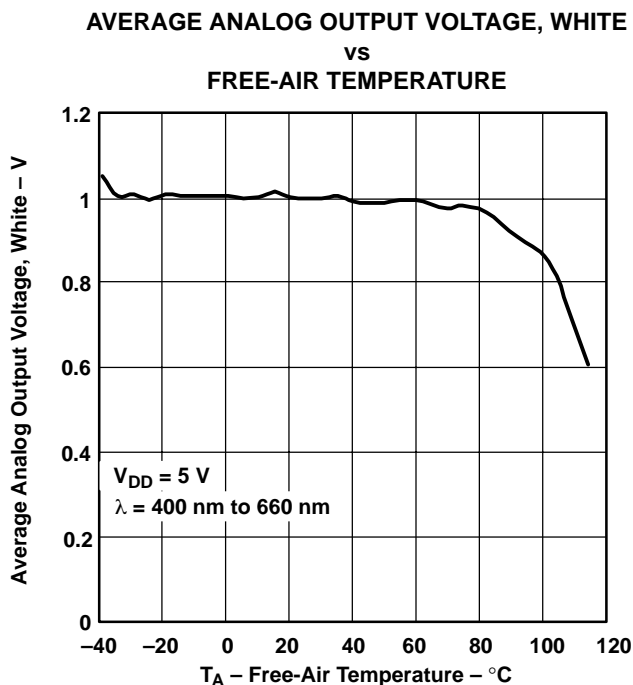
TYPICAL CHARACTERISTICS

AVERAGE ANALOG OUTPUT VOLTAGE, DARK
vs
FREE-AIR TEMPERATURE
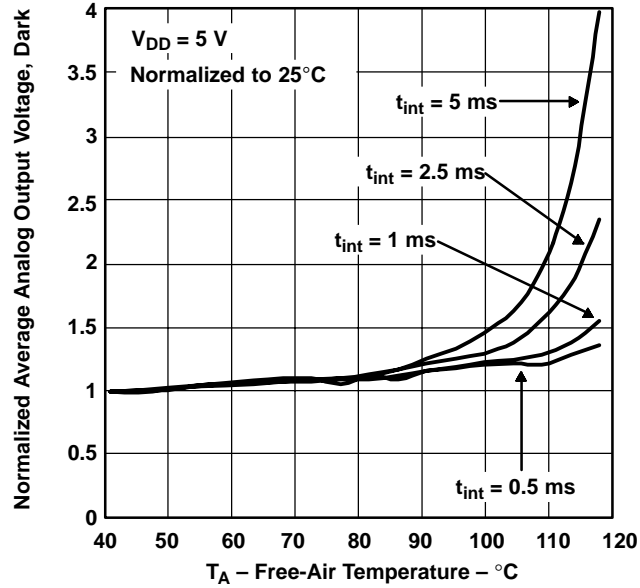
Figure 8

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MECHANICAL INFORMATION

The integrated circuit is mounted in a window frame package with a clear, flat glass cover.

Pin 1 SI
Pin 2 CLK
Pin 3 AO
Pin 4 V_{DD}
Pin 5 GND
Pin 6 GND
Pin 7 GND
Pin 8 GND

NOTES: A. All linear dimensions are in inches and parenthetically in [millimeters] (± 0.1 mm).
        B. Pixel 1 typical location aligns on leading edge of pin 1 and 0.71 mm above package centerline.
        C. Glass thickness nominally 1 mm with refraction index of 1.5186.

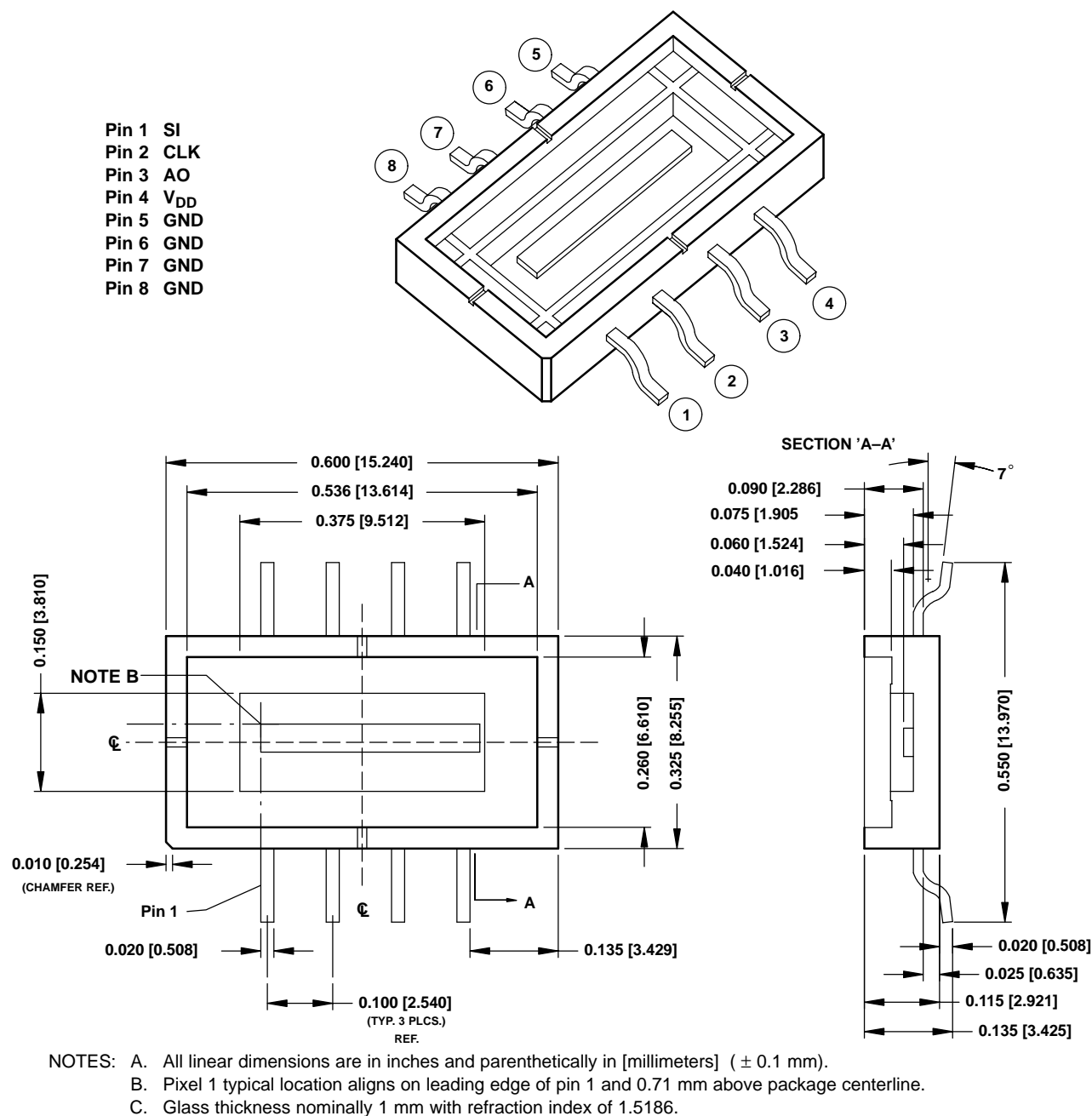**Figure 9. Packaging Configuration**

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