Description

The SK10/100EL33W is a ÷4 Divider. This device is fully compatible with MC10/100EL33 and MC10/100LVEL33.

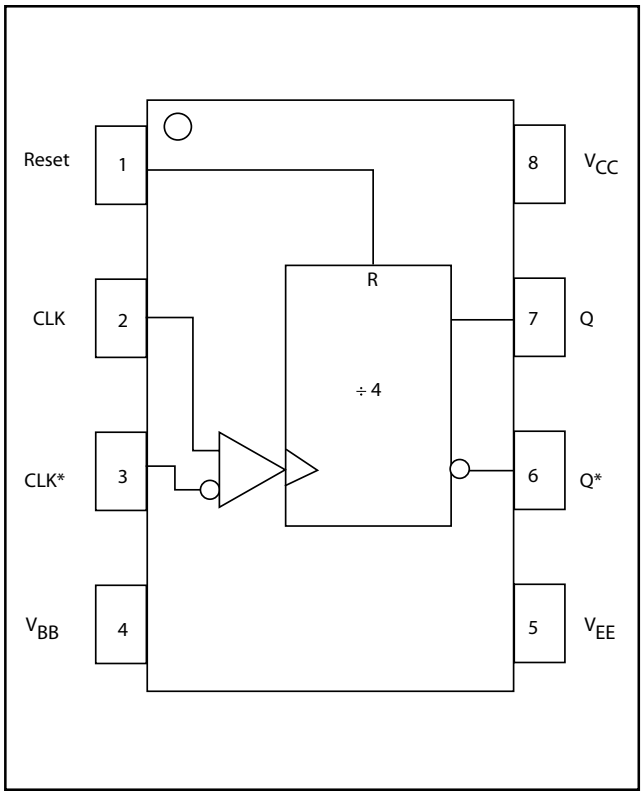
The SK10/100EL33W provides a V_{BB} output for either single-ended use or as a DC bias for AC coupling to the device. The V_{BB} pin should be used only as a bias for the SK10/100EL33W as its current sink/source capability is limited. Whenever used, the V_{BB} pin should be bypassed to V_{CC} via a 0.01 µF capacitor.

The Reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state. The Reset pin allows for the synchronization of multiple EL33W's in a system.

Features

- Extended Supply Voltage Range: (VEE = –5.5V to –3.0V, VCC = 0V) or (VCC = +3.0V to +5.5V, VEE = 0V)
- High Bandwidth Output Transition
- 650ps Propagation Delay
- V_{BB} Output
- 75KΩ Internal Input Pulldown Resistor
- 4.0 GHz Toggle Frequency
- New Differential Input Common Mode Range
- Fully Compatible with MC10/100EL33 and MC10/100LVEL33
- ESD Protection of >4000V
- Industrial Temperature Range: –40°C to 85°C
- Available in 8-Pin SOIC (150 mils) Package

Functional Block Diagram

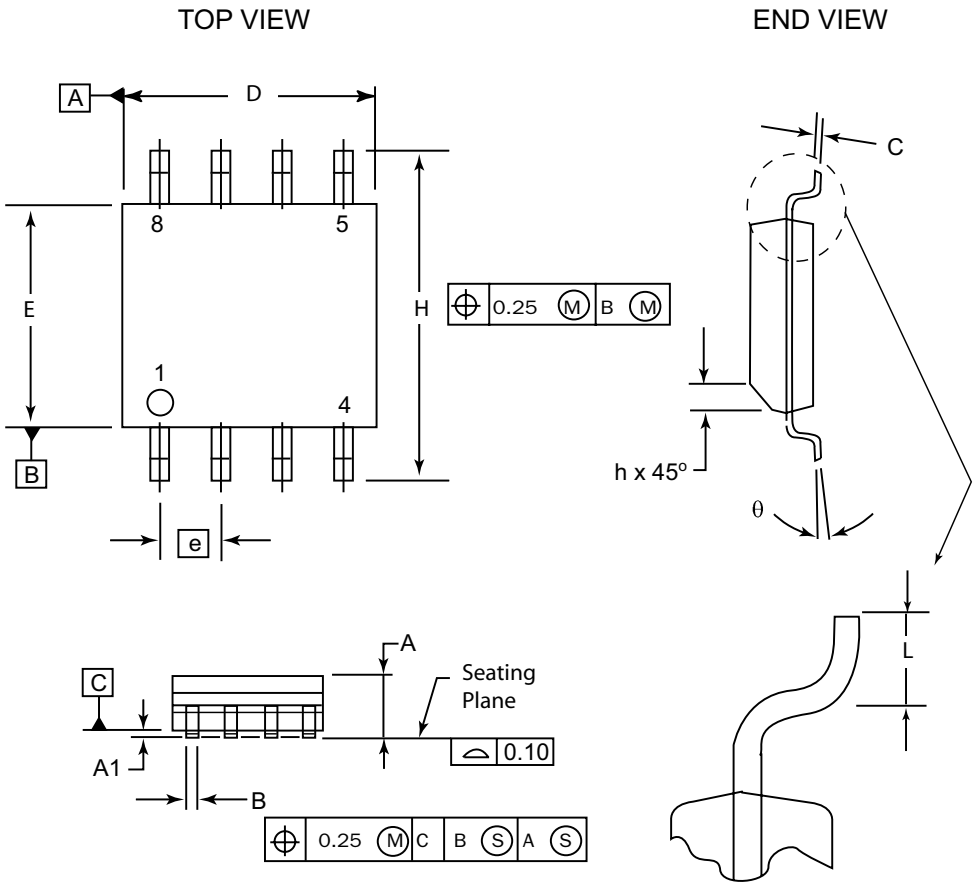


PIN Description

Pin	Function
CLK, CLK*	Clock Inputs
Reset	Asynch Reset
V_{BB}	Ref Voltage Output
Q, Q*	Data Outputs

Package Information

8 Pin SOIC Package



DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

NOTES:
1. Dimensions are in millimeters.
2. Dimensions D and E do not include mold protrusion.
3. Maximum mold protrusion 0.15 per side.
4. Dimension B does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.127 total in excess of the B dimension at maximum material condition.

DC Characteristics

SK10/100EL33W DC Electrical Characteristics (Notes 1, 2)

(V_{CC} – V_{EE} = 3.0V to 5.5V; VOUT Loaded 50Ω to VCC – 2.0V)

Symbol	Characteristic	TA = –40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{IN}	Input Current (Diff) (SE)	-150		150 150	-150		150 150	-150		150 150	-150		150 150	µA µA
I_{EE}	Power Supply Current 10EL 100EL	 16 20	 23 27	 30 38	 16 20	 23 27	 30 38	 16 20	 23 27	 30 38	 16 20	 23 27	 30 38	 mA mA
V_{BB}	Output Reference Voltage[5] 10EL 100EL	 -1.43 -1.38		 -1.30 -1.26	 -1.38 -1.38		 -1.27 -1.26	 -1.35 -1.38		 -1.25 -1.26	 -1.31 -1.38		 -1.19 -1.26	 V V
V_{CC} - V_{EE}	Power Supply Voltage	3.0		5.5	3.0		5.5	3.0		5.5	3.0		5.5	V

AC Characteristics

SK10/100EL33W AC Characteristics *(Notes 1, 2)*

(V_{CC} – V_{EE} = 3.0V to 5.5V; VOUT Loaded 50Ω to VCC – 2.0V)

Symbol	Characteristic	TA = –40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	3.4	4.2		3.8	4.2		3.8	4.2		3.8	4.2		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Q Reset to Q	 550 430	 590 490	 660 555	 555 410	 600 475	 670 555	 565 400	 610 460	 680 555	 590 355	 625 440	 730 560	 ps ps
t_{skew}	Duty Cycle Skew			20			20			20			20	ps
V_{PP}[3]	Minimum Input Swing	150		1000	150		1000	150		1000	150		1000	mV
V_{CMR}[4]	Common Mode Range	VEE + 1.7		VCC - 0.4	VEE + 1.7		VCC - 0.4	VEE + 1.7		VCC - 0.4	VEE + 1.7		VCC - 0.4	V
t_r t_f	Output Rise/Fall Times (20% – 80%) Q, Q*	125	150	210	130	160	215	135	165	220	145	170	225	ps

AC Characteristics *(continued)*

Notes:

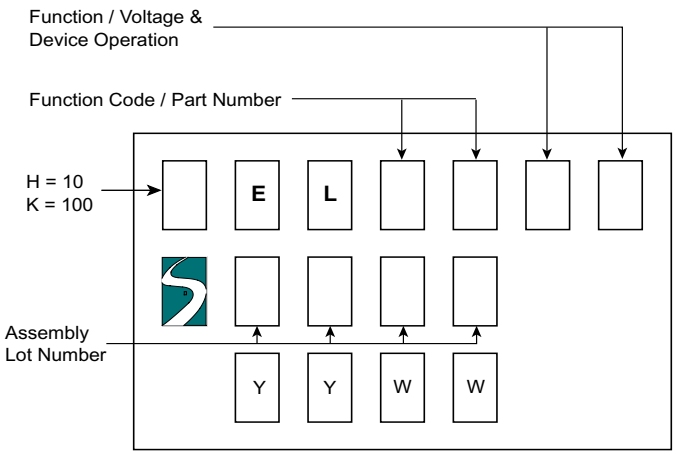
1. 10EL circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained. Outputs are terminated through a 50W resistor to VCC - 2.0V except where otherwise specified on the individual data sheets.
2. 100K circuits are designed to meet the DC specifications shown in the table where transverse airflow greater than 500 lfpm is maintained.
3. Minimum input swing for which AC parameters are guaranteed.
4. CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between $VPP_{(min)}$ and 1V. The lower end of the CMR range varies 1:1 with VEE and is equal to VEE + 1.7V.
5. Voltages referenced to VCC = 0V.
6. For standard ECL DC specifications, refer to the ECL Logic Family Standard DC Specifications Data Sheet.
7. For part ordering description, see HPP Part Ordering Information Data Sheet.

Ordering Information

Ordering Code	Package ID	Temperature Range
SK10EL33WD	8-SOIC	Industrial
SK10EL33WDT	8-SOIC	Industrial
SK100EL33WD	8-SOIC	Industrial
SK100EL33WDT	8-SOIC	Industrial
SK10EL33WU	Die	
SK100EL33WU	Die	

Marking Information

8 PIN SOIC PACKAGE



YY: Last two digits of the Year
WW: Working Week

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