

GC5322 Wideband Digital Predistortion Transmit Processor

FEATURES

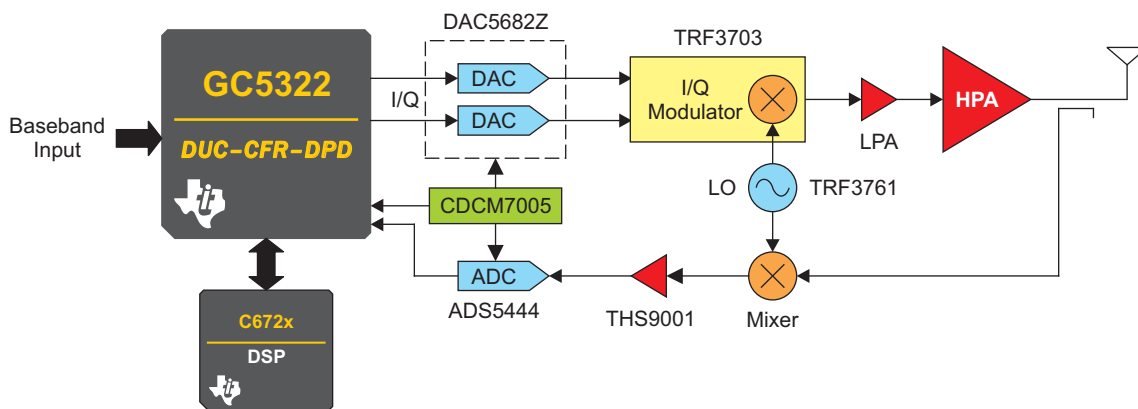
- Integrated DUC, CFR, and DPD Functions
- Up to 40-MHz Combined Signal Bandwidth
- DUC: up to 12 CDMA2000 or TD-SCDMA, 4 W-CDMA, 4–10 MHz or 2–20 MHz OFDMA Carriers
- CFR: Typically Meets 3GPP TS 25.141 <6.5 dB PAR, <8 dB PAR for 802.16e Signals
- DPD: Memory Compensation, Typical ACLR Improvement of 20 dB to 30 dB or More
- Transmit- and Feedback-Channel Equalizers
- 352-Ball S-PBGA Package, 27 mm × 27 mm

- 1.2-V Core, 3.3-V I/O
- Typical Power Consumption = 2.5 W
- Flexible DSP Algorithm Supports Existing and Emerging Wireless Standards
- Supports Direct Interface to TI High-Speed Data Converters

APPLICATIONS

- 3GPP (W-CDMA, TD-SCDMA) Base Stations
- 3GPP2 (CDMA2000) Base Stations
- WiMAX and WiBro (OFDMA) Base Stations
- Multicarrier Power Amplifiers (MCPAs)

SYSTEM BLOCK DIAGRAM



B0278-01

DESCRIPTION

The GC5322 is a wideband digital predistortion transmit processor that includes a digital upconverter (DUC) block, a crest factor reduction (CFR) block, and a digital predistortion (DPD) block with its associated feedback chain and capture buffers. The GC5322 processes composite input bandwidths of up to 40 MHz and processes DPD sample rates of up to 140 MHz. The GC5322 DUC block accepts baseband signals over an interleaved parallel interface at a data rate of up to 93.3 MSPS. The GC5322 CFR block reduces the peak-to-average ratio (PAR) of wideband digital signals provided in quadrature (I/Q) format, such as those used in third-generation (3G) code division multiple access (CDMA) wireless and orthogonal frequency division multiple access (OFDMA) applications. The GC5322 DPD block reduces adjacent-channel leakage ratio (ACLR), or out-of-band energy, by 20 dB to 30 dB or more. The efficiency of follow-on power amplifiers (PAs) is substantially improved by reducing the PAR and ACLR of digital signals. The digital-to-RF conversion can be further simplified by the fractional interpolator between the CFR and the DPD blocks, and a bulk upconverter (BUC) in the final stage of the GC5322. This feature typically eliminates the need for superheterodyne (dual-stage) upconversion architectures. Transmit and feedback NCO/mixers provide additional flexibility in the system frequency planning.

To request more information on the GC5322 Wideband Digital Pre-Distortion Transmit Processor, go to <http://www.ti.com/gc5322-info>.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

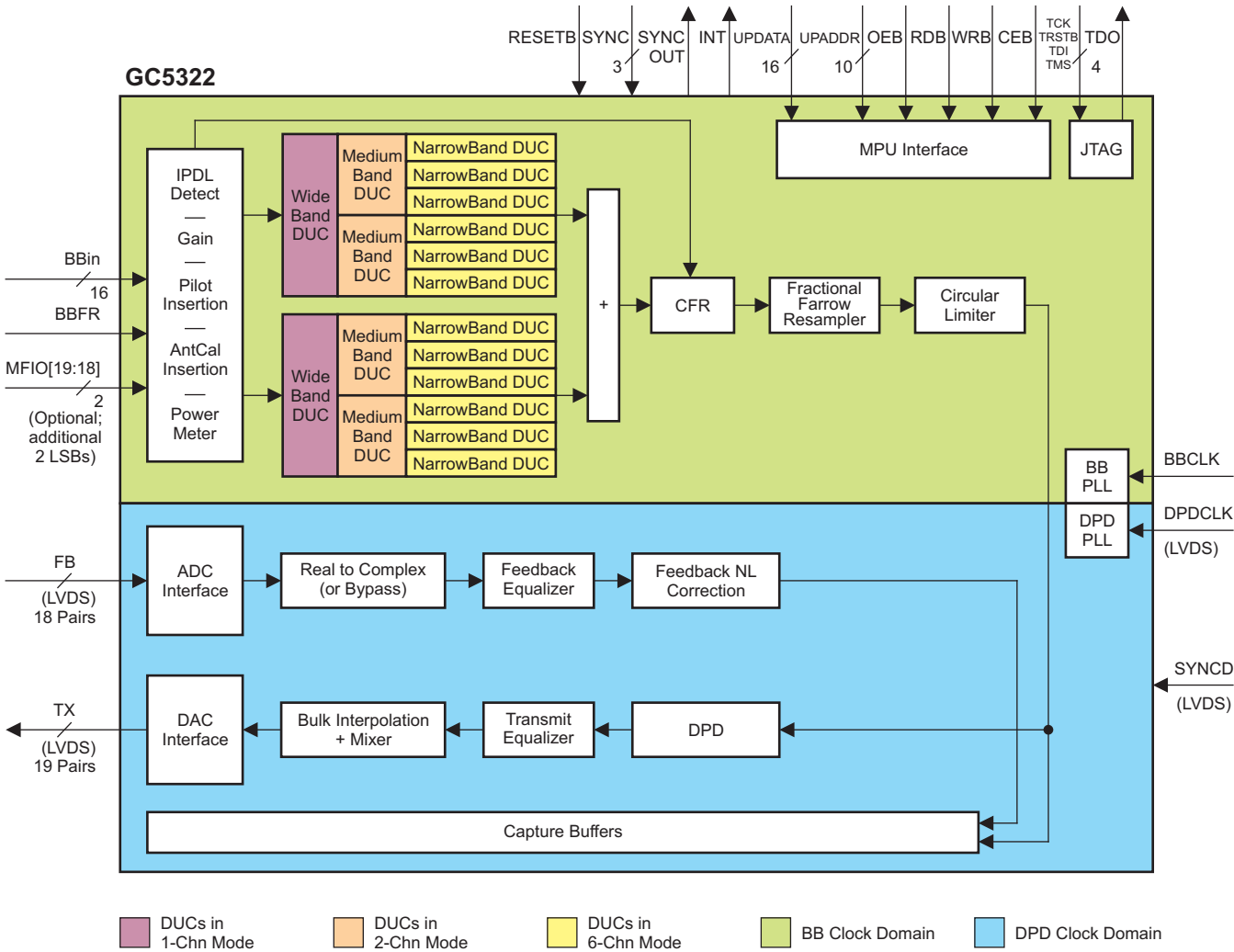
AVAILABLE OPTIONS

T _A	PACKAGED DEVICE ⁽¹⁾
	352-ball S-PBGA package, 27 mm × 27 mm

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

GC5322 FUNCTIONAL BLOCK DIAGRAM

ADVANCE INFORMATION



B0279-01

DETAILED DESCRIPTION

GC5322 Introduction

The GC5322 is a flexible transmit sector processor that includes a digital upconverter (DUC) block, a crest factor reduction (CFR) block, and a digital predistortion (DPD) block and its associated feedback chain. The GC5322 processes composite input bandwidths of up to 40 MHz and processes DPD expansion bandwidths of up to 140 MHz (actual performance may vary for signal bandwidths exceeding 23 MHz). By reducing both the peak-to-average ratio (PAR) of the input signals using the CFR block and linearizing the power amplifier (PA) using the DPD block, the GC5322 reduces the costs of multicarrier PAs (MCPA) for wireless infrastructure applications. The GC5322 applies CFR and DPD while a separate microprocessor (a Texas Instruments TMS320C6727 DSP) is used to optimize performance levels and maintain target PA performance levels.

By including the GC5322 in their system architecture, manufacturers of BTS equipment can realize significant savings on power amplifier bill of materials (BOM) and overall operational costs due to the PA efficiency improvement. The GC5322 meets multicarrier 3G performance standards (PCDE, composite EVM, and ACLR) at PAR levels down to 6.5 dB and improves the ACLR, at the PA output, by 20 dB to 30 dB or more. The GC5322 integrates easily into the transmit signal chain between baseband processors such as the Texas Instruments TMS320C64x™ DSP family and their high-performance data converters.

A typical GC5322 system application would include the following transmit-chain components:

- TMS320C6727 digital signal processor (DSP)
- DAC5682 16-bit, 1-GSPS DAC (transmit path)
- CDCM7005 clock generator
- TRF3761 integrated VCO/PLL synthesizer
- TRF3703 quadrature modulator
- ADS5517 11-bit 200-MSPS or ADS5444 13-bit, 250-MSPS ADC (feedback path)
- AMC7823 analog monitoring and control circuit with GPIO and SPI

Baseband Interface

The GC5322 BB interface block accepts baseband signals over an interleaved parallel interface at a data rate of up to 93.3 MHz. The input interface supports up to 12 separate baseband carriers. The GC5322 DUC block can be programmed in a wideband mode in which users are required to channelize the data using an external processor.

Gain/Pilot Insertion/AntCal Insertion/Power Meter

Baseband gain can be applied on a per-carrier basis to accurately control the individual channel power through the system. Also present is the functionality for adding pilot codes to the data stream for antenna calibration applications. Independent programmable RMS power meters for up to 12 channels are also included in this block of the device.

Digital Upconverters (DUCs)

The GC5322 DUC block digitally upconverts, spectrally shapes and combines multiple channels into one wideband, composite signal. It can support:

- Up to twelve cdma2000/TDSCDMA carriers
- Up to four 5-MHz W-CDMA (UMTS) carriers
- Up to two 10-MHz OFDMA (WiMAX/WiBRO) channels
- One 20-MHz OFDMA (WiMAX/WiBRO) channel

Or, with reduced DPD expansion bandwidth:

- Up to four 10-MHz OFDMA (WiMAX/WiBRO) channels
- Up to two 20-MHz OFDMA channels
- One 40-MHz OFDMA channel

Users can specify the filter characteristics of the DUC programmable finite impulse response (PFIR), compensating finite impulse response (CFIR), and cascade integrator comb (CIC) filters. Users can also specify the center frequencies of each carrier with a resolution of 0.25 μ Hz. Additional controls available in the DUCs include bulk and fractional time delay adjustments, phase adjustments, and equalization. The maximum DUC output bandwidth is 40 MHz. The maximum DUC complex output sampling rate is 70 MSPS.

Crest Factor Reduction (CFR)

The GC5322 CFR block selectively reduces the peak-to-average ratio (PAR) of wideband digital signals provided in quadrature (I and Q) format, such as those used in third-generation (3G) code division multiple access (CDMA) wireless applications. The CFR block can reduce the PAR of W-CDMA Test Model 1 and Test Model 3 signals down to 6.5 dB output PAR while still meeting all 3GPP requirements for ACLR, composite EVM, and peak code domain error (PCDE). The CFR block accepts input sampling rates up to 70 MSPS complex either from the DUC block or directly from the input interface.

Fractional Farrow Resampler (FR)

The CFR block output signal bandwidth is up to 40 MHz wide, sampled at up to 70 MSPS. However; the DPD block provides PA compensation over an expansion bandwidth of up to 140 MHz, using a complex sampling rate of up to 140 MSPS. To provide the requisite sampling rate of up to 140 MSPS at the input to DPD, the output of the CFR block must be resampled. The GC5322 performs this (nominally 2 $\times$) upsampling function using a Farrow filter resampler. The user-programmable Farrow resampler supports upsampling rates from 1 $\times$ to 64 $\times$, with 16-bit precision on the interpolation ratio. It marks the transition of the input clock domain (driven by the input interface clock) to the transmit domain (driven by the DAC sampling clock).

Digital Predistortion (DPD)

The DPD block provides predistortion for up to Nth-order nonlinearities, and can correct multiple orders and lengths of PA memory effects. The predistortion correction terms are computed by an external processor (for example, TI TMS320C6727 DSP) based on PA feedback data captured in the GC5322. The external processor reads the captured data buffers from the GC5322 and writes back the newly computed DPD correction terms on a continuous basis. TI provides a base delivery of 'C6727 software to GC5322 customers that achieves a typical ACLR improvement of 20 dB to 30 dB or more when compared to a PA without DPD. The standard EMIF bus allows the user to provide an alternate DPD adaptation algorithm and DSP embodiment, if desired.

Bulk Upconverter (BUC)

The bulk upconverter block can interpolate the DPD block output by 1.5 $\times$, 2 $\times$, 3 $\times$, or 6 $\times$. The complex-to-real converter block optionally modifies the DPD complex output stream into a real output stream. The bulk upconverter has flexible mixing options between its various interpolation stages. When used in combination, the bulk upconverter and the complex-to-real functions allow the GC5322 to output a 16-bit real signal at up to 840 MSPS, or a complex signal at up to 420 MSPS. Next-generation data converters can accept sampling rates as high as 1 GSPS and sample widths of 16 bits. In a typical application, the bulk upconverter outputs a 737.28-MSPS real sampling rate (16 bits/sample) directly to the DAC on a modified center frequency of 184.32 MHz (1/4 of the 737.28-MSPS sampling rate). The bulk upconverter has multiple high-speed, low-voltage, single-ended/differential output interfaces to existing and future TI DACs.

Feedback Path (FB)

The feedback block accepts an external A/D converter input that represents the PA output signal. This feedback signal is processed by a feedback path that adjusts for gain, frequency, and phase anomalies in the RF-to-IF downconversion chain. The feedback path includes an 8-tap complex receive equalizer and lookup tables that can compensate for the nonlinearities in the RF-to-IF part of the feedback chain. The block also includes a real-to-complex conversion to facilitate signal processing. The GC5322 connects directly to the ADS5444, ADS5545, ADS5546, and ADS5517 among others, without requiring external components. The GC5322 simplifies timing by providing a FIFO for each ADC port, sampling the input data using the ADC data-ready signal.

Microprocessor Interface (MPU)

The MPU interface is designed to interface with external memory interface (EMIF) ports on TI DSPs operating in asynchronous mode. It consists of a 16-bit bidirectional data bus, a 10-bit address bus, and RDB, WRB, OEB, and CEB control signals. The interface fully supports TI 'C55x™, 'C64x™ DSPs and, with minimal effort, supports the low-cost 'C6727 floating-point DSP.

Smart Capture Buffers (SCB)

The GC5322 has two capture buffers, each 4096 complex words deep, which are periodically read by the external coefficient update controller (DSP) in order to optimize the DPD coefficients. The first capture buffer can be used to capture:

- The output of the Farrow resampler; this is also called the reference signal.
- The feedback output; this represents the waveform as seen by the PA.
- The error output
- Testbus(31:16)

The second capture buffer can be used to provide:

- The output of the Farrow resampler; this is also called the reference signal.
- The feedback output; this represents the waveform as seen by the PA.
- The error output
- Testbus(15:0)

The reference and feedback buffers are time-aligned by the GC5322, because there may be a delay of tens or even hundreds of samples between the transmitted signal and the feedback signal from the PA output. The capture controller can trigger a capture on several different metrics, including an above-threshold peak count or an average signal power value.

Input and Output Syncs

The GC5322 features multiple-user programmable input syncs. These are typically used as trigger mechanisms to activate features within the device. These triggers can be provided internally or through externally provided inputs. The input syncs can be used to trigger:

- Power measurements
- DUC channel delay, dither, and tuner alignment
- Initializing/loading the DUC, feedback, equalizer, LUTs, etc.
- Flush out data within the processing blocks of the device
- Feedback path tuner alignment
- Capturing and sourcing of data through SCBs

Programmable Power Meters

There are three power meter locations/functions within the GC5322. The first is a channel RMS power meter. The second power meter is located at the output of the CFR block, and the final power detector is similar to the CFR output power detector and is located at the Farrow resampler output. This power meter can measure RMS power integrated up to a million samples at the DPD sample rate.

Related Material and Documents

- GC5322 Quick Start Guide
- Application Note: GC5322 Configuration and Performance for a UMTS (W-CDMA) BTS
- Application Note: GC5322 Configuration and Performance for an OFDMA (802.16e) BTS
- Application Note: GC5322 Configuration and Performance for a TD-SCDMA BTS
- GC5322 Architecture Data Sheet (DUC, CFR, FR, DPD, and BUC)

Contact Texas Instruments for projected availability of listed documents.

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