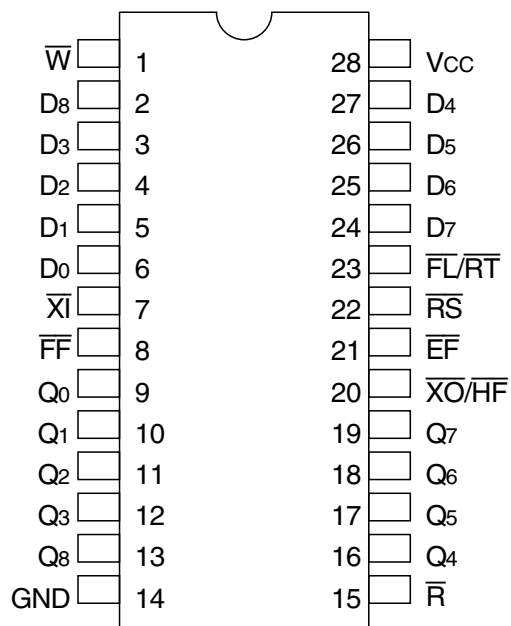
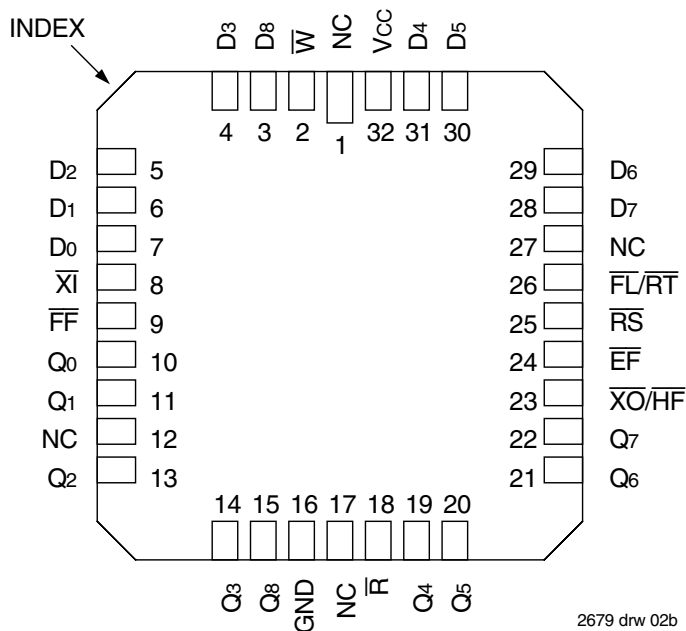




PIN CONFIGURATIONS



2679 drw 02a



2679 drw 02b

Package Type	Reference Identifier	Order Code
PLASTIC DIP ⁽¹⁾	P28-1	P
PLASTIC THIN DIP	P28-2	TP
CERDIP ⁽¹⁾	D28-1	D
THIN CERDIP	D28-3	TD
SOIC	SO28-3	SO

TOP VIEW

Package Type	Reference Identifier	Order Code
LCC ⁽¹⁾	L32-1	L
PLCC	J32-1	J

TOP VIEW

NOTE:

1. The 600-mil-wide DIP (P28-1 and D28-1) and LCC are not available for the IDT7200.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Com'l & Ind'l	Mil.	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T _{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I _{OUT}	DC Output Current	-50 to +50	-50 to +50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage Commercial/Industrial/Military	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH} ⁽¹⁾	Input High Voltage Com'l/Ind'l	2.0	—	—	V
V _{IH} ⁽¹⁾	Input High Voltage Military	2.2	—	—	V
V _{IL} ⁽²⁾	Input Low Voltage Commercial/Industrial/Military	—	—	0.8	V
T _A	Operating Temperature Commercial	0	—	70	°C
T _A	Operating Temperature Industrial	-40	—	85	°C
T _A	Operating Temperature Military	-55	—	125	°C

NOTES:

1. For $\overline{RT}/\overline{RS}/\overline{XI}$ input, V_{IH} = 2.6V (commercial).
For $\overline{RT}/\overline{RS}/\overline{XI}$ input, V_{IH} = 2.8V (military).
2. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: $V_{CC} = 5V \pm 10\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; Industrial: $V_{CC} = 5V \pm 10\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; Military: $V_{CC} = 5V \pm 10\%$, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$)

Symbol	Parameter	IDT7200L IDT7201LA IDT7202LA Com'l & Ind'l ⁽¹⁾ $t_A = 12, 15, 20, 25, 35, 50 \text{ ns}$		IDT7200L IDT7201LA IDT7202LA Military ⁽²⁾ $t_A = 20, 30, 50, 80 \text{ ns}$		Unit
		Min.	Max.	Min.	Max.	
$I_{LI}^{(3)}$	Input Leakage Current (Any Input)	-1	1	-10	10	μA
$I_{LO}^{(4)}$	Output Leakage Current	-10	10	-10	10	μA
V_{OH}	Output Logic "1" Voltage $I_{OH} = -2\text{mA}$	2.4	—	2.4	—	V
V_{OL}	Output Logic "0" Voltage $I_{OL} = 8\text{mA}$	—	0.4	—	0.4	V
$I_{CC1}^{(5,6,7)}$	Active Power Supply Current	—	80	—	100	mA
$I_{CC2}^{(5,8)}$	Standby Current ($\overline{R}=\overline{W}=\overline{RS}=\overline{FL}/\overline{RT}=V_{IH}$)	—	5	—	15	mA

NOTES:

- Industrial temperature range product for the 15ns and 25 ns speed grades are available as a standard device.
- Military speed grades of 50ns and 80ns are only available for the IDT7201LA.
- Measurements with $0.4 \leq V_{IN} \leq V_{CC}$.
- $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$.
- Tested with outputs open ($I_{OUT} = 0$).
- Tested at $f = 20 \text{ MHz}$.
- Typical $I_{CC1} = 15 + 2 \cdot f_s + 0.02 \cdot C_L \cdot f_s$ (in mA) with $V_{CC} = 5V$, $T_A = 25^\circ\text{C}$, $f_s = \text{WCLK frequency} = \text{RCLK frequency}$ (in MHz, using TTL levels), data switching at $f_s/2$, C_L = capacitive load (in pF).
- All Inputs = $V_{CC} - 0.2V$ or $\text{GND} + 0.2V$.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0 \text{ MHz}$)

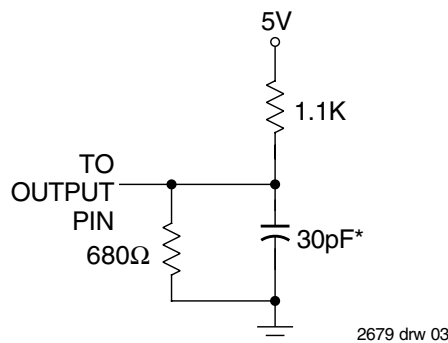
Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	8	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	pF

NOTE:

- Characterized values, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1



or equivalent circuit

Figure 1. Output Load

* Includes scope and jig capacitances.

AC ELECTRICAL CHARACTERISTICS⁽¹⁾

(Commercial: $V_{CC} = 5V \pm 10\%$, $T_A = 0^\circ C$ to $+70^\circ C$; Industrial: $V_{CC} = 5V \pm 10\%$, $T_A = -40^\circ C$ to $+85^\circ C$; Military: $V_{CC} = 5V \pm 10\%$, $T_A = -55^\circ C$ to $+125^\circ C$)

Symbol	Parameter	Commercial		Com'l & Ind'l ⁽²⁾		Com'l & Mil.		Com'l & Ind'l ⁽²⁾		Unit
		IDT7200L12 IDT7201LA12 IDT7202LA12		IDT7200L15 IDT7201LA15 IDT7202LA15		IDT7200L20 IDT7201LA20 IDT7202LA20		IDT7200L25 IDT7201LA25 IDT7202LA25		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _S	Shift Frequency	—	50	—	40	—	33.3	—	28.5	MHz
t _{RC}	Read Cycle Time	20	—	25	—	30	—	35	—	ns
t _A	Access Time	—	12	—	15	—	20	—	25	ns
t _{RR}	Read Recovery Time	8	—	10	—	10	—	10	—	ns
t _{RPW}	Read Pulse Width ⁽³⁾	12	—	15	—	20	—	25	—	ns
t _{RLZ}	Read Pulse Low to Data Bus at Low Z ⁽⁴⁾	3	—	3	—	3	—	3	—	ns
t _{WLZ}	Write Pulse High to Data Bus at Low Z ^(4,5)	5	—	5	—	5	—	5	—	ns
t _{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns
t _{RHZ}	Read Pulse High to Data Bus at High Z ⁽⁴⁾	—	12	—	15	—	15	—	18	ns
t _{WC}	Write Cycle Time	20	—	25	—	30	—	35	—	ns
t _{WPW}	Write Pulse Width ⁽³⁾	12	—	15	—	20	—	25	—	ns
t _{WR}	Write Recovery Time	8	—	10	—	10	—	10	—	ns
t _{DS}	Data Set-up Time	9	—	11	—	12	—	15	—	ns
t _{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t _{RSC}	Reset Cycle Time	20	—	25	—	30	—	35	—	ns
t _{RS}	Reset Pulse Width ⁽³⁾	12	—	15	—	20	—	25	—	ns
t _{RSS}	Reset Set-up Time ⁽⁴⁾	12	—	15	—	20	—	25	—	ns
t _{RSR}	Reset Recovery Time	8	—	10	—	10	—	10	—	ns
t _{RTC}	Retransmit Cycle Time	20	—	25	—	30	—	35	—	ns
t _{RT}	Retransmit Pulse Width ⁽³⁾	12	—	15	—	20	—	25	—	ns
t _{RTS}	Retransmit Set-up Time ⁽⁴⁾	12	—	15	—	20	—	25	—	ns
t _{RTTR}	Retransmit Recovery Time	8	—	10	—	10	—	10	—	ns
t _{EFL}	Reset to Empty Flag Low	—	12	—	25	—	30	—	35	ns
t _{HFH,FFH}	Reset to Half-Full and Full Flag High	—	17	—	25	—	30	—	35	ns
t _{RTF}	Retransmit Low to Flags Valid	—	20	—	25	—	30	—	35	ns
t _{REF}	Read Low to Empty Flag Low	—	12	—	15	—	20	—	25	ns
t _{RFH}	Read High to Full Flag High	—	14	—	15	—	20	—	25	ns
t _{RPE}	Read Pulse Width after EF High	12	—	15	—	20	—	25	—	ns
t _{WEF}	Write High to Empty Flag High	—	12	—	15	—	20	—	25	ns
t _{WFF}	Write Low to Full Flag Low	—	14	—	15	—	20	—	25	ns
t _{WHF}	Write Low to Half-Full Flag Low	—	17	—	25	—	30	—	35	ns
t _{RHF}	Read High to Half-Full Flag High	—	17	—	25	—	30	—	35	ns
t _{WPF}	Write Pulse Width after FF High	12	—	15	—	20	—	25	—	ns
t _{XOL}	Read/Write to X0 Low	—	12	—	15	—	20	—	25	ns
t _{XOH}	Read/Write to X0 High	—	12	—	15	—	20	—	25	ns
t _{XI}	X1 Pulse Width ⁽³⁾	12	—	15	—	20	—	25	—	ns
t _{XIR}	X1 Recovery Time	8	—	10	—	10	—	10	—	ns
t _{XIS}	X1 Set-up Time	8	—	10	—	10	—	10	—	ns

NOTES:

1. Timings referenced as in AC Test Conditions.
2. Industrial temperature range product for 15ns and 25ns speed grades are available as a standard device.
3. Pulse widths less than minimum value are not allowed.
4. Values guaranteed by design, not currently tested.
5. Only applies to read data flow-through mode

AC ELECTRICAL CHARACTERISTICS⁽¹⁾ (Continued)

(Commercial: $V_{CC} = 5V \pm 10\%$, $T_A = 0^\circ C$ to $+70^\circ C$; Industrial: $V_{CC} = 5V \pm 10\%$, $T_A = -40^\circ C$ to $+85^\circ C$; Military: $V_{CC} = 5V \pm 10\%$, $T_A = -55^\circ C$ to $+125^\circ C$)

Symbol	Parameter	Military		Commercial		Com'l & Mil. ⁽²⁾		Military ⁽²⁾		Unit
		IDT7200L30 IDT7201LA30 IDT7202LA30		IDT7200L35 IDT7201LA35 IDT7202LA35		IDT7200L50 IDT7201LA50 IDT7202LA50		IDT7201LA80		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _S	Shift Frequency	—	25	—	22.2	—	15	—	10	MHz
t _{RC}	Read Cycle Time	40	—	45	—	65	—	100	—	ns
t _A	Access Time	—	30	—	35	—	50	—	80	ns
t _{RR}	Read Recovery Time	10	—	10	—	15	—	20	—	ns
t _{RPW}	Read Pulse Width ⁽³⁾	30	—	35	—	50	—	80	—	ns
t _{RLZ}	Read Pulse Low to Data Bus at Low Z ⁽⁴⁾	3	—	3	—	3	—	3	—	ns
t _{WLZ}	Write Pulse High to Data Bus at Low Z ^(4, 5)	5	—	5	—	5	—	5	—	ns
t _{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns
t _{RHZ}	Read Pulse High to Data Bus at High Z ⁽⁴⁾	—	20	—	20	—	30	—	30	ns
t _{WC}	Write Cycle Time	40	—	45	—	65	—	100	—	ns
t _{WPW}	Write Pulse Width ⁽³⁾	30	—	35	—	50	—	80	—	ns
t _{WR}	Write Recovery Time	10	—	10	—	15	—	20	—	ns
t _{DS}	Data Set-up Time	18	—	18	—	30	—	40	—	ns
t _{DH}	Data Hold Time	0	—	0	—	5	—	10	—	ns
t _{RSC}	Reset Cycle Time	40	—	45	—	65	—	100	—	ns
t _{RS}	Reset Pulse Width ⁽³⁾	30	—	35	—	50	—	80	—	ns
t _{RSS}	Reset Set-up Time ⁽⁴⁾	30	—	35	—	50	—	80	—	ns
t _{RSR}	Reset Recovery Time	10	—	10	—	15	—	20	—	ns
t _{RTC}	Retransmit Cycle Time	40	—	45	—	65	—	100	—	ns
t _{RT}	Retransmit Pulse Width ⁽³⁾	30	—	35	—	50	—	80	—	ns
t _{RTS}	Retransmit Set-up Time ⁽⁴⁾	30	—	35	—	50	—	80	—	ns
t _{TRR}	Retransmit Recovery Time	10	—	10	—	15	—	20	—	ns
t _{EFL}	Reset to Empty Flag Low	—	40	—	45	—	65	—	100	ns
t _{HFH, FFH}	Reset to Half-Full and Full Flag High	—	40	—	45	—	65	—	100	ns
t _{RTF}	Retransmit Low to Flags Valid	—	40	—	45	—	65	—	100	ns
t _{REF}	Read Low to Empty Flag Low	—	30	—	30	—	45	—	60	ns
t _{RFF}	Read High to Full Flag High	—	30	—	30	—	45	—	60	ns
t _{RPE}	Read Pulse Width after EF High	30	—	35	—	50	—	80	—	ns
t _{WEF}	Write High to Empty Flag High	—	30	—	30	—	45	—	60	ns
t _{WFF}	Write Low to Full Flag Low	—	30	—	30	—	45	—	60	ns
t _{WHF}	Write Low to Half-Full Flag Low	—	40	—	45	—	65	—	100	ns
t _{RHF}	Read High to Half-Full Flag High	—	40	—	45	—	65	—	100	ns
t _{WPF}	Write Pulse Width after FF High	30	—	35	—	50	—	80	—	ns
t _{XOL}	Read/Write to X $\overline{O}$ Low	—	30	—	35	—	50	—	80	ns
t _{XOH}	Read/Write to X $\overline{O}$ High	—	30	—	35	—	50	—	80	ns
t _{XI}	X $\overline{I}$ Pulse Width ⁽³⁾	30	—	35	—	50	—	80	—	ns
t _{XIR}	X $\overline{I}$ Recovery Time	10	—	10	—	10	—	10	—	ns
t _{XIS}	X $\overline{I}$ Set-up Time	10	—	10	—	15	—	15	—	ns

NOTES:

1. Timings referenced as in AC Test Conditions
2. Military speed grades of 50ns and 80ns are only available for IDT7201LA.
3. Pulse widths less than minimum value are not allowed.
4. Values guaranteed by design, not currently tested.
5. Only applies to read data flow-through mode.

SIGNAL DESCRIPTIONS

INPUTS:

DATA IN (D₀ – D₈)

Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the HIGH state during the window shown in Figure 2, (i.e., t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be reset to HIGH after Reset ($\overline{RS}$).**

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go HIGH after t_{RFF} , allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes HIGH, the Data Outputs (Q₀–Q₈) will return to a high impedance condition until the next Read operation. When all data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, allowing the “final” read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL/RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single

Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7200/7201A/7202A can be made to retransmit data when the Retransmit Enable control ($\overline{RT}$) input is pulsed LOW. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the HIGH state during retransmit. This feature is useful when less than 256/512/1,024 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operation, when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full-Flag ($\overline{FF}$) will go LOW after 256 writes for IDT7200, 512 writes for the IDT7201A and 1,024 writes for the IDT7202A.

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO/HF}$)

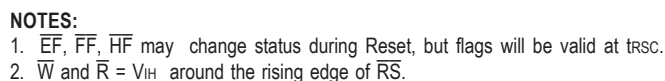
This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by using rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS (Q₀ – Q₈)

Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read ($\overline{R}$) is in a HIGH state.



The timing diagram illustrates the relationship between the $\overline{R}$ (Reset), Q_0-Q_8 (Data Out), and $\overline{W}$ (Write Enable) signals. The diagram shows two data transfer cycles. Key timing parameters are defined as follows:

- t_{RC} : Reset to Command delay (from $\overline{R}$ falling edge to first command).
- t_A : Access time (from command to data output).
- t_{RR} : Read to Read delay (between consecutive read commands).
- t_{RPW} : Read to Precharge delay (from read command to precharge).
- t_{RLZ} : Read Latency (from $\overline{R}$ falling edge to data output).
- t_{DV} : Data Valid time (duration of data output).
- t_{RHZ} : Read Hold time (from data output to $\overline{R}$ rising edge).
- t_{WC} : Write to Command delay (from $\overline{W}$ falling edge to first command).
- t_{WPW} : Write to Precharge delay (from write command to precharge).
- t_{WR} : Write to Read delay (between write and read commands).
- t_{DS} : Data Setup time (before data input).
- t_{DH} : Data Hold time (after data input).

The diagram shows that data output is valid during read operations and data input is valid during write operations. The signals Q_0-Q_8 and D_0-D_8 are shown as data buses.

The diagram illustrates the timing relationships between the Read ($\overline{R}$), Write ($\overline{W}$), and Flash Enable ($\overline{FF}$) signals during different memory operations. The operations are divided into five phases: LAST WRITE, IGNORED WRITE, FIRST READ, ADDITIONAL READS, and FIRST WRITE.

- LAST WRITE:** $\overline{W}$ is active (low). $\overline{FF}$ is active (low). t_{WFF} is the time from the start of $\overline{W}$ to the start of $\overline{FF}$.
- IGNORED WRITE:** $\overline{W}$ is active (low). $\overline{FF}$ is inactive (high).
- FIRST READ:** $\overline{R}$ is active (low). $\overline{FF}$ is active (low). t_{RFF} is the time from the start of $\overline{R}$ to the start of $\overline{FF}$.
- ADDITIONAL READS:** $\overline{R}$ is active (low). $\overline{FF}$ is inactive (high).
- FIRST WRITE:** $\overline{W}$ is active (low). $\overline{FF}$ is inactive (high).

2679 drw 06

Figure 4. Full Flag From Last Write to First Read

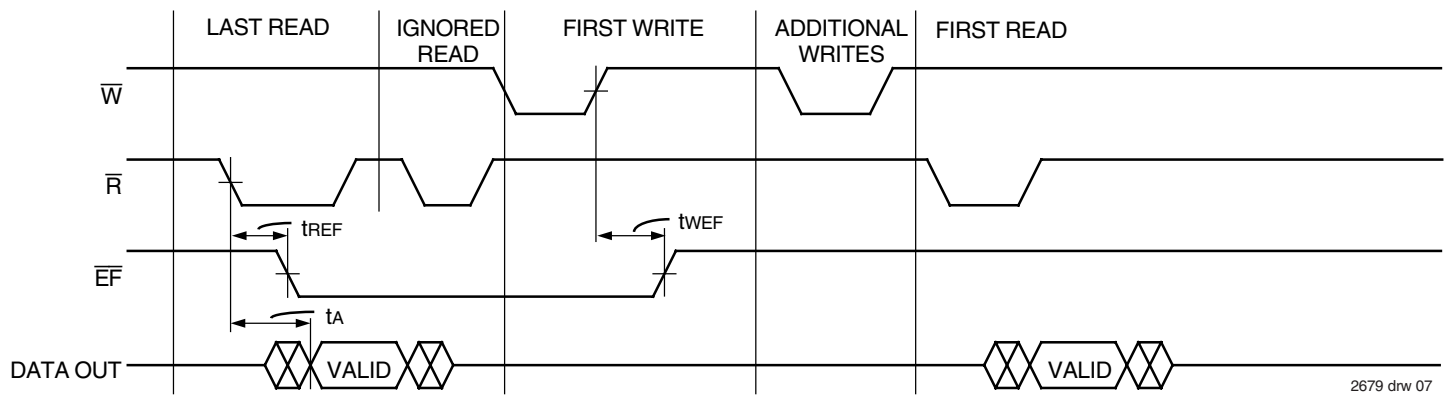


Figure 5. Empty Flag From Last Read to First Write

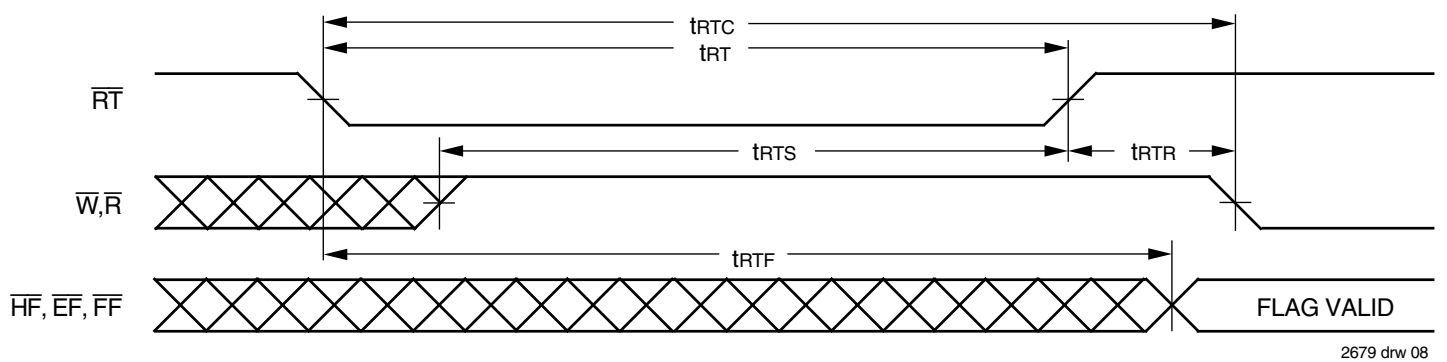


Figure 6. Retransmit

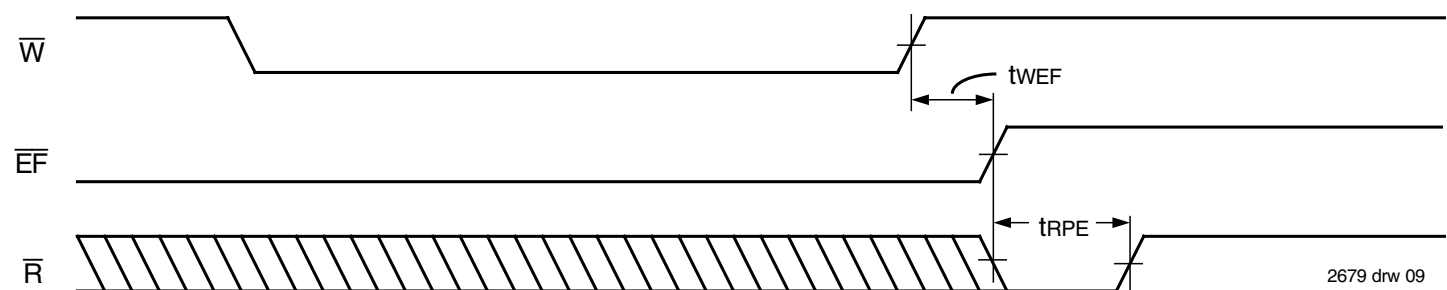


Figure 7. Minimum Timing for an Empty Flag Coincident Read Pulse

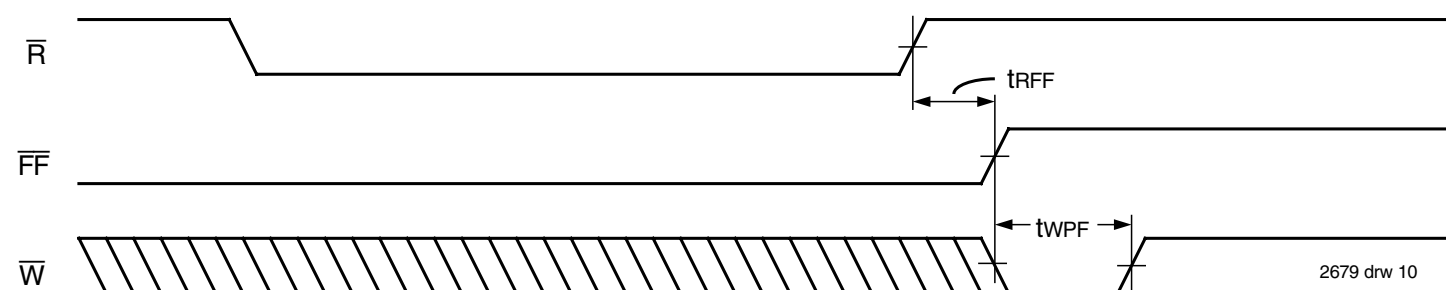
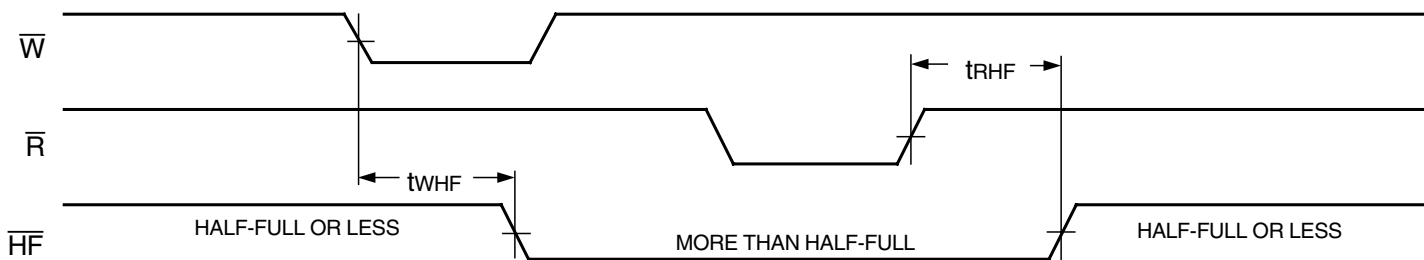
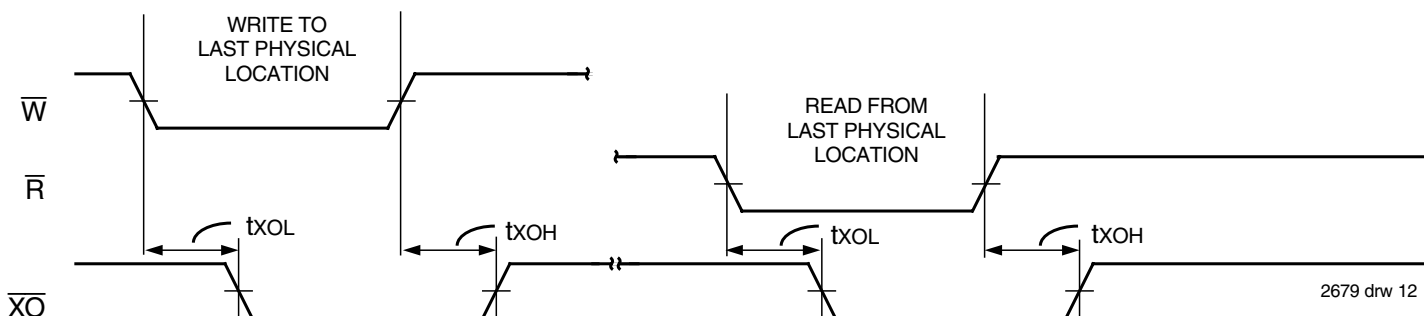


Figure 8. Minimum Timing for a Full Flag Coincident Write Pulse



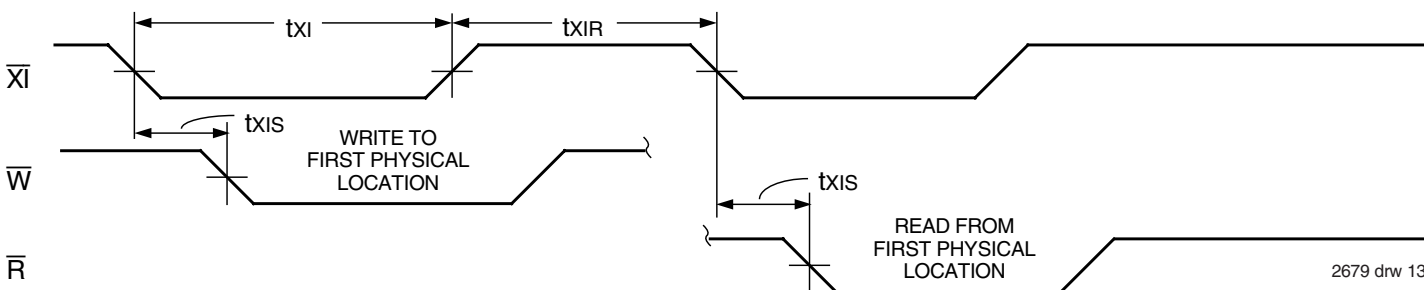
2679 drw 11

Figure 9. Half-Full Flag Timing



2679 drw 12

Figure 10. Expansion Out



2679 drw 13

Figure 11. Expansion In

OPERATING MODES:

Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). For additional information, refer to Tech Note 8: *Operating FIFOs on Full and Empty Boundary Conditions* and Tech Note 6: *Designing with FIFOs*.

SINGLE DEVICE MODE

A single IDT7200/7201A/7202A may be used when the application requirements are for 256/512/1,024 words or less. These devices are in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12).

DEPTH EXPANSION

The IDT7200/7201A/7202A can easily be adapted to applications when the requirements are for greater than 256/512/1,024 words. Figure 14 demonstrates Depth Expansion using three IDT7200/7201A/7202As. Any

depth can be attained by adding additional IDT7200/7201A/7202As. These FIFOs operate in the Depth Expansion mode when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$ s and ORing of all $\overline{FF}$ s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information, refer to Tech Note 9: *Cascading FIFOs or FIFO Modules*.

USAGE MODES:

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7200/7201A/7202As. Any word width can be attained by adding additional IDT7200/7201A/7202As (Figure 13).

BIDIRECTIONAL OPERATION

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7200/7201A/7202As as shown in Figure 16. Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH

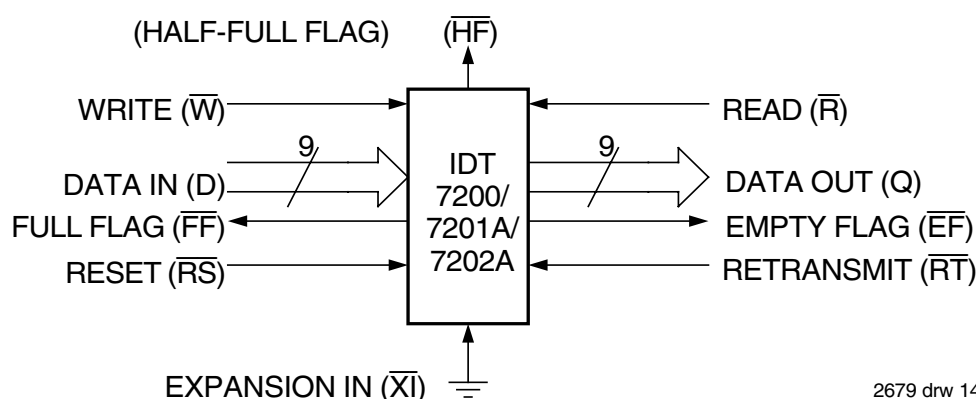
Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17),

the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from LOW-to-HIGH, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line being LOW causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

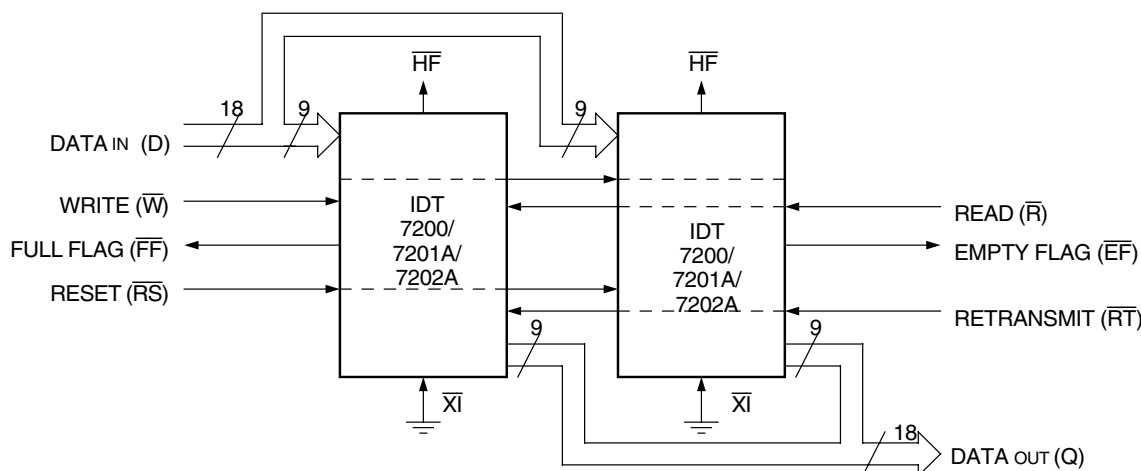
COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).



2679 drw 14

Figure 12. Block Diagram of Single 256 x 9, 512 x 9, 1,024 x 9 FIFO



2679 drw 15

Figure 13. Block Diagram of 256 x 18, 512 x 18, 1,024 x 18 FIFO Memory Used in Width Expansion Mode

TABLE 1 — RESET AND RETRANSMIT

Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment ⁽¹⁾	Increment ⁽¹⁾	X	X	X

NOTE:

1. Pointer will increment if flag is HIGH.

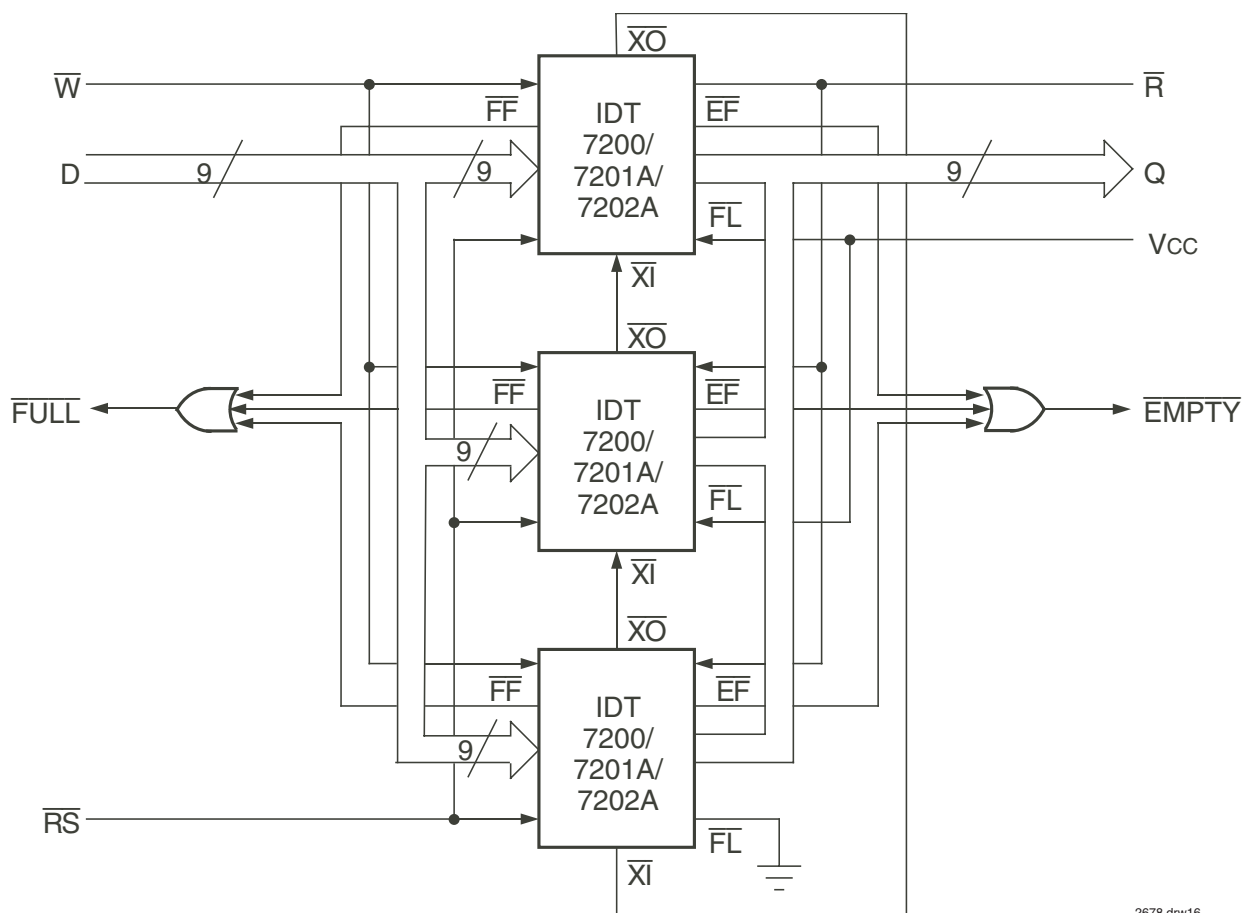
TABLE 2 — RESET AND FIRST LOAD TRUTH TABLE

Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

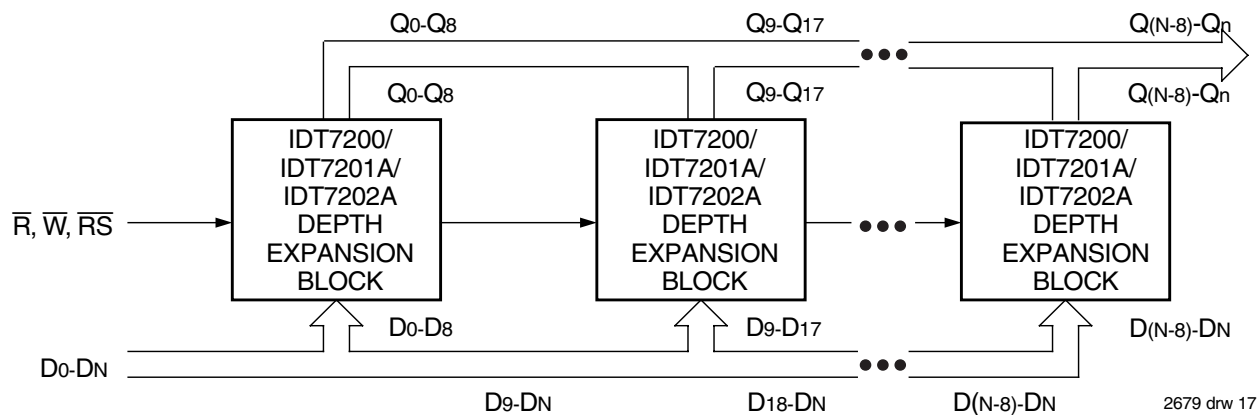
NOTE:

1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output



2678 drw16

Figure 14. Block Diagram of 768 x 9, 1,536 x 9, 3,072 x 9 FIFO Memory (Depth Expansion)



NOTES:

1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For flag detection see section on Width Expansion and Figure 13.

Figure 15. Compound FIFO Expansion

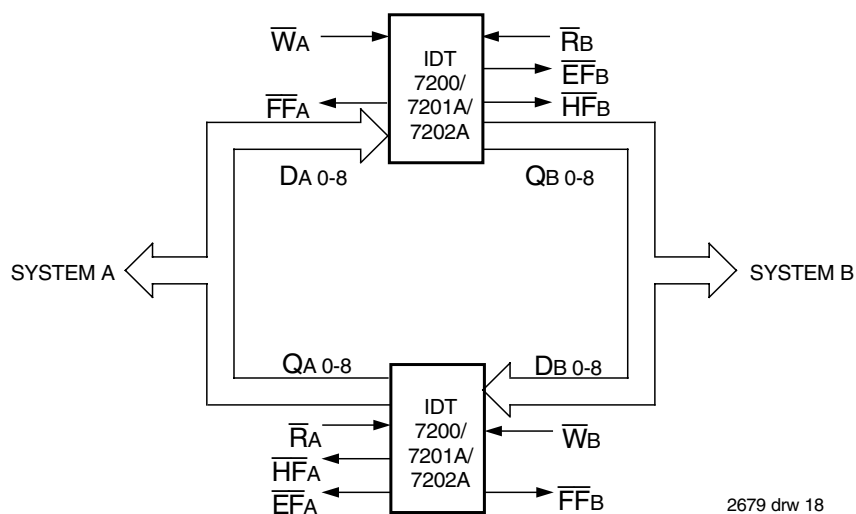


Figure 16. Bidirectional FIFO Mode

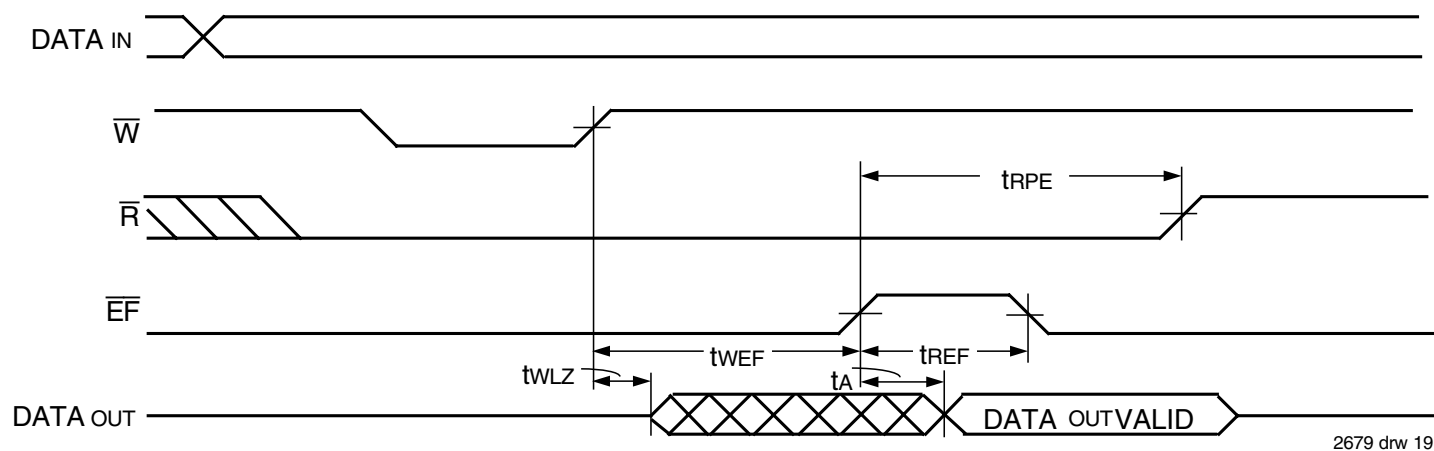


Figure 17. Read Data Flow-Through Mode

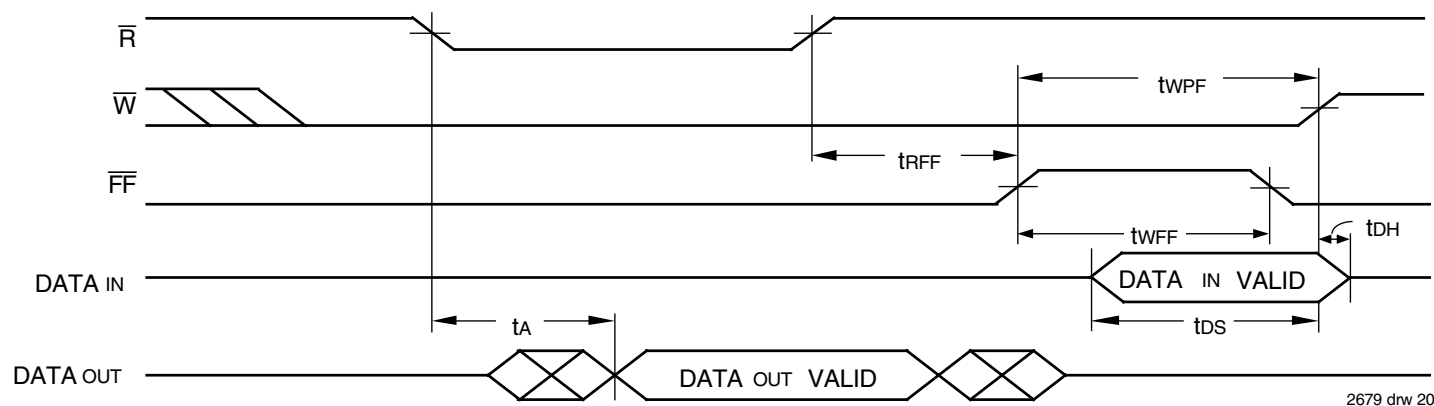


Figure 18. Write Data Flow-Through Mode

XXXX	X	XXX	X	X	X	X					
Device Type	Power	Speed	Package		Process/ Temperature Range						
							Blank 8	Tube or Tray Tape and Reel			
							Blank I ⁽¹⁾ B	Commercial (0°C to +70°C) Industrial (-40°C to +85°C) Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B			
							G ⁽³⁾	Green			
							P ⁽⁴⁾ TP D TD J SO L	Plastic DIP Plastic Thin DIP CERDIP Thin CERDIP Plastic Leaded Chip Carrier SOIC Leadless Chip Carrier	PLCC LCC	P28-1 P28-2 D28-1 D28-3 J32-1 SO28-3 L32-1	(7201 & 7202 Only) (7201 & 7202 Only) (7201 & 7202 Only)
							12 15 20 25 30 35 50 80	Commercial Only Commercial and Industrial Commercial and Military Commercial and Industrial Military Only Commercial Only Commercial and (Military only for 7201) Military only for 7201			Access Time (t _A) Speed in Nanoseconds
							LA ⁽²⁾	Low Power			
							7200 7201 7202 7280 7281 7282	256 x 9-Bit FIFO 512 x 9-Bit FIFO 1,024 x 9-Bit FIFO 256 x 9-Bit DUAL FIFO 512 x 9-Bit DUAL FIFO 1,024 x 9-Bit DUAL FIFO			See 7280/7281/7282 data sheet for details

1. Industrial temperature range product is available for the 15ns and 25ns as a standard product.
2. "A" to be included for IDT7201 and IDT7202 ordering part number.
3. Green parts are available. For specific speeds and packages contact your local sales office.
4. For "P", Plastic Dip, when ordering green package, the suffix is "PDG".

05/02/2001 pgs. 1, 2, 3, 4, 5 and 14.
04/03/2006 pgs. 1 and 14.
10/22/2008 pg. 1.
6/29/2012 pgs. 1 and 14.



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