LCD driver for segment-type LCDs
BU9728AKV

The BU9728AKV is a segment-type LCD system driver which can accommodate microcomputer control and a serial interface. An internal 4-bit common output and LCD drive power supply circuit enable configuration of a display system at low cost.

●Applications

Movie projectors, car audio systems, telephones

●Features

1) Serial interface. (8-bit length)
2) Display RAM: Internal, 128 bits. (up to 128 segments can be displayed)
3) Internal power supply circuit for LCD drive.
4) Display duty: 1 / 4
5) Can be driven with low voltage and low current dissipation.

●Absolute maximum ratings (Ta = 25°C, V_{SS} = 0V)

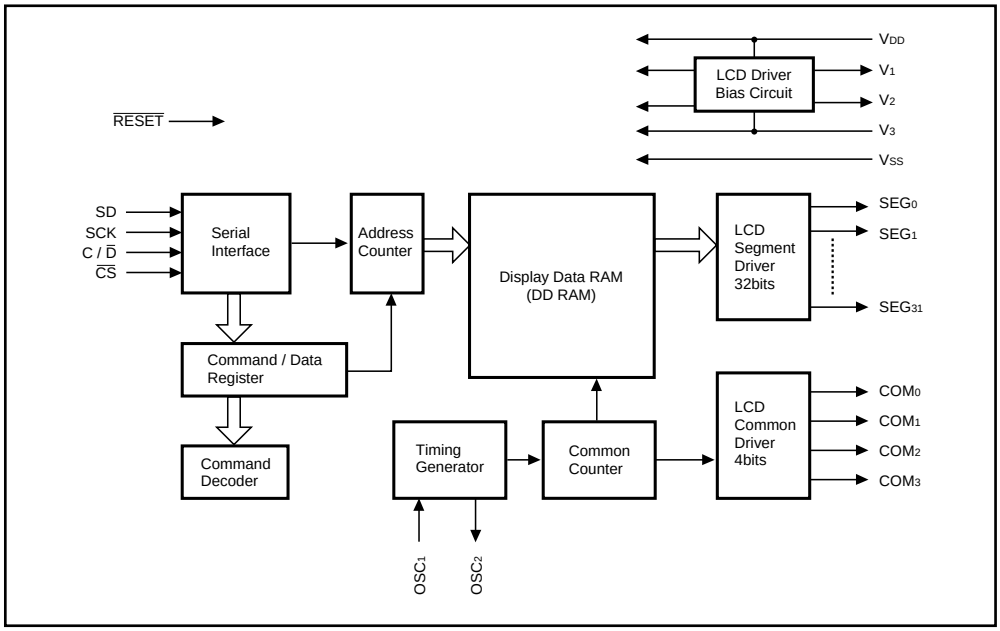
Parameter	Symbol	Limits	Unit
Power supply voltage 1	V_{DD}	– 0.3 ~ + 7.0	V
Power supply voltage 2	V_{LCD}	– 0.3 ~ + V_{DD}	V
Power dissipation	Pd	400*	mW
Operating temperature	Topr	– 20 ~ + 75	°C
Storage temperature	Tstg	– 55 ~ + 125	°C

* Reduced by 4.0mW for each increase in Ta of 1°C over 25°C .

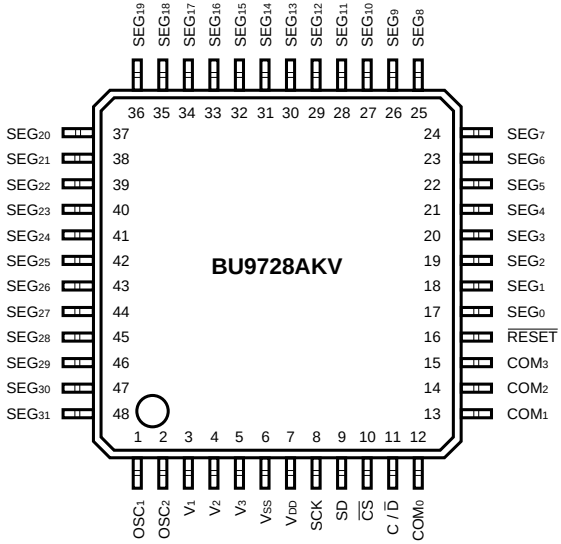
●Recommended operating conditions (Ta = 25°C, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply voltage 1	V_{DD}	2.5	—	5.5	V	—
Power supply voltage 2 (V_{DD} - V_3)	V_{LCD}	0	—	V_{DD}	V	The following relationship should be maintained: $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_{SS}$.
Oscillation frequency	f_{OSC}	—	36	—	kHz	R_f = 470kΩ

●Block diagram



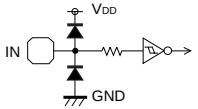
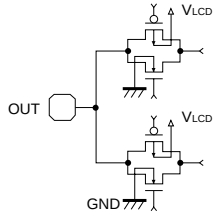
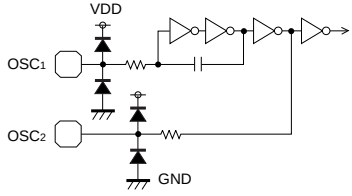
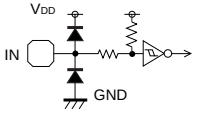
●Pin assignments



●Pin descriptions

Pin name	Pin NO.	I / O	Function
OSC_1 OSC_2	1 2	I O	Input / output pins for the internal oscillator. Resistance is connected between these pins when the internal clock is running. When an external clock is running, the clock is input from OSC_1 and OSC_2 is left open.
$V_1 \sim V_3$	3 ~ 5	—	These are power supply pins for LCD drive. The following relationship must be satisfied: $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_{SS}$ (Low) .
V_{SS}	6	—	This is the V_{SS} power supply pin.
V_{DD}	7	—	This is the V_{DD} power supply pin.
SCK	8	I	This is the shift clock input pin for serial data. The contents of the SD pin are read one bit at a time at the rising edge of SCK.
SD	9	I	This is the serial data input pin, used to input display data and commands. Display data is displayed when this is "1" and not displayed when it is "0".
$\overline{CS}$	10	I	This is the chip select signal input pin. When this pin is LOW, SD input can be received. The SCK counter is reset when the $\overline{CS}$ pin goes from HIGH to LOW.
C / $\overline{D}$	11	I	This signal detects whether the SD input is command or display data. If the pin is LOW at the rising edge of the 8th SCK pulse, the input is recognized as display data, and if HIGH, the input is recognized as command data.
COM_0 ʃ COM_3	12 ~ 15	O	These are the common output pins for LCD drive. They are connected to the LCD panel commons.
$\overline{RESET}$	16	I	This is the reset input pin. When this pin is LOW, the BU9728AKV is initialized. It resets the address counter and turns the display off.
SEG_0 ʃ SEG_{31}	17 ~ 48	O	These are the segment output pins for LCD drive. They are connected to the LCD panel segments.

●Input / output equivalent circuits

Pin name	I / O	Equivalent Circuit	Pin name	I / O	Equivalent Circuit
SD SCK C / $\overline{D}$ $\overline{CS}$	I		SEG_0 ʃ SEG_{31} COM_0 ʃ COM_3	O	
OSC_1 OSC_2	—				
$\overline{RESET}$	I				

●Electrical characteristics

DC characteristics (unless otherwise noted, V_{DD} = 2.5 ~ 5.5V, V_{SS} = 0V, Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Pin
Input high level voltage	V_{IH1}	0.8 × V_{DD}	—	V_{DD}	V	—	OSC_1, SD, SCK, C / $\overline{D}$, $\overline{CS}$ $\overline{RESET}$
Input low level voltage	V_{IL1}	0	—	0.2 × V_{DD}	V	—	
LCD driver ON resistance*1	R_{ON}	—	—	30	kΩ	$\lvert \Delta V_{ON} \rvert$ = 0.1V	$SEG_{0 \sim 31}$, $COM_{0 \sim 3}$
Input low level current 1	I_{IL1}	—	—	100	µA	V_{IN} = 0V	$\overline{RESET}$
Input low level current 2	I_{IL2}	—	—	2	µA	V_{IN} = 0V	OSC_1, SD, SCK, C / $\overline{D}$, $\overline{CS}$
Input high level current	I_{IH}	– 2	—	—	µA	V_{IN} = V_{DD}	OSC_1, SD, SCK, C / $\overline{D}$, $\overline{CS}$, $\overline{RESET}$
Input capacitance	C_{IN}	—	5	—	pF	—	SD, SCK, C / $\overline{D}$, $\overline{CS}$
Current dissipation	I_{DD}	—	0.05	1	µA	In wait state*2	V_{DD}
		—	40	80	µA	When display is operating*3	
		—	100	250	µA	During access operation*4	

*1 Internal power supply impedance is not included in the LCD driver ON resistance.

*2 All inputs, including V_3 = 0V and OSC_1, are fixed at either V_{DD} or V_{SS}.

*3 Except for V_3 = 0V, Rf = 470kΩ , and OSC_1, all inputs are fixed at either V_{DD} or V_{SS}.

*4 V_3 = 0V, Rf = 470kΩ , f_{SCK} = 200kHz

AC characteristics (unless otherwise noted, V_{DD} = 2.5 ~ 5.5V, V_{SS} = 0V, Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
SCK rise time	t_{TLH}	—	—	100	ns	—
SCK fall time	t_{THL}	—	—	100	ns	—
SCK cycle time	t_{CYC}	800	—	—	ns	—
Command wait time	t_{WAIT}	800	—	—	ns	—
SCK pulse width "H"	t_{WH1}	300	—	—	ns	—
SCK pulse width "L"	t_{WL1}	300	—	—	ns	—
Data setup time	t_{SU1}	100	—	—	ns	—
Data hold time	t_{H1}	100	—	—	ns	—
$\overline{CS}$ pulse width "H"	t_{WH2}	300	—	—	ns	—
$\overline{CS}$ pulse width "L"	t_{WL2}	6400	—	—	ns	—
$\overline{CS}$ set-up time	t_{SU2}	100	—	—	ns	—
$\overline{CS}$ hold time	t_{H2}	100	—	—	ns	—
C / $\overline{D}$ set-up time	t_{SU3}	100	—	—	ns	—
C / $\overline{D}$ hold time	t_{H3}	100	—	—	ns	Use rise for 8th CK of SCK as standard
C / $\overline{D}$ - $\overline{CS}$ time*5	t_{CCH}	100	—	—	ns	Use $\overline{CS}$ riss as standard
C / $\overline{D}$ - SCK time*5	t_{SCH}	100	—	—	ns	Use rise for 8th CK of SCK as standard

*5 Only one (either one) of the conditions needs to be satisfied.

●Timing charts

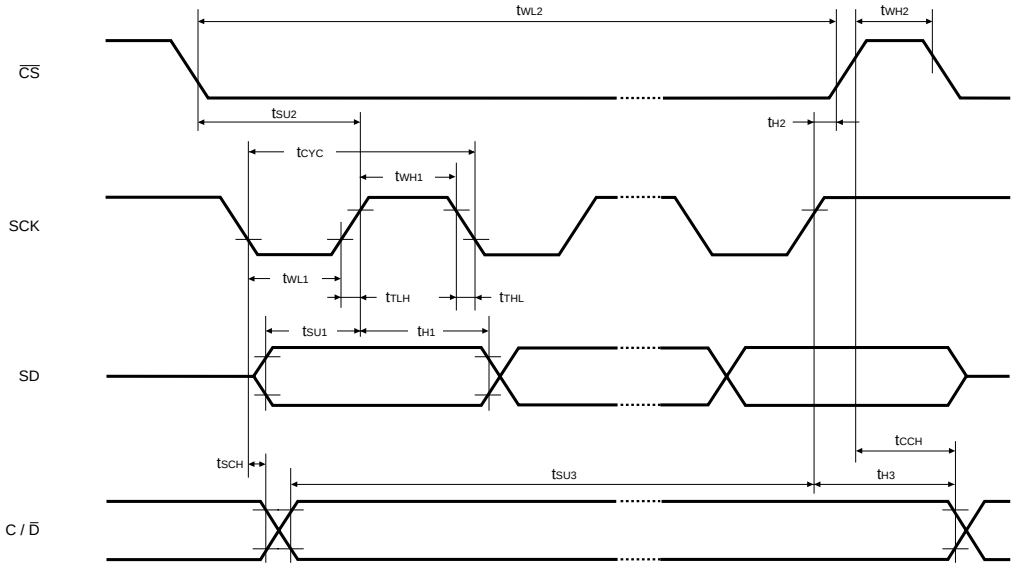


Fig.1 Interface timing

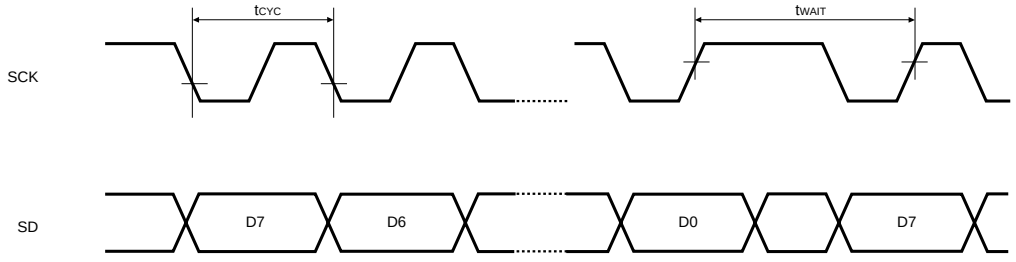


Fig.2 Command cycle

●Data format

Serial data is 4-line data transmitted in synchronization with the clock. Serial data with a bit length of 8 bits is input in synchronization with SCK. If C / D is HIGH at the rising edge of the 8 × nth SCK clock pulse, the serial data is recognized as command data, and if C / D is LOW, the serial data is recognized as display data. Serial data is input in sequential order, starting from the MSB.

●A detailed look at commands

The BU9728AKV has the following commands (C / D is HIGH at 8 × nth clock pulse of SCK).

(1) Address Set

MSB							LSB
0	0	0	A	A	A	A	A

AAAAA and the address data displayed in binary format are set in the address counter. Each time input of the display data (8 bits) has been completed, the address is incremented by + 2.

(2) Display On

MSB							LSB	
0	0	1	*	*	*	*	*	* Irrelevant

All display segments light, regardless of the contents of the Display Data RAM (DDRAM). The contents of the DDRAM do not change.

(3) Display Off

MSB							LSB	
0	1	0	*	*	*	*	*	* Irrelevant

All display segments go out, regardless of the contents of the DDRAM. The contents of the DDRAM do not change.

(4) Display Start

MSB							LSB	
0	1	1	*	*	*	*	*	* Irrelevant

Display begins, in accordance with the contents of the DDRAM.

(5) Rewrite Display Data RAM (DDRAM)

MSB							LSB	
1	0	0	*	D	D	D	D	* Irrelevant

The binary bit data DDDD is written to the DDRAM. The data is written to the address specified by the Address Set command, and after this command is executed, the address is automatically incremented by + 1.

(6) Reset

MSB							LSB	
1	1	0	*	*	*	*	*	* Irrelevant

This command should be executed before any other command, immediately after the power supply is turned on. This command resets the BU9728AKV to the following status:

- Display is off
- Address counter is reset

●Description of functions

(1) Register

The BU9728AKV has a command / data register configured of eight bits. Serial data is read in 8-pulse units of the SCK clock.

If the data read to the register is display data (C / $\overline{D}$ is LOW at the 8th clock pulse of SCK), it is written to the DDRAM, and if the data is command data (C / $\overline{D}$ is HIGH at the 8th clock pulse of SCK), it is output to a command decoder and used to control the BU9728AKV.

(2) Address counter

The address counter indicates the DDRAM address. When the set address is written to the command / data register, the address data is automatically sent to the address counter.

After the data is written to the DDRAM, the address counter is automatically incremented by either + 1 or + 2. The amount by which the counter is incremented is determined automatically, based on the following statuses:

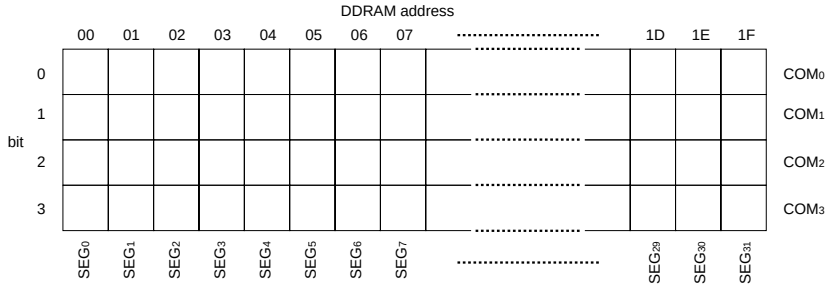
8 bits written to DDRAM (C / $\overline{D}$ LOW at 8th clock pulse of SCK) $\rightarrow$ + 2

4 bits written to DDRAM (C / $\overline{D}$ HIGH at 8th clock pulse of SCK) $\rightarrow$ + 1

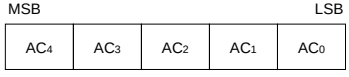
When the address counter reaches 1FH, it will be reset back to 00H the next time it is incremented.

(3) Display Data RAM (DDRAM)

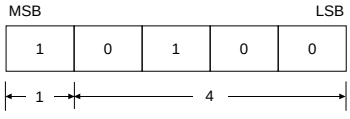
The Display Data RAM (DDRAM) is where displays are stored. The capacity of the DDRAM is 32 addresses $\times$ 4 bits. The illustration below shows the relationship between the DDRAM and the display positions.



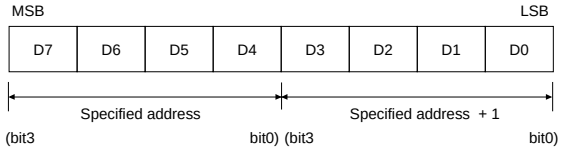
DDRAM addresses set in the address counter are in hexadecimal format and are indicated as follows.



(Example) For a DDRAM address of “14” (display position: SEG_{20})

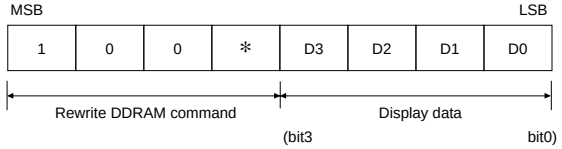


The display data input to the command / data register (when C / $\overline{D}$ is LOW) is written to the DDRAM address and the address consisting of the specified address + 1, which are indicated by the upper four and lower four bits of the data, respectively. The four bits of the display data are written sequentially, starting from the MSB, to the MSB of the DDRAM bits.



If the Rewrite DDRAM command is input (C / $\overline{D}$ is HIGH), the four bits of the display data in the Rewrite DDRAM command are written to the specified DDRAM address.

The four bits of the display data are written sequentially, starting from the MSB, to the MSB of the DDRAM bits.



(4) Timing generator

Connecting Rf between OSC_1 and OSC_2 causes the internal oscillator circuit to start oscillating, and generates a display timing signal. The oscillator can also be started by inputting an external clock.

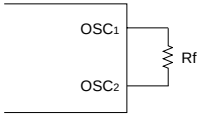


Fig. 3 Rf oscillator circuit

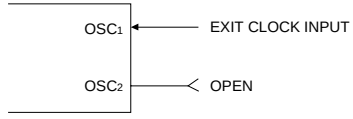


Fig. 4 External clock input

(5) LCD drive power supply

The LCD drive power supply is generated by the BU9728AKV. The LCD drive voltage (V_{LCD}) is supplied by V_{DD} - V_3, and the power supply is generated by $V_1 = 2 \bullet V_{LCD} / 3$, $V_2 = V_{LCD} / 3$.

If an external bleeder resistance is used to supply the LCD drive voltage externally, the following relationship must be observed:

$V_{DD} = V_1 \geqq V_2 \geqq V_3 \geqq V_{SS}$

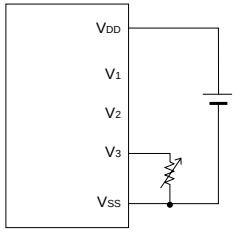


Fig. 5 Example of connection when using internal power supply

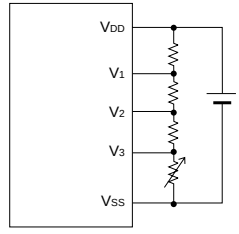


Fig. 6 Example of connection when using external power supply

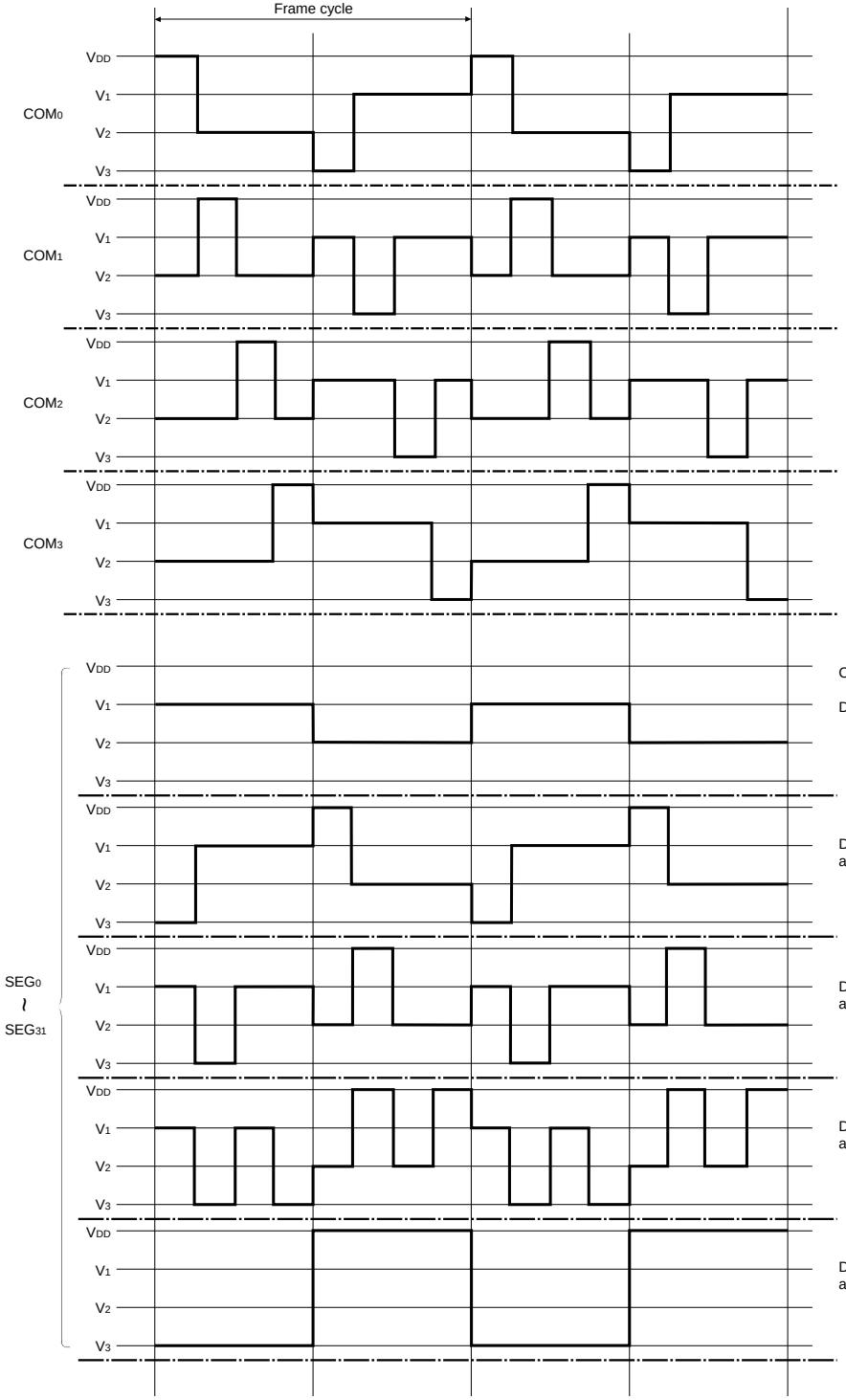
(6) LCD drive circuit

The LCD drive circuit is configured of four common drivers and 32 segment drivers. When oscillation begins, selected waveforms are output automatically for valid common outputs by the common counter, and de-selected waveforms are output for other outputs.

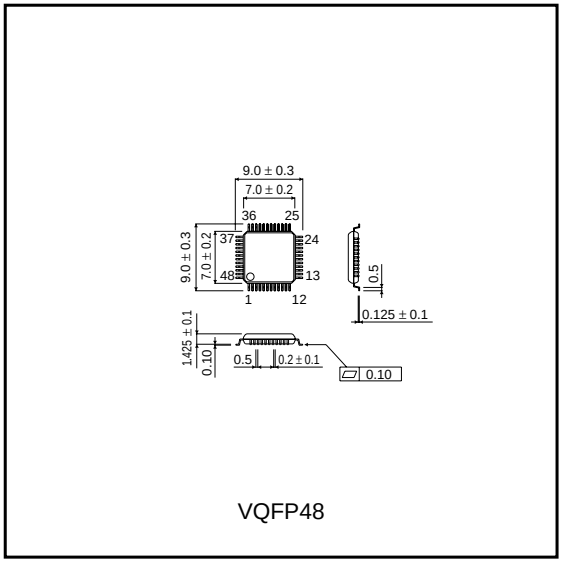
For segment outputs, drive waveforms are output automatically by the display data and common counter.

The following page shows examples of common / segment output waveforms.

●LCD drive waveforms



●External dimensions (Units: mm)



VQFP48