ANALOG DEVICES

Stereo, 24-Bit, 192 kHz, Multibit $\Sigma\Delta$ DAC
AD1853

FEATURES
5 V Stereo Audio DAC System
Accepts 16-/18-/20-/24-Bit Data
Supports 24 Bits and 192 kHz Sample Rate
Accepts a Wide Range of Sample Rates Including:
  32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz and 192 kHz
Multibit Sigma-Delta Modulator with "Perfect Differential Linearity Restoration" for Reduced Idle Tones and Noise Floor
Data Directed Scrambling DAC—Least Sensitive to Jitter
Differential Output for Optimum Performance
120 dB Signal to Noise (Not Muted) at 48 kHz (A-Weighted Mono)
117 dB Signal to Noise (Not Muted) at 48 kHz (A-Weighted Stereo)
119 dB Dynamic Range (Not Muted) at 48 kHz Sample Rate (A-Weighted Mono)
116 dB Dynamic Range (Not Muted) at 48 kHz Sample Rate (A-Weighted Stereo)
–107 dB THD+N (Mono Application Circuit, See Figure 30)
–104 dB THD+N (Stereo)
115 dB Stopband Attenuation (96 kHz)
On-Chip Clickless Volume Control
Hardware and Software Controllable Clickless Mute
Serial (SPI) Control for: Serial Mode, Number of Bits, Interpolation Factor, Volume, Mute, De-Emphasis, Reset
Digital De-Emphasis Processing for 32, 44.1 and 48 kHz Sample Rates
Clock Auto-Divide Circuit Supports Five Master-Clock Frequencies
Flexible Serial Data Port with Right-Justified, Left-Justified, I²S-Compatible and DSP Serial Port Modes
28-Lead SSOP Plastic Package

APPLICATIONS
Hi End: DVD, CD, Home Theater Systems, Automotive Audio Systems, Sampling Musical Keyboards, Digital Mixing Consoles, Digital Audio Effects Processors

PRODUCT OVERVIEW
The AD1853 is a complete high performance single-chip stereo digital audio playback system. It is comprised of a high performance digital interpolation filter, a multibit sigma-delta modulator, and a continuous-time current-out analog DAC section. Other features include an on-chip clickless stereo attenuator and mute capability, programmed through an SPI-compatible serial control port. The AD1853 is fully compatible with all known DVD formats and supports 48 kHz, 96 kHz and 192 kHz sample rates with up to 24 bits word lengths. It also provides the "Redbook" standard 50 µs/15 µs digital de-emphasis filters at sample rates of 32 kHz, 44.1 kHz and 48 kHz.

The AD1853 has a very flexible serial data input port that allows for glueless interconnection to a variety of ADCs, DSP chips, AES/EBU receivers and sample rate converters. The AD1853 can be configured in left-justified, I²S, right-justified, or DSP serial port compatible modes. The AD1853 accepts serial audio data in MSB first, twos complement format.

The AD1853 operates from a single +5 V power supply. It is fabricated on a single monolithic integrated circuit and is housed in a 28-lead SSOP package for operation over the temperature range 0°C to +70°C.

FUNCTIONAL BLOCK DIAGRAM
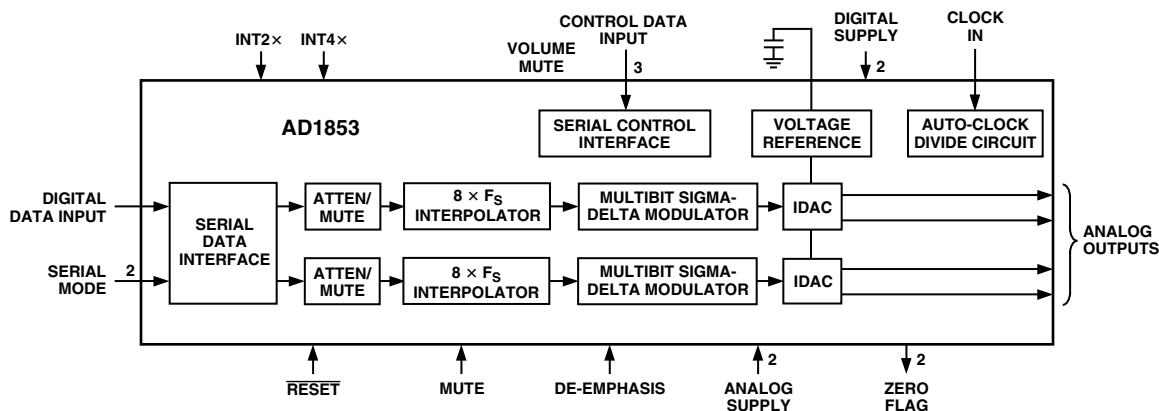
AD1853* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-211: The Alexander Current-Feedback Audio Power Amplifier
- AN-327: DAC ICs: How Many Bits Is Enough?

Data Sheet

- AD1853: Stereo, 24-Bit, 192 kHz, Multibit Sigma Delta DAC Data Sheet

DESIGN RESOURCES

- AD1853 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD1853 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

AD1853–SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltages (AV_{DD}, DV_{DD})	+5.0 V
Ambient Temperature	+25°C
Input Clock	24.576 MHz ($512 \times F_S$ Mode)
Input Signal	996.094 kHz
	−0.5 dB Full Scale
Input Sample Rate	48 kHz
Measurement Bandwidth	20 Hz to 20 kHz
Word Width	20 Bits
Input Voltage HI	3.5 V
Input Voltage LO	0.8 V

ANALOG PERFORMANCE (See Figures)

	Min	Typ	Max	Units
Resolution		24		Bits
Signal-to-Noise Ratio (20 Hz to 20 kHz)				
No Filter (Stereo)		114		dB
No Filter (Mono—See Figure 30)		117		dB
With A-Weighted Filter (Stereo)		117		dB
With A-Weighted Filter (Mono—See Figure 30)		120		dB
Dynamic Range (20 Hz to 20 kHz, −60 dB Input)				
No Filter (Stereo)	107.5	113		dB
No Filter (Mono—See Figure 30)		116		dB
With A-Weighted Filter (Stereo)	110	116		dB
With A-Weighted Filter (Mono—See Figure 30)		119		dB
Total Harmonic Distortion + Noise (Stereo)	−94	−104		dB
		0.00063		%
Total Harmonic Distortion + Noise (Mono—See Figure 30)		−107		dB
		0.00045		**%**
Analog Outputs				
Differential Output Range (±Full Scale w/1 mA into I_{REF})		3.0		mA p-p
Output Capacitance at Each Output Pin			30	pF
Out-of-Band Energy ($0.5 \times F_S$ to 75 kHz)			−90	dB
CMOUT		2.75		V
DC Accuracy				
Gain Error		±3.0		%
Interchannel Gain Mismatch	−0.15	0.01	+0.15	dB
Gain Drift		25		ppm/°C
Interchannel Crosstalk (EIAJ Method)		−125		dB
Interchannel Phase Deviation		±0.1		Degrees
Mute Attenuation		−100		dB
De-Emphasis Gain Error			±0.1	dB

NOTES
Single-ended current output range: 1 mA ± 0.75 mA.

Performance of right and left channels are identical (exclusive of the Interchannel Gain Mismatch and Interchannel Phase Deviation specifications).
Specifications subject to change without notice.

DIGITAL I/O (+25°C–AV_{DD}, DV_{DD} = +5.0 V ± 10%)

	Min	Typ	Max	Units
Input Voltage HI (V_{IH})	2.4			V
Input Voltage LO (V_{IL})			0.8	V
Input Leakage (I_{IH} @ V_{IH} = 3.5 V)			10	μA
Input Leakage (I_{IL} @ V_{IL} = 0.8 V)			10	μA
Input Capacitance			20	pF
Output Voltage HI (V_{OH})	DV_{DD}–0.5	DV_{DD}–0.4		V
Output Voltage LO (V_{OL})		0.2	0.5	V

Specifications subject to change without notice.

POWER

	Min	Typ	Max	Units
Supplies				
Voltage, Analog and Digital	4.5	5	5.5	V
Analog Current		12	15	mA
Digital Current		28	33	mA
Dissipation				
Operation—Both Supplies		200		mW
Operation—Analog Supply		60		mW
Operation—Digital Supply		140		mW
Power Supply Rejection Ratio				
1 kHz 300 mV p-p Signal at Analog Supply Pins		−77		dB
20 kHz 300 mV p-p Signal at Analog Supply Pins		−72		dB

Specifications subject to change without notice.

TEMPERATURE RANGE

	Min	Typ	Max	Units
Specifications Guaranteed		25		°C
Functionality Guaranteed	0		70	°C
Storage	−55		125	°C

Specifications subject to change without notice.

DIGITAL FILTER CHARACTERISTICS

Sample Rate (kHz)	Passband (kHz)	Stopband (kHz)	Stopband Attenuation (dB)	Passband Ripple (dB)
44.1	DC–20	24.1–328.7	110	±0.0002
48	DC–21.8	26.23–358.28	110	±0.0002
96	DC–39.95	56.9–327.65	115	±0.0005
192	DC–87.2	117–327.65	95	+0/−0.04 (DC–21.8 kHz)
				+0/−0.5 (DC–65.4 kHz)
				+0/−1.5 (DC–87.2 kHz)

Specifications subject to change without notice.

GROUP DELAY

Chip Mode	Group Delay Calculation	F_S	Group Delay	Units
INT8x Mode	$5553/(128 \times F_S)$	48 kHz	903.8	µs
INT4x Mode	$5601/(64 \times F_S)$	96 kHz	911.6	µs
INT2x Mode	$5659/(32 \times F_S)$	192 kHz	921	µs

Specifications subject to change without notice.

DIGITAL TIMING (Guaranteed Over 0°C to +70°C, $AV_{DD} = DV_{DD} = +5.0$ V ± 10%)

		Min	Units
t_{DMP}	MCLK Period (With $F_{MCLK} = 256 \times F_{LRCLK}$)★	54	ns
t_{DML}	MCLK LO Pulsewidth (All Modes)	$0.4 \times t_{DMP}$	ns
t_{DMH}	MCLK HI Pulsewidth (All Modes)	$0.4 \times t_{DMP}$	ns
t_{DBH}	BCLK HI Pulsewidth	20	ns
t_{DBL}	BCLK LO Pulsewidth	20	ns
t_{DBP}	BCLK Period	140	ns
t_{DLS}	LRCLK Setup	20	ns
t_{DLH}	LRCLK Hold (DSP Serial Port Mode Only)	5	ns
t_{DDS}	SDATA Setup	5	ns
t_{DDH}	SDATA Hold	10	ns
t_{PDRP}	PD/RST LO Pulsewidth	5	ns

*Higher MCLK frequencies are allowable when using the on-chip Master Clock Auto-Divide feature.

Specifications subject to change without notice.
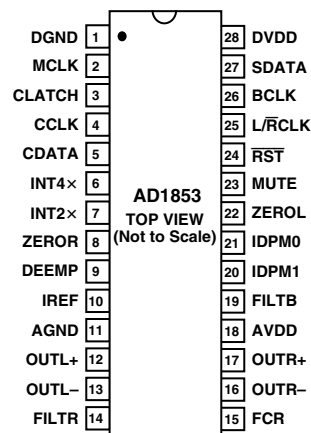
AD1853

ABSOLUTE MAXIMUM RATINGS*

	Min	Max	Units
DV_{DD} to DGND	−0.3	6	V
AV_{DD} to AGND	−0.3	6	V
Digital Inputs	DGND − 0.3	DV_{DD} + 0.3	V
Analog Outputs	AGND − 0.3	AV_{DD} + 0.3	V
AGND to DGND	−0.3	0.3	V
Reference Voltage		$(AV_{DD}$ + 0.3)/2	
Soldering		+300	°C
		10	sec

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE CHARACTERISTICS

	Min	Typ	Max	Units
θ_{JA} (Thermal Resistance [Junction-to-Ambient])		109		°C/W
θ_{JC} (Thermal Resistance [Junction-to-Case])		39		°C/W

PIN CONFIGURATION

AD1853
TOP VIEW
(Not to Scale)

Pin	Name		Pin	Name
1	DGND		28	DVDD
2	MCLK		27	SDATA
3	CLATCH		26	BCLK
4	CCLK		25	L/$\overline{R}$CLK
5	CDATA		24	$\overline{RST}$
6	INT4×		23	MUTE
7	INT2×		22	ZEROL
8	ZEROR		21	IDPM0
9	DEEMP		20	IDPM1
10	IREF		19	FILTB
11	AGND		18	AVDD
12	OUTL+		17	OUTR+
13	OUTL−		16	OUTR−
14	FILTR		15	FCR

ORDERING GUIDE

Model	Temperature	Package Description	Package Options
AD1853JRS	0°C to +70°C	28-Lead Shrink Small Outline	RS-28
AD1853JRSRL	0°C to +70°C	28-Lead Shrink Small Outline	RS-28 on 13" Reels

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PIN FUNCTION DESCRIPTIONS

| Pin	Input/Output	Pin Name	Description
1	I	DGND	Digital Ground.
2	I	MCLK	Master Clock Input. Connect to an external clock source. See Table II for allowable frequencies.
3	I	CLATCH	Latch input for control data. This input is rising-edge sensitive.
4	I	CCLK	Control clock input for control data. Control input data must be valid on the rising edge of CCLK. CCLK may be continuous or gated.
5	I	CDATA	Serial control input, MSB first, containing 16 bits of unsigned data. Used for specifying control information and channel-specific attenuation.
6	I	INT4×	Assert HI to select interpolation ratio of 4×, for use with double-speed inputs (88 kHz or 96 kHz). Assert LO to select 8× interpolation ratio.
7	I	INT2×	Assert HI to select interpolation ratio of 2×, for quad-speed inputs (176 kHz or 192 kHz). Assert LO to select 8× interpolation ratio.
8	O	ZEROR	Right Channel Zero Flag Output. This pin goes HI when Right Channel has no signal input for more than 1024 LR Clock Cycles.
9	I	DEEMP	De-Emphasis. Digital de-emphasis is enabled when this input signal is HI. This is used to impose a 50 μs/15 μs response characteristic on the output audio spectrum at an assumed 44.1 kHz sample rate. Curves for 32 kHz and 48 kHz sample rates may be selected via SPI control register.
10	I	IREF	Connection point for external bias resistor. Voltage held at V_{REF}.
11	I	AGND	Analog Ground.
12	O	OUTL+	Left Channel Positive line level analog output.
13	O	OUTL–	Left Channel Negative line level analog output.
14	O	FILTR	Voltage Reference Filter Capacitor Connection. Bypass and decouple the voltage reference with parallel 10 μF and 0.1 μF capacitors to the AGND (Pin 11).
15	I	FCR	Filter cap return pin for cap connected to FILTB (Pin 19).
16	O	OUTR–	Right Channel Negative line level analog output.
17	O	OUTR+	Right Channel Positive line level analog output.
18	I	AVDD	Analog Power Supply. Connect to analog +5 V supply.
19	O	FILTB	Filter Capacitor connection, connect 10 μF capacitor to FCR (Pin 15).
20	I	IDPM1	Input serial data port mode control one. With IDPM0, defines one of four serial modes.
21	I	IDPM0	Input serial data port mode control zero. With IDPM1, defines one of four serial modes.
22	O	ZEROL	Left Channel Zero Flag output. This pin goes HI when Left Channel has no signal input for more than 1024 LR Clock Cycles.
23	I	MUTE	Mute. Assert HI to mute both stereo analog outputs. Deassert LO for normal operation.
24	I	$\overline{RST}$	$\overline{Reset}$. The AD1853 is placed in a reset state when this pin is held LO. The AD1853 is reset on the rising edge of this signal. The serial control port registers are reset to the default values. Connect HI for normal operation.
25	I	L/$\overline{R}$CLK	Left/$\overline{Right}$ clock input for input data. Must run continuously.
26	I	BCLK	Bit clock input for input data.
27	I	SDATA	Serial input, MSB first, containing two channels of 16/18/20/24 bit twos-complement data.
28	I	DVDD	Digital Power Supply Connect to digital +5 V supply.
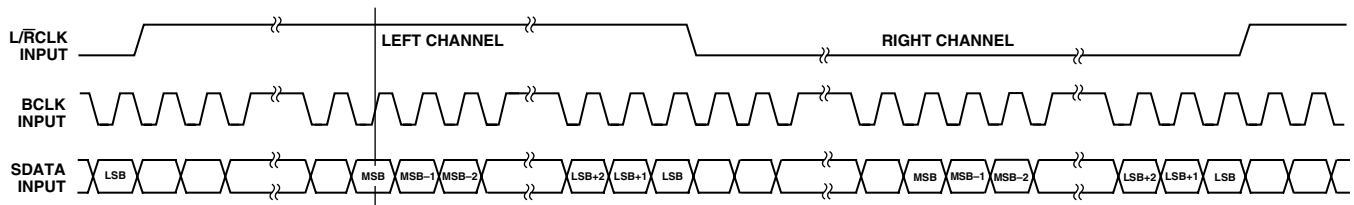
AD1853
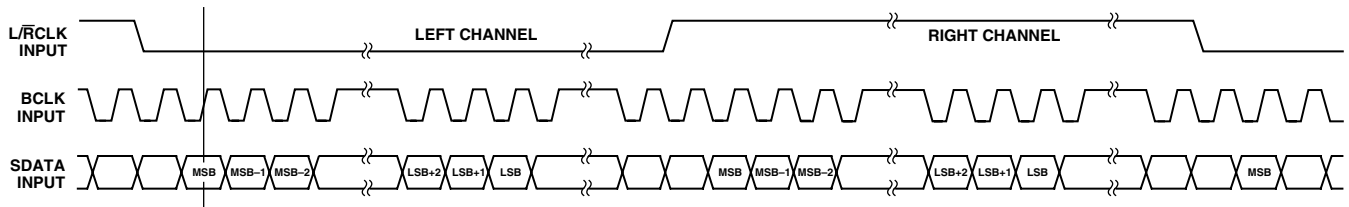

Figure 1. Right-Justified Mode
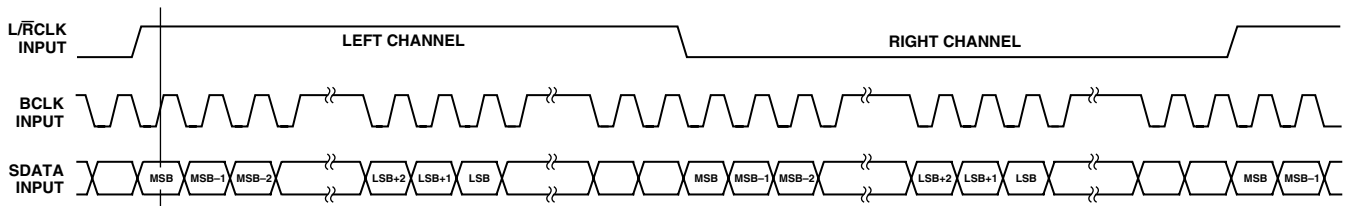

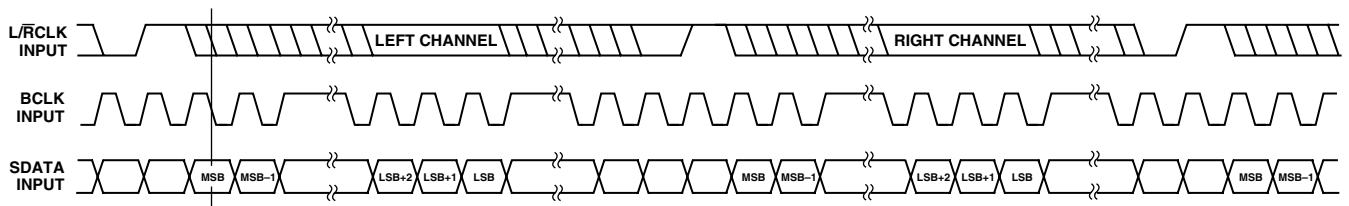*Figure 2. I²S-Justified Mode*

Figure 3. Left-Justified Mode
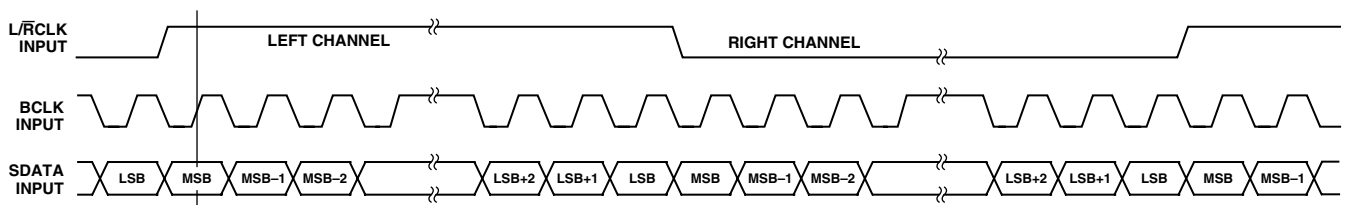

Figure 4. Left-Justified DSP Mode

Figure 5. 32 × F$_S$ Packed Mode

REV. A

OPERATING FEATURES

Serial Data Input Port

The AD1853's flexible serial data input port accepts data in twos-complement, MSB-first format. The left channel data field always precedes the right channel data field. The serial mode is set by using either the external mode pins (IDPM0 Pin 21 and IDPM1 Pin 20) or the mode select bits (Bits 4 and 5) in the SPI control register. To control the serial mode using the external mode pins, the SPI mode select bits should be set to zero (default at power-up). To control the serial mode using the SPI mode select bits, the external mode control pins should be grounded.

In all modes except for the right-justified mode, the serial port will accept an arbitrary number of bits up to a limit of 24 (extra bits will not cause an error, but they will be truncated internally). In the right-justified mode, control register Bits 8 and 9 are used to set the word length to 16, 20, or 24 bits. The default on power-up is 24-bit mode. When the SPI Control Port is not being used, the SPI pins (3, 4 and 5) should be tied LO.

Serial Data Input Mode

The AD1853 uses two multiplexed input pins to control the mode configuration of the input data port mode.

Table I. Serial Data Input Modes

IDPM1 (Pin 20)	IDPM0 (Pin 21)	Serial Data Input Format
0	0	Right Justified (24 Bits) Default
0	1	I^{2}S-Compatible
1	0	Left Justified
1	1	DSP

Figure 1 shows the right-justified mode. LRCLK is HI for the left channel, LO for the right channel. Data is valid on the rising edge of BCLK.

In normal operation, there are 64-bit clocks per frame (or 32 per half-frame). When the SPI word length control bits (Bits 8 and 9 in the control register) are set to 24 bits (0:0), the serial port will begin to accept data starting at the 8th bit clock pulse after the L/$\overline{R}$CLK transition. When the word length control bits are set to 20-bit mode, data is accepted starting at the 12th bit clock position. In 16-bit mode, data is accepted starting at the 16th-bit clock position. These delays are independent of the number of bit clocks per frame, and therefore other data formats are possible using the delay values described above. For detailed timing, see Figure 6.

Figure 2 shows the I^{2}S mode. L/$\overline{R}$CLK is LO for the left channel, and HI for the right channel. Data is valid on the rising edge of BCLK. The MSB is left-justified to an L/$\overline{R}$CLK transition but with a single BCLK period delay. The I^{2}S mode can be used to accept any number of bits up to 24.

Figure 3 shows the left-justified mode. L/$\overline{R}$CLK is HI for the left channel, and LO for the right channel. Data is valid on the rising edge of BCLK. The MSB is left-justified to an L/$\overline{R}$CLK transition, with no MSB delay. The left-justified mode can accept any word length up to 24 bits.

Figure 4 shows the DSP serial port mode. L/$\overline{R}$CLK must pulse HI for at least one bit clock period before the MSB of the left channel is valid, and L/$\overline{R}$CLK must pulse HI again for at least one bit clock period before the MSB of the right channel is valid. Data is valid on the falling edge of BCLK. The DSP serial port mode can be used with any word length up to 24 bits.
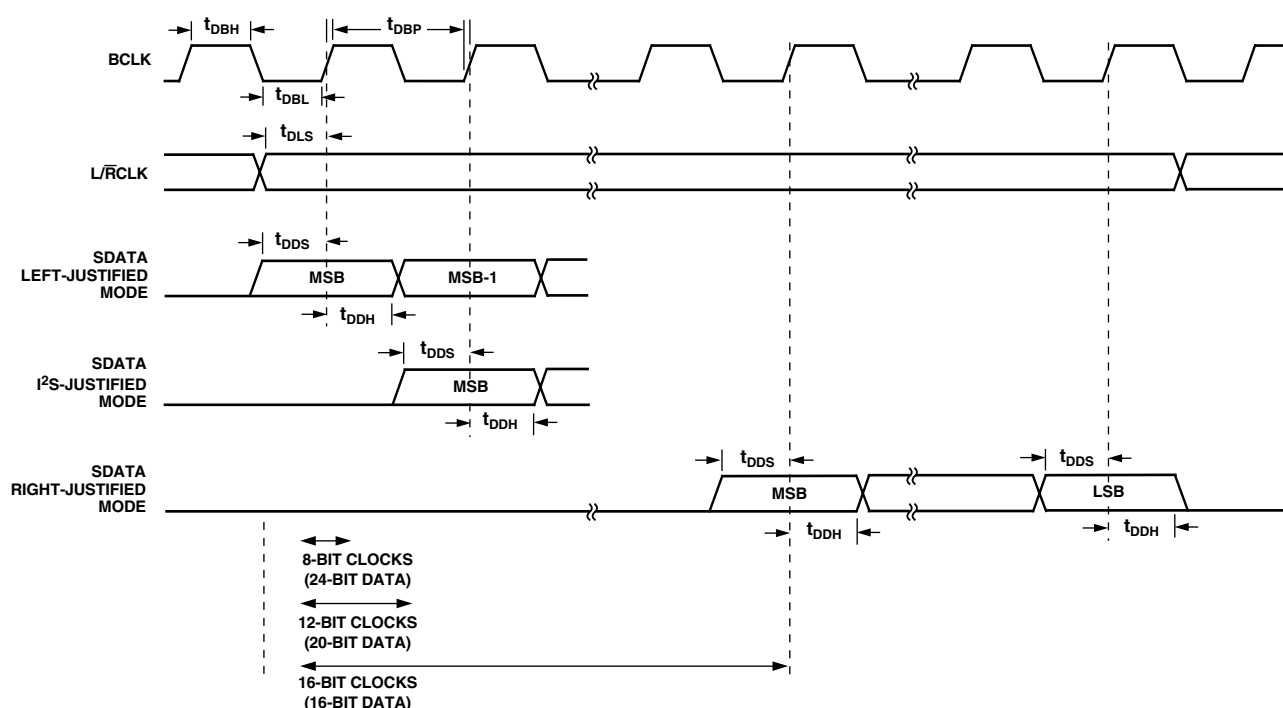

Figure 6. Serial Data Port Timing

AD1853

Table II.

Chip Mode	Allowable Master Clock Frequencies	Nominal Input Sample Rate	Internal Sigma-Delta Clock Rate
INT8× Mode	$256 \times F_S$, $384 \times F_S$, $512 \times F_S$, $768 \times F_S$, $1024 \times F_S$	48 kHz	$128 \times F_S$
INT4× Mode	$128 \times F_S$, $192 \times F_S$, $256 \times F_S$, $384 \times F_S$, $512 \times F_S$	96 kHz	$64 \times F_S$
INT2× Mode	$64 \times F_S$, $96 \times F_S$, $128 \times F_S$, $192 \times F_S$, $256 \times F_S$	192 kHz	$32 \times F_S$

In this mode, it is the responsibility of the DSP to ensure that the left data is transmitted with the first LRCLK pulse, and that synchronism is maintained from that point forward.

Note that the AD1853 is capable of a $32 \times F_S$ BCLK frequency "packed mode" where the MSB is left-justified to an L/$\overline{R}$CLK transition, and the LSB is right-justified to the opposite L/$\overline{R}$CLK transition. L/$\overline{R}$CLK is HI for the left channel, and LO for the right channel. Data is valid on the rising edge of BCLK. Packed mode can be used when the AD1853 is programmed in right-justified or left-justified mode. Packed mode is shown is Figure 5.

Master Clock Auto-Divide Feature
The AD1853 has a circuit that autodetects the relationship between master clock and the incoming serial data, and internally sets the correct divide ratio to run the interpolator and modulator. The allowable frequencies for each mode are shown above.

Serial Control Port
The AD1853 serial control port is SPI-compatible. SPI (Serial Peripheral Interface) is an industry standard serial port protocol. The write-only serial control port gives the user access to: select input mode, soft reset, soft de-emphasis, channel specific attenuation and mute (both channels at once). The SPI port is a 3-wire interface with serial data (CDATA), serial bit clock (CCLK), and data latch (CLATCH). The data is clocked into an internal shift register on the rising edge of CCLK. The serial data should change on the falling edge of CCLK and be stable on the rising edge of CCLK. The rising edge of

CLATCH is used internally to latch the parallel data from the serial-to-parallel converter. This rising edge should be aligned with the falling edge of the last CCLK pulse in the 16-bit frame. The CCLK can run continuously between transactions.

The serial control data is 16-bit MSB first, and is unsigned. Bits 0 and 1 are used to select 1 of 3 registers (control, volume left, and volume right). The remaining 14 bits (bits 15:2) are used to carry the data for the selected register. If a volume register is selected, then the upper 14 bits are used to multiply the digital input signal by the control word, which is interpreted as an unsigned number (for example, 11111111111111 is 0 dB, and 01111111111111 is –6 dB, etc.). The default volume control words on power-up are all 1s (0 dB). The control register only uses bits 11:2 to carry data; the upper bits (15:12) should always be written with zeroes, as several test modes are decoded from these upper bits. The control register defaults on power-up to 8× interpolation mode, 24-bit right-justified serial mode, unmuted, and no de-emphasis filter. The intent with these reset defaults is to enable AD1853 applications without requiring the use of the serial control port. For those users that do not use the serial control port, it is still possible to mute the AD1853 output by using the MUTE pin (Pin 23) signal.

Note that the serial control port timing is asynchronous to the serial data port timing. Changes made to the attenuator level will be updated on the next edge of the LRCLK after CLATCH write pulse as shown in Figure 6.
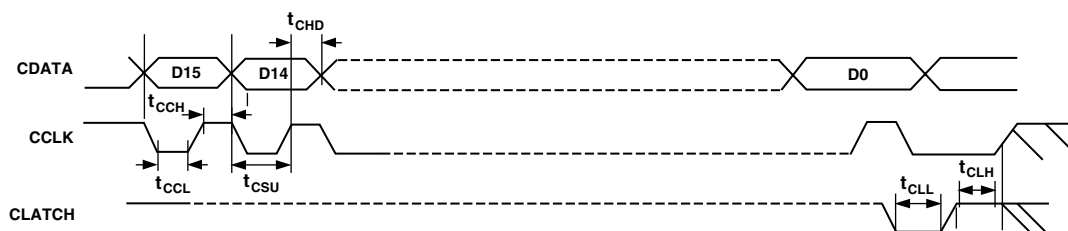

Figure 7. Serial Control Port Timing

Table III. Digital Timing

		Min	Units
t_{CCH}	CCLK HI Pulsewidth	40	ns
t_{CCL}	CCLK LOW Pulsewidth	40	ns
t_{CSU}	CDATA Setup Time	10	ns
t_{CHD}	CDATA Hold Time	10	ns
t_{CLL}	CLATCH LOW Pulsewidth	10	ns
t_{CLH}	CLATCH HI Pulsewidth	10	ns

SPI REGISTER DEFINITIONS

The SPI port allows flexible control of many chip parameters. It is organized around three registers; a LEFT-CHANNEL VOLUME register, a RIGHT-CHANNEL VOLUME register and a CONTROL register. Each WRITE operation to the AD1853 SPI control port requires 16 bits of serial data in MSB-first format. The bottom two bits are used to select one of three registers, and the top 14 bits are then written to that register. This allows a write to one of the three registers in a single 16-bit transaction.

The SPI CCLK signal is used to clock in the data. The incoming data should change on the falling edge of this signal. At the end of the 16 CCLK periods, the CLATCH signal should rise to latch the data internally into the AD1853.

Register Addresses

The lowest two bits of the 16-bit input word are decoded as follows to set the register into which the upper 14 bits will be written.

Bit 1	Bit 0	Register
0	0	Volume Left
1	0	Volume Right
0	1	Control Register

VOLUME LEFT and VOLUME RIGHT Registers

A write operation to the left or right volume registers will activate the "auto-ramp" clickless volume control feature of the AD1853. This feature works as follows. The upper 10 bits of the volume control word will be incremented or decremented by 1 at a rate equal to the input sample rate. The bottom 4 bits are not fed into the auto-ramp circuit and thus take effect immediately. This arrangement gives a worst-case ramp time of about $1024/F_S$ for step changes of more than 60 dB, which has been determined by listening tests to be optimal in terms of preventing the perception of a "click" sound on large volume changes. See Figure 8 for a graphical description of how the volume changes as a function of time.

The 14-bit volume control word is used to multiply the signal, and therefore the control characteristic is linear, not dB. A constant dB/step characteristic can be obtained by using a lookup table in the microprocessor that is writing to the SPI port.
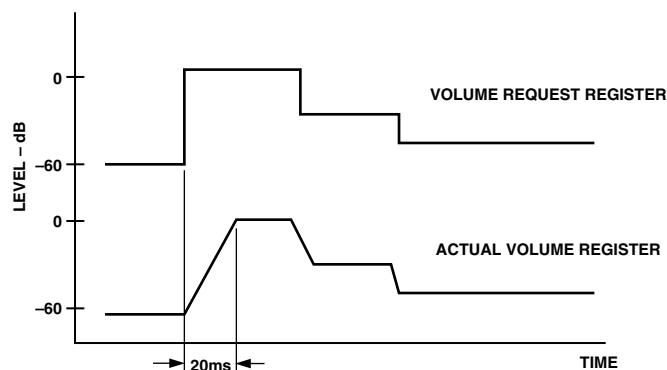
Figure 8. Smooth Volume Control

AD1853

Control Register

The following table shows the functions of the control register. The control register is addressed by having a "01" in the bottom 2 bits of the 16-bit SPI word. The top 14 bits are then used for the control register.

Bit 11	Bit 10	Bit 9:8	Bit 7	Bit 6	Bit 5:4	Bit 3:2
INT2× Mode OR'd with Pin. Default = 0	INT4× Mode OR'd with Pin. Default = 0	Number of Bits in Right-Justified Serial Mode. 0:0 = 24 0:1 = 20 1:0 = 16 Default = 0:0	Soft Reset. Default = 0	Soft Mute OR'd with Pin. Default = 0	Serial Mode OR'd with Mode Pins. IDPMI:IDPM0 0:0 Right-Justified 0:1 I²S 1:0 Left-Justified 1:1 DSP Mode Default = 0:0	De-Emphasis Filter Select. 0:0 No Filter 0:1 44.1 kHz Filter 1:0 32 kHz Filter 1:1 48 kHz Filter Default = 0.0

Mute

The AD1853 offers two methods of muting the analog output. By asserting the MUTE (Pin 23) signal HI, both the left and right channel are muted. As an alternative, the user can assert the mute bit in the serial control register (Bit 6) HI. The AD1853 has been designed to minimize pops and clicks when muting and unmuting the device by automatically "ramping" the gain up or down. When the device is unmuted, the volume returns to the value set in the volume register.

Analog Attenuation

The AD1853 also offers the choice of using IREF (Pin 10) to attenuate by up to 50 dB in the analog domain. This feature can be used as an analog volume control. It is also a convenient place to add a compressor/limiter gain control signal.

Output Drive, Buffering and Loading

The AD1853 analog output stage is able to drive a 1 kΩ (in series with 2 nF) load. The analog outputs are usually ac coupled with a 10 µF capacitor.

De-Emphasis

The AD1853 has a built-in de-emphasis filter that can be used to decode CDs that have been encoded with the standard "Redbook" 50 µs/15 µs emphasis response curve. Three curves are available; one each for 32 kHz, 44.1 kHz and 48 kHz sampling rates. The external "DEEMP" pin (Pin 9) turns on the 44.1 kHz de-emphasis filter. The other filters may be selected by writing to control Bits 2 and 3 in the control register. If the SPI port is used to control the de-emphasis filter, the external DEEMP pin should be tied LO.

Control Signals

The IDPM0 and IDPM1 control inputs are normally connected HI or LO to establish the operating state of the AD1853. They can be changed dynamically (and asynchronously to LRCLK and the master clock), but it is possible that a click or pop sound may result during the transition from one serial mode to another. If possible, the AD1853 should be placed in mute before such a change is made.

Figures 9–14 show the calculated frequency response of the digital interpolation filters. Figures 15–27 show the performance of the AD1853 as measured by an Audio Precision System 2 Cascade. For the wideband plots, the noise floor shown in the plots is higher than the actual noise floor of the AD1853. This is caused by the higher noise floor of the "High Bandwidth" ADC used in the Audio Precision measurement system. The two-tone test shown in Figure 18 is per the SMPTE standard for measuring Intermodulation Distortion.
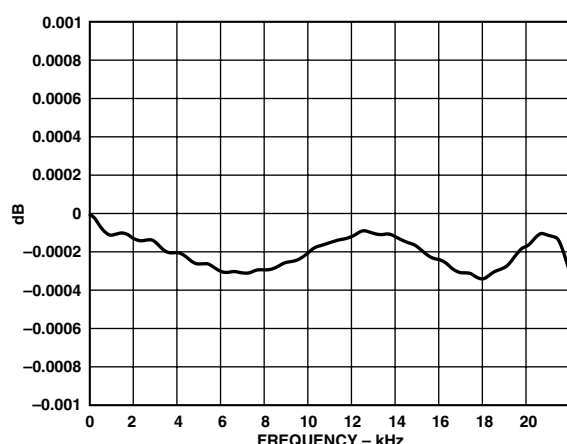

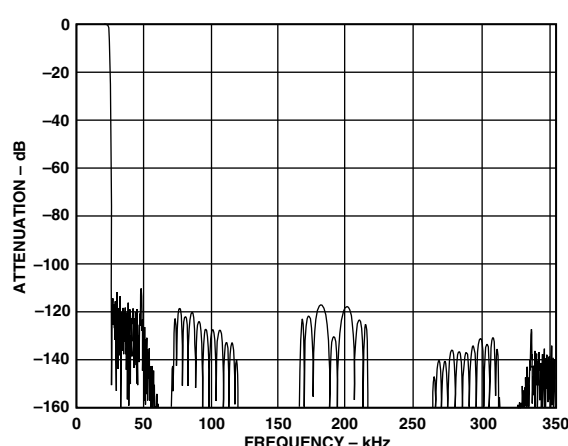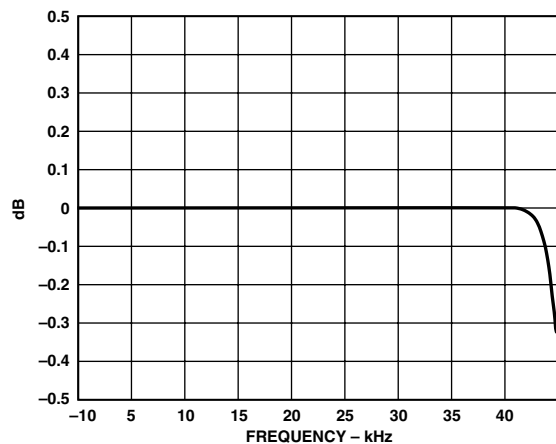Figure 9. Passband Response 8× Mode, 48 kHz Sample Rate
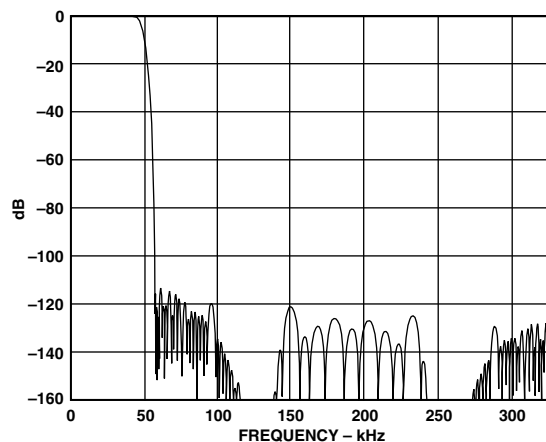

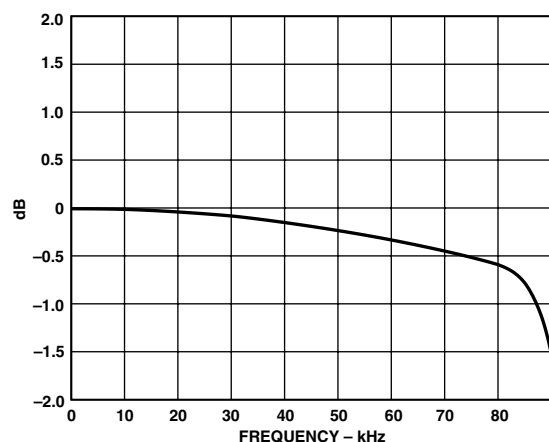Figure 10. Complete Response, 8× Mode, 48 kHz Sample Rate

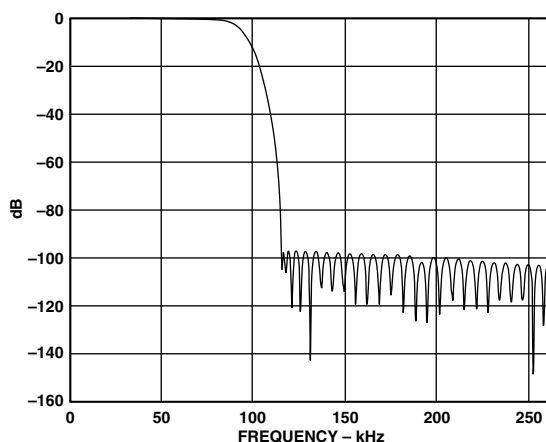Figure 11. 44 kHz Passband Response 4× Mode, 96 kHz Sample Rate

Figure 12. 88 kHz Passband Response 2× Mode, 192 kHz Sample Rate

Figure 13. THD vs. Frequency Input @ –3 dBFS, SR 48 kHz

Figure 14. Complete Response, 4× Mode, 96 kHz Sample Rate

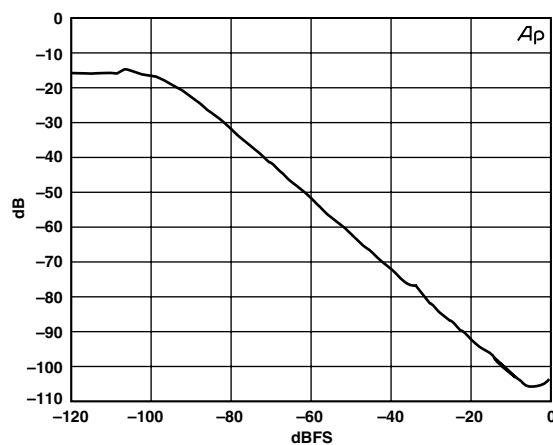Figure 15. Complete Response, 2× Mode, 192 kHz Sample Rate

Figure 16. THD + N Ratio vs. Amplitude Input 1 kHz, SR 48 kHz, 24-Bit

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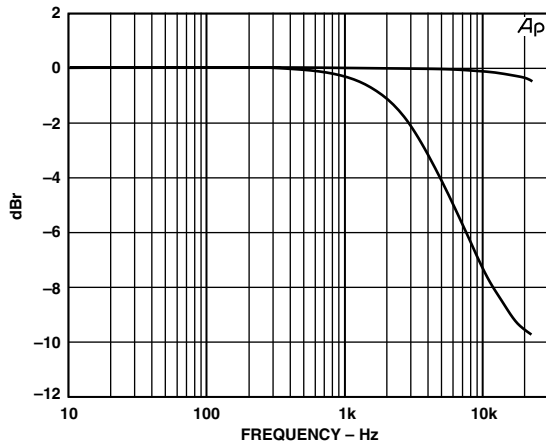
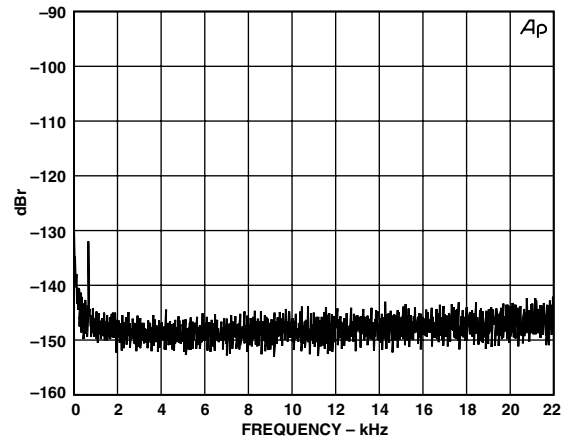Figure 17. Normal De-Emphasis Frequency Response Input @ –10 dBFS, SR 48 kHz

Figure 20. Noise Floor for Zero Input, SR 48 kHz, SNR –117 dBFS A-Weighted
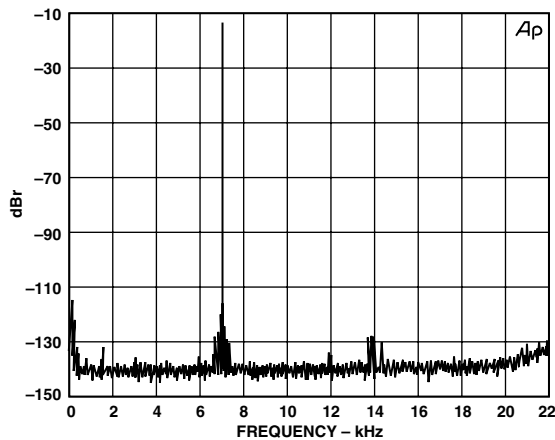
Figure 18. SMPTE/DIN 4:1 IMD 60 Hz/7 kHz @ 0 dBFS
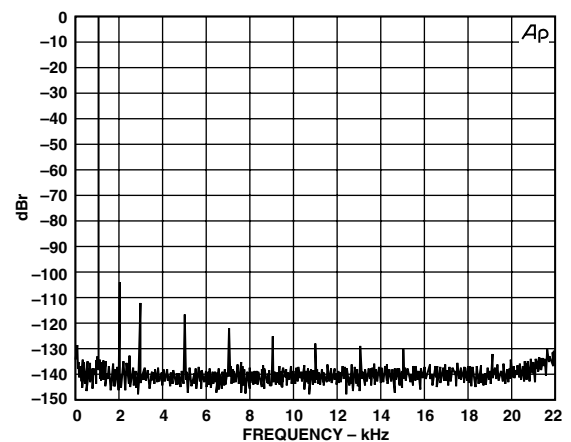
Figure 21. Input 0 dBFS @ 1 kHz, BW 10 Hz to 22 kHz, SR 48 kHz, THD+N 104 dBFS
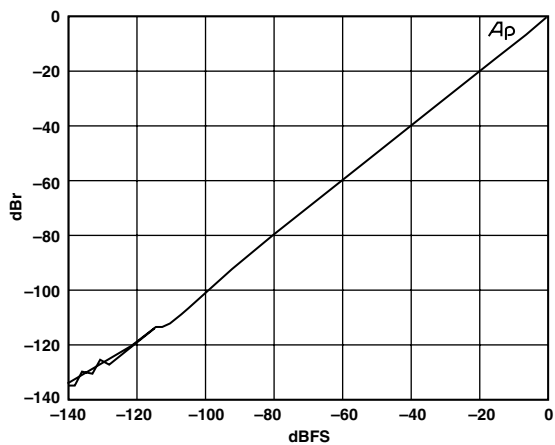
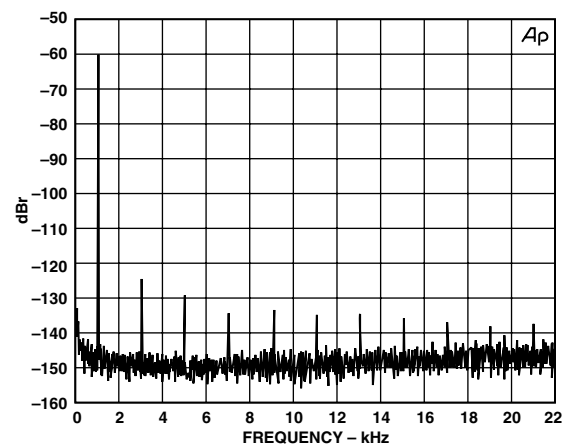Figure 19. Linearity vs. Amplitude Input 200 Hz, SR 48 kHz, 24-Bit Word

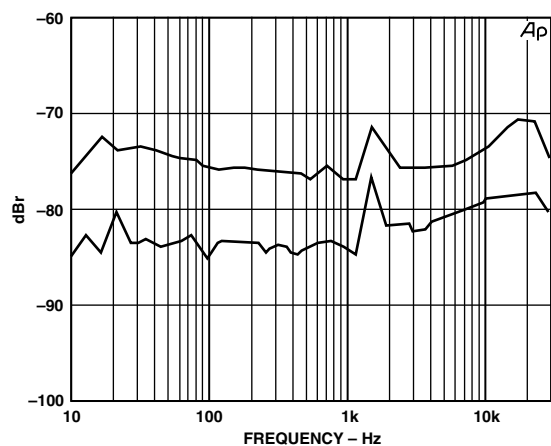Figure 22. Dynamic Range for 1 kHz @ –60 dBFS, 116 dB, Triangular Dithered Input

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Figure 23. Power Supply Rejection vs. Frequency
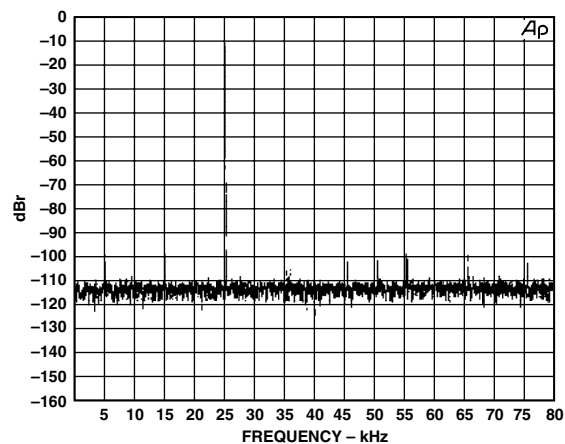AV_{DD} 5 V dc + 100 mV p-p ac

Figure 26. Wideband Plot, 25 kHz Input, 2× Interpolation,
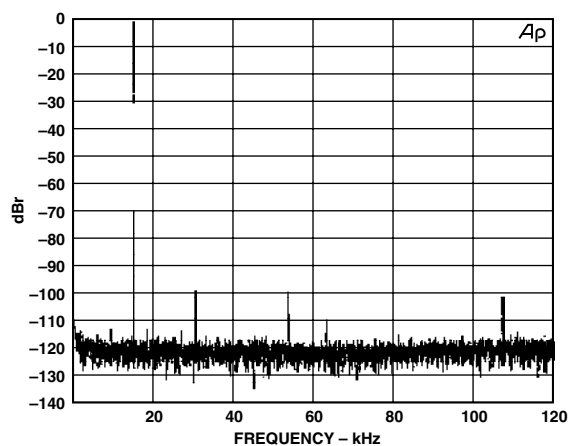SR 192 kHz

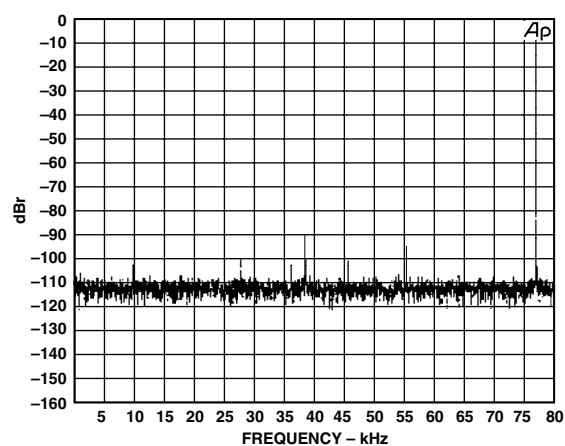Figure 24. Wideband Plot, 15 kHz Input, 8× Interpolation,
SR 48 kHz

Figure 27. Wideband Plot, 75 kHz Input, 2× Interpolation,
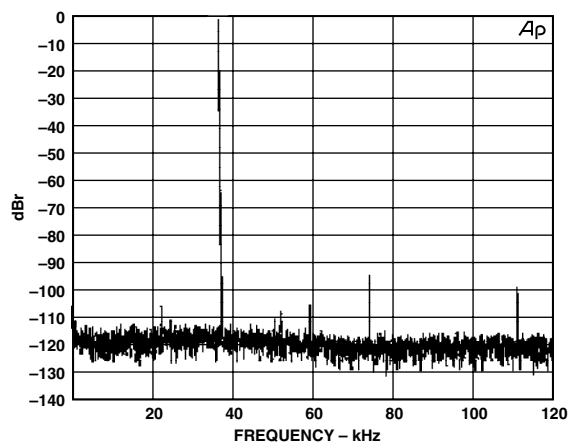SR 192 kHz

Figure 25. Wideband Plot, 37 kHz Input, 4× Interpolation,
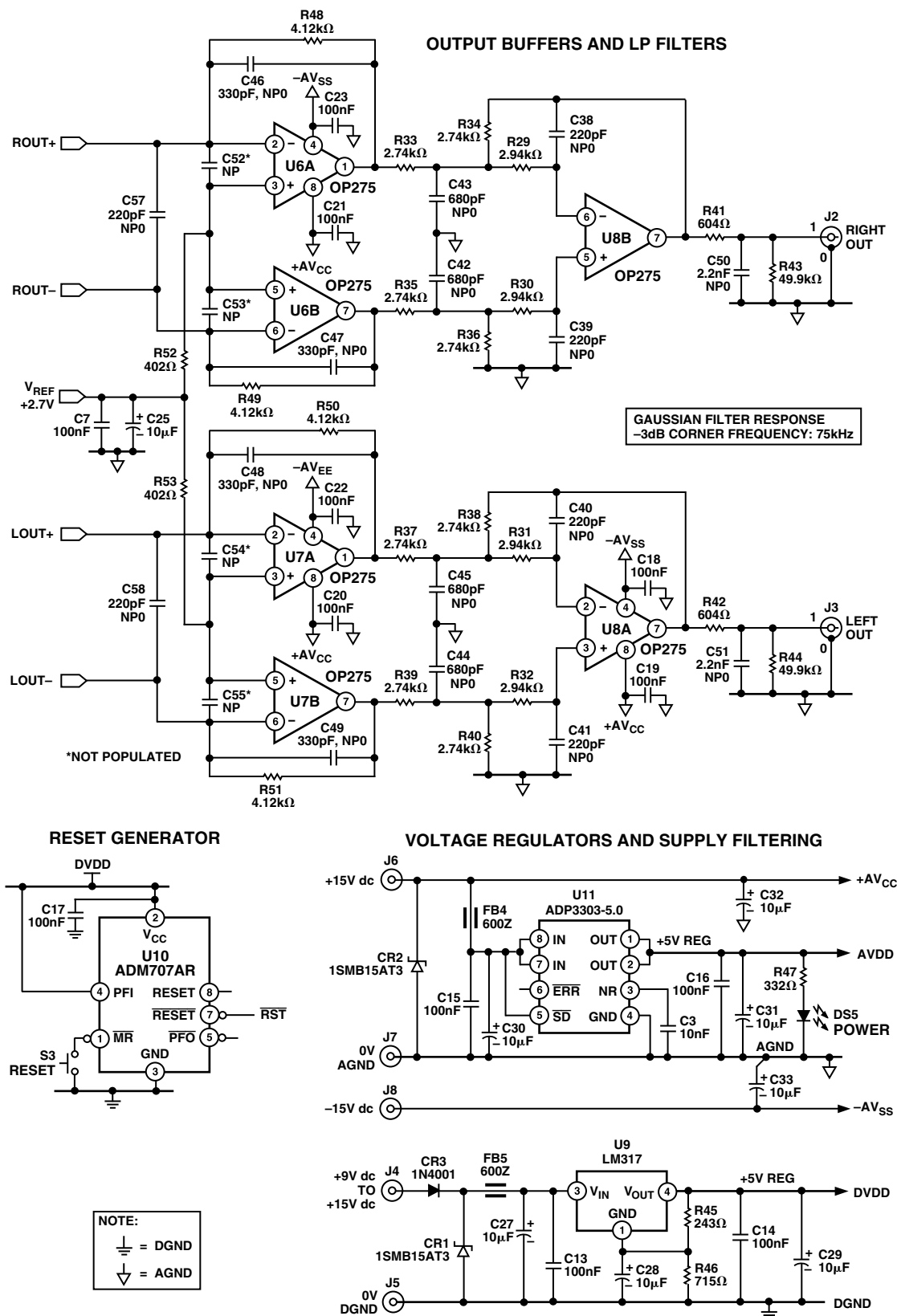SR 96 kHz

AD1853

STEREO MODE OUTPUT FILTER

Figure 28. Digital Receiver, MUX and AD1853 DAC

REV. A

OUTPUT BUFFERS AND LP FILTERS

GAUSSIAN FILTER RESPONSE
–3dB CORNER FREQUENCY: 75kHz

*NOT POPULATED

RESET GENERATOR

VOLTAGE REGULATORS AND SUPPLY FILTERING

NOTE:
⏚ = DGND
▽ = AGND

Figure 29. DAC Output LP Filter, Power and Reset

AD1853

I/V CONVERTERS AND LP FILTER
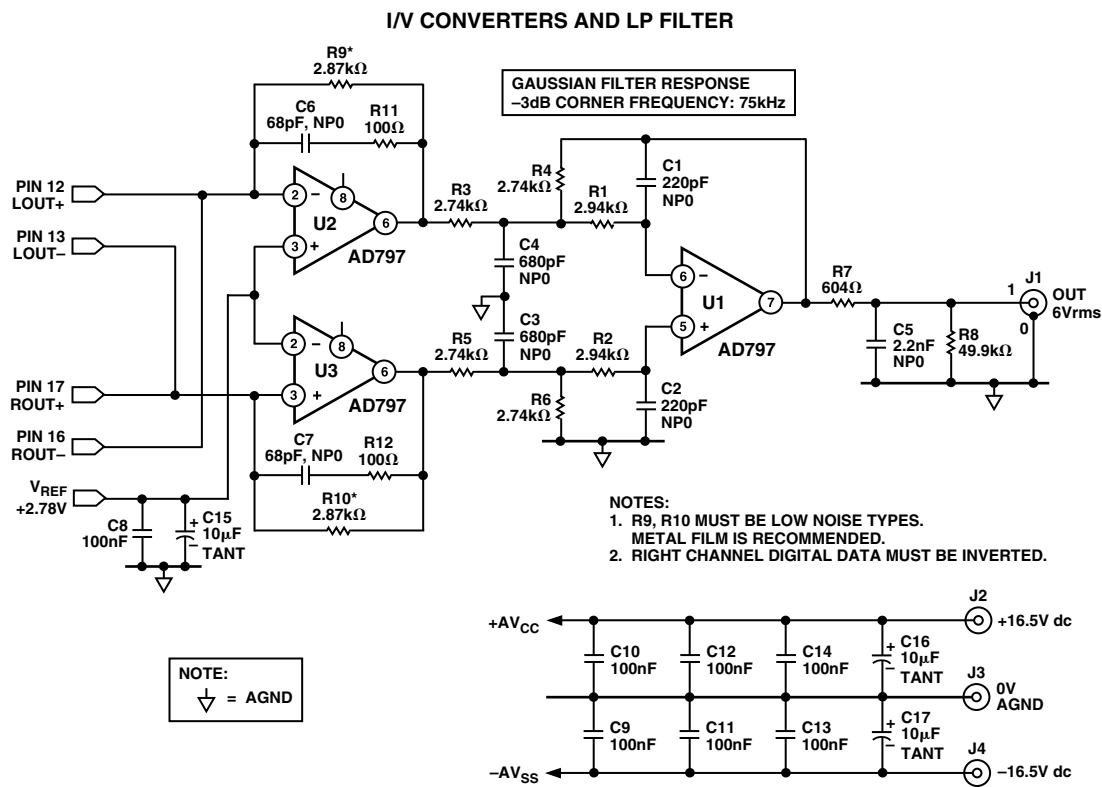
Figure 30. Mono Application Circuit

NOTES:
1. R9, R10 MUST BE LOW NOISE TYPES. METAL FILM IS RECOMMENDED.
2. RIGHT CHANNEL DIGITAL DATA MUST BE INVERTED.

NOTE:
▽ = AGND

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Shrink Small Outline Package (SSOP)
(RS-28)

REV. A