

FSFR-HS Series — Advanced Fairchild Power Switch (FPS™) for Half-Bridge Resonant Converters

Features

- Variable Frequency Control with 50% Duty Cycle for Half-Bridge Resonant Converter Topology
- High Efficiency through Zero Voltage Switching (ZVS)
- Built-in High-Side Gate Driver IC
- Internal UniFET™s with Fast-Recovery Type Body Diode (t_{rr} =160 ns Typical)
- Fixed Dead Time (350 ns) Optimized for MOSFETs
- Operating Frequency Up to 600 kHz for Soft-Start
- Self Auto-Restart Operation for All Protections, Despite External LV_{CC} Bias
- Line UVLO with Programmable Hysteresis Level
- Simple On/Off with Line UVLO Pin
- Easy Configuration and Compatibility with FAN7930 for Line UVLO without External Components
- Protection Functions: Over-Voltage Protection (OVP), Over-Current Protection (OCP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD)

Applications

- PDP and LCD TVs
- Desktop PCs and Servers
- Adapters
- Telecom Power Supplies

Description

The FSFR-HS is a highly integrated power switch designed for high-efficiency half-bridge resonant converters. Offering everything necessary to build a reliable and robust resonant converter, the FSFR-HS simplifies designs while improving productivity and performance. The FSFR-HS combines power MOSFETs, a high-side gate-drive circuit, an accurate current-controlled oscillator, and built-in protection functions.

The high-side gate-drive circuit has a common-mode noise cancellation capability, which provides stable operation with excellent noise immunity. Using zero-voltage-switching (ZVS) technique dramatically reduces the switching losses and significantly improves efficiency. The ZVS also reduces the switching noise noticeably, even though the operating frequency increases. It allows a small Electromagnetic Interference (EMI) filter, besides the high operating frequency, to reduce the volume of the resonant tank and to increase power density.

The FSFR-HS can be applied to resonant converter topologies such as series resonant, parallel resonant, and LLC resonant converters.

Related Resources

[AN4151 — Half-Bridge LLC Resonant Converter Design Using FSFR-Series Fairchild Power Switch \(FPS™\)](#)

Ordering Information

Part Number	Package	Operating Junction Temperature	$R_{DS(ON_MAX)}$	Maximum Output Power without Heatsink ($V_{IN}=350\sim400\text{ V}$) ^(1,2)	Maximum Output Power with Heatsink ($V_{IN}=350\sim400\text{ V}$) ^(1,2)
FSFR1800HS	9-SIP	-40 to +130°C	0.95 Ω	120 W	260 W
FSFR1800HSL	9-SIP L-Forming				
FSFR1700HS	9-SIP	-40 to +130°C	1.25 Ω	100 W	200 W
FSFR1700HSL	9-SIP L-Forming				

Notes:

1. The junction temperature can limit the maximum output power.
2. Maximum practical continuous power in an open-frame design at 50°C ambient.

Application Circuit Diagram

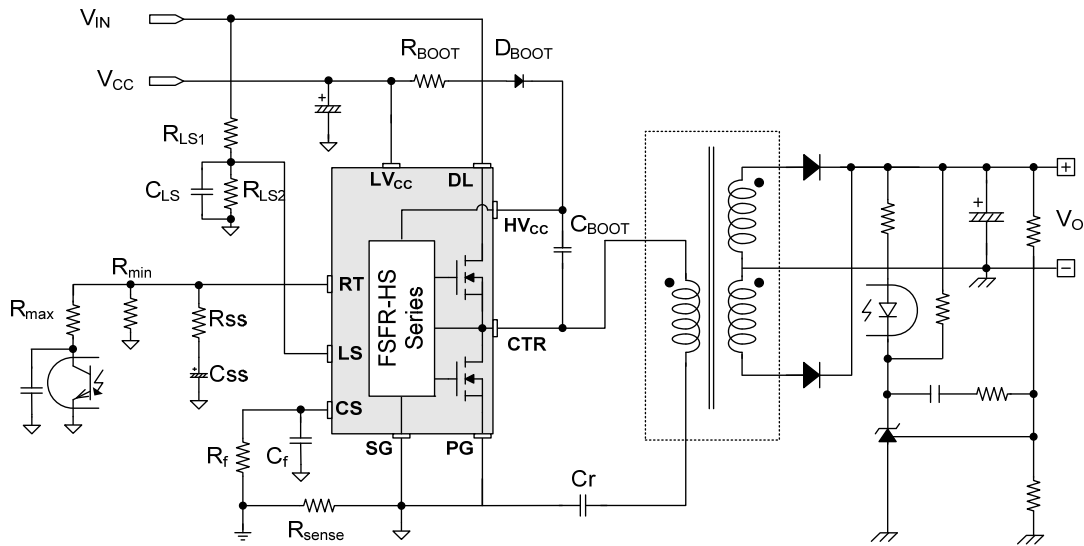


Figure 1. Typical Application Circuit (LLC Resonant Half-Bridge Converter)

Block Diagram

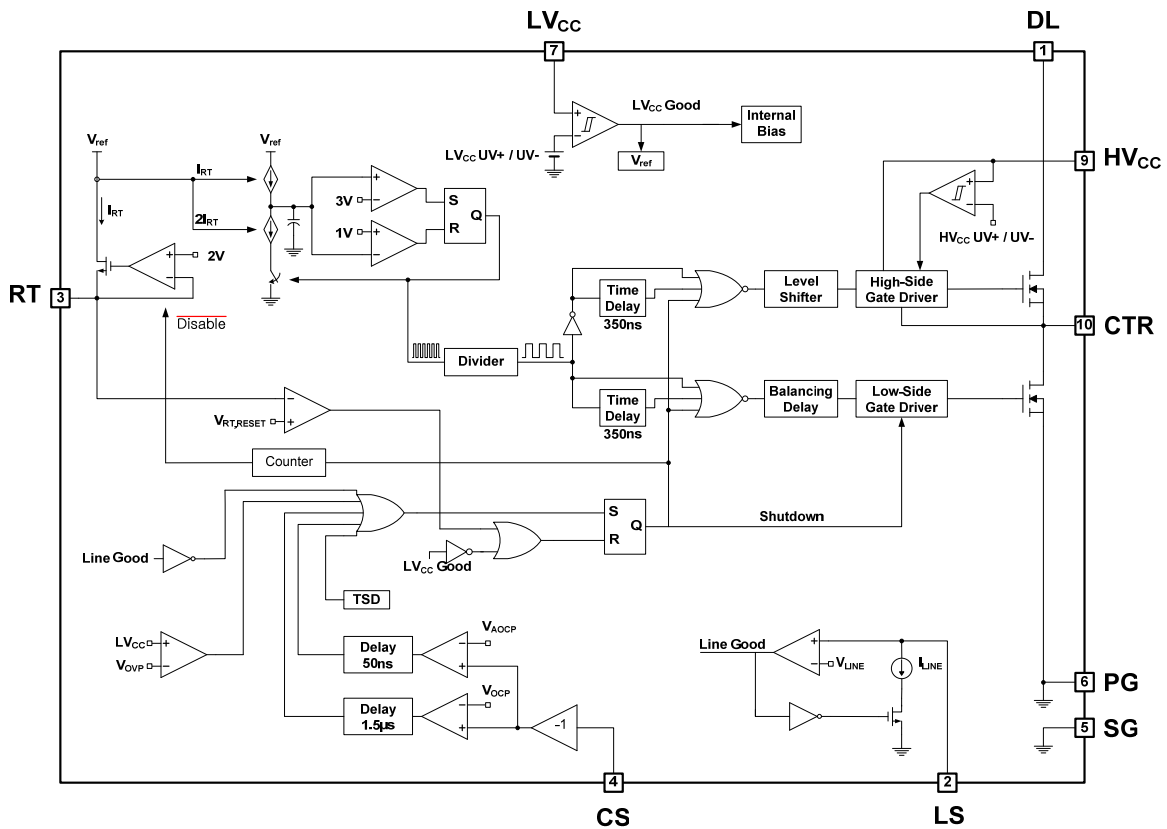


Figure 2. Internal Block Diagram

Pin Configuration

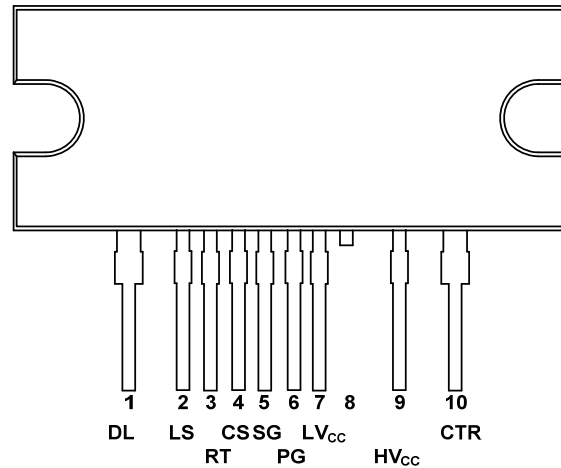


Figure 3. Package Diagram

Pin Definitions

Pin #	Name	Description
1	DL	This is the drain of the high-side MOSFET, typically connected to the input DC link voltage.
2	LS	This is the line-sensing pin for the input voltage Under-Voltage Lockout (UVLO).
3	RT	This pin is used for controlling the switching frequency in normal operation. When any protections are triggered, the internal Auto/Restart (A/R) circuit starts to sense the voltage on the pin, which is discharged naturally by external resistance. The IC can be operated with A/R when the voltage decreases 0.1 V. Typically, an opto-coupler is connected to control the switching frequency for the output voltage regulation and resistors for setting minimum / maximum operating frequency.
4	CS	This pin senses the current flowing through the low-side MOSFET. Typically, negative voltage is applied to this pin.
5	SG	This pin is the ground of the control part.
6	PG	This pin is the power ground. This pin is connected to the source of the low-side MOSFET.
7	LV _{CC}	This pin is the supply voltage of the control IC.
8	NC	No connection
9	HV _{CC}	This is the supply voltage of the high-side gate-drive circuit.
10	CTR	This is the drain of the low-side MOSFET. Typically, a transformer is connected to this pin.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V _{DS}	Maximum Drain-to-Source Voltage (DL-CTR and CTR-PG)		500		V
LV _{CC}	Low-Side Supply Voltage		-0.3	25.0	V
HV _{CC} to CTR	High-Side V _{CC} Pin to Low-Side Drain Voltage		-0.3	25.0	V
HV _{CC}	High-Side Floating Supply Voltage		-0.3	525.0	V
V _{RT}	Timing Resistor Connecting and Auto-Restart Pin Voltage		-0.3	5.0	V
V _{LS}	Line Sensing Input Voltage		-0.3	LV _{CC}	V
V _{CS}	Current Sense (CS) Pin Input Voltage		-5	1	V
f _{sw}	Recommended Switching Frequency		10	600	kHz
dV _{CTR} /dt	Allowable Low-Side MOSFET Drain Voltage Slew Rate			50	V/ns
P _D	Total Power Dissipation ⁽⁴⁾	FSFR1800HS/L		11.7	W
		FSFR1700HS/L		11.6	
T _J	Maximum Junction Temperature ⁽⁵⁾			+150	°C
	Recommended Operating Junction Temperature ⁽⁵⁾		-40	+130	
T _{STG}	Storage Temperature Range		-55	+150	°C
MOSFET Section					
V _{DGR}	Drain Gate Voltage (R _{GS} =1 MΩ)		500		V
V _{GS}	Gate Source (GND) Voltage			±30	V
I _{DM}	Drain Current Pulsed ⁽⁶⁾	FSFR1800HS/L		23	A
		FSFR1700HS/L		20	
I _D	Continuous Drain Current	FSFR1800HS/L	T _C =25°C	7.0	A
			T _C =100°C	4.5	
		FSFR1700HS/L	T _C =25°C	6.0	
			T _C =100°C	3.9	
Package Section					
Torque	Recommended Screw Torque		5~7		kgf·cm

Notes:

- These parameters, although guaranteed, are tested only in EDS (wafer test) process.
- Per MOSFET when both MOSFETs are conducting.
- The maximum value of the recommended operating junction temperature is limited by thermal shutdown.
- Pulse width is limited by maximum junction temperature.

Thermal Impedance

$T_A=25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter		Value	Unit
θ_{JC}	Junction-to-Case Center Thermal Impedance (Both MOSFETs Conducting)	FSFR1800HS/L	10.7	°C/W
		FSFR1700HS/L	10.8	
θ_{JA}	Junction-to-Ambient Thermal Impedance	FSFR1800HS/L FSFR1700HS/L	80	°C/W

Electrical Characteristics

$T_A=25^\circ\text{C}$, LV_{CC} , $HV_{CC}=17\text{ V}_{DC}$ and $R_T=26\text{ k}\Omega$ unless otherwise specified.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
MOSFET Section							
BV _{DSS}	Drain-to-Source Breakdown Voltage		I _D =200 μA, T _A =25°C	500			V
			I _D =200 μA, T _A =125°C		540		
R _{DS(ON)}	On-State Resistance	FSFR1800HS/L	V _{GS} =10 V, I _D =3.0 A		0.77	0.95	Ω
		FSFR1700HS/L	V _{GS} =10 V, I _D =2.0 A		1.00	1.25	
t _{rr}	Body Diode Reverse Recovery Time ⁽⁷⁾	FSFR1800HS/L	V _{GS} =0 V, I _{DIODE} =7.0 A, dI _{DIODE} /dt=100 A/μs		160		ns
		FSFR1700HS/L	V _{GS} =0 V, I _{DIODE} =6.0 A, dI _{DIODE} /dt=100 A/μs		160		
C _{ISS}	Input Capacitance ⁽⁷⁾	FSFR1800HS/L	V _{DS} =25 V, V _{GS} =0 V, f=1.0 MHz		639		pF
		FSFR1700HS/L			512		pF
C _{OSS}	Output Capacitance ⁽⁷⁾	FSFR1800HS/L			82.1		pF
		FSFR1700HS/L			66.5		pF
Supply Section							
I _{LK}	Offset Supply Leakage Current		HV _{CC} =V _{CTR} =500 V			50	μA
I _{QHVCC}	Quiescent HV _{CC} Supply Current		(HV _{CC} UV+) - 0.1 V		50	120	μA
I _{QLVCC}	Quiescent LV _{CC} Supply Current		(LV _{CC} UV+) - 0.1 V		100	200	μA
I _{OHVCC}	Operating HV _{CC} Supply Current (RMS Value)		f _{OSC} =50 KHz		6	9	mA
			No Switching		100	200	μA
I _{OLVCC}	Operating LV _{CC} Supply Current (RMS Value)		f _{OSC} =50 KHz		7	11	mA
			No Switching		2	4	mA
UVLO Section							
LV _{CC} UV+	LV _{CC} Supply Under-Voltage Positive Going Threshold (LV _{CC,START})			11.2	12.5	13.8	V
LV _{CC} UV-	LV _{CC} Supply Under-Voltage Negative Going Threshold (LV _{CC,STOP})			8.9	10.0	11.1	V
LV _{CC} UVH	LV _{CC} Supply Under-Voltage Hysteresis				2.5		V
HV _{CC} UV+	HV _{CC} Supply Under-Voltage Positive Going Threshold (HV _{CC,START})			8.2	9.2	10.2	V
HV _{CC} UV-	HV _{CC} Supply Under-Voltage Negative Going Threshold (HV _{CC,STOP})			7.8	8.7	9.6	V
HV _{CC} UVH	HV _{CC} Supply Under-Voltage Hysteresis				0.5		V
Oscillator & Feedback Section							
V _{RT}	Output Voltage on RT Pin		R _T =26 kΩ	1.5	2.0	2.5	V
f _{OSC}	Output Oscillation Frequency			47	50	53	kHz
DC	Output Duty Cycle			48	50	52	%

Continued on the following page...

Electrical Characteristics (Continued)

$T_A=25^{\circ}\text{C}$, LV_{CC} , $HV_{CC}=17\text{ V}_{DC}$ and $R_T=26\text{ k}\Omega$ unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Protection Section						
$V_{RT,RESET}$	Threshold Voltage to Begin Restart		0.07	0.12	0.17	V
$t_{DELAY,RESET}$	Delay to Disable OSC Circuit After Protection	$f_{osc}=50\text{ kHz}$		20		ms
V_{LINE}	On Threshold of Input Voltage		2.38	2.50	2.62	V
I_{LINE}	Hysteresis Current for Line UVLO		7.5	9.5	11.5	μA
V_{OVP}	LV_{CC} Over-Voltage Protection		21	23	25	V
V_{AOCP}	AOCP Threshold Voltage		-1.0	-0.9	-0.8	V
t_{BAO}	AOCP Blanking Time ⁽⁷⁾	$V_{CS} < V_{AOCP}$		50		ns
V_{OCP}	OCP Threshold Voltage		-0.64	-0.58	-0.52	V
t_{BO}	OCP Blanking Time ⁽⁷⁾	$V_{CS} < V_{OCP}$	1.0	1.5	2.0	μs
t_{DA}	Delay Time (Low-Side) Detecting from V_{AOCP} to Switch Off ⁽⁷⁾			250	400	ns
T_{SD}	Thermal Shutdown Temperature ⁽⁷⁾		120	135	150	$^{\circ}\text{C}$
Dead-Time Control Section						
D_T	Dead Time ⁽⁸⁾			350		ns

Notes:

7. This parameter, although guaranteed, is not tested in production.
8. These parameters, although guaranteed, are tested only in EDS (wafer test) process.

Typical Performance Characteristics

These characteristic graphs are normalized at $T_A=25^\circ\text{C}$.

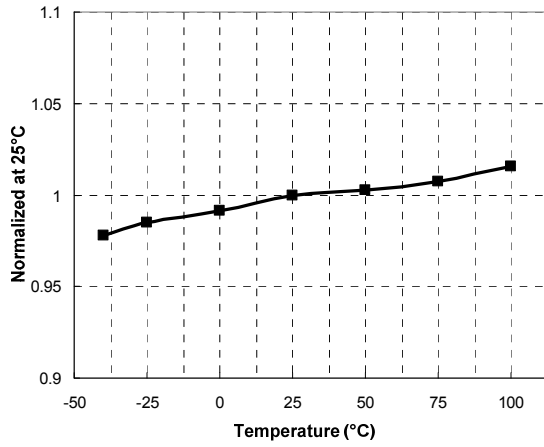


Figure 4. Low-Side MOSFET Duty Cycle vs. Temperature

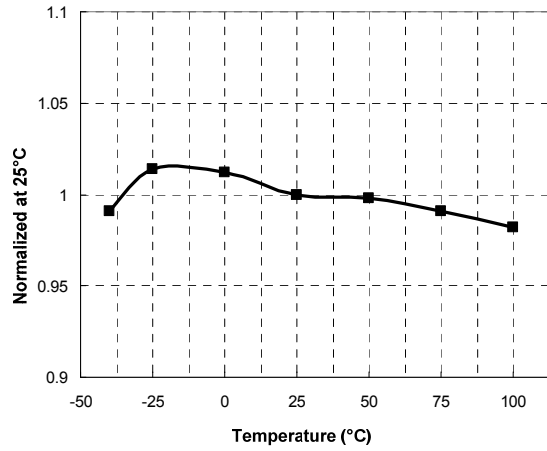


Figure 5. Switching Frequency vs. Temperature

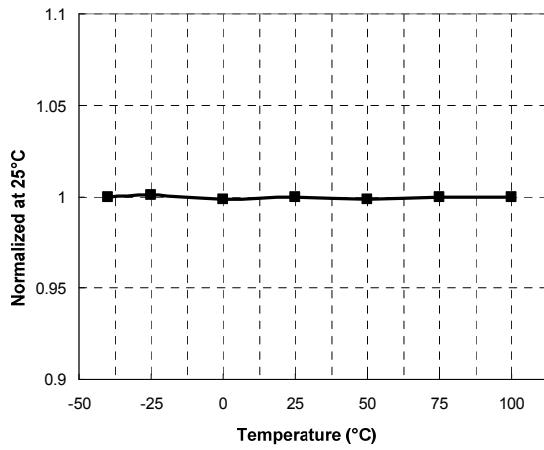


Figure 6. High-Side V_{CC} (HV_{CC}) Start vs. Temperature

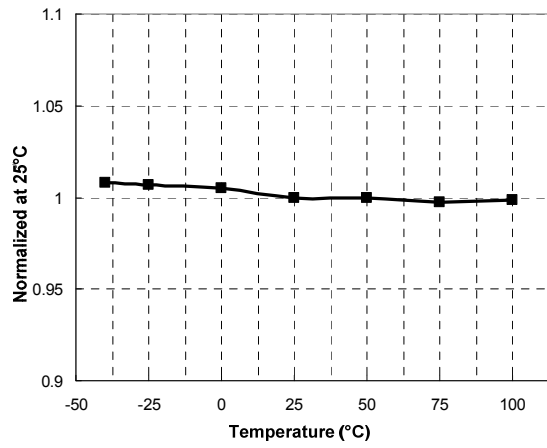


Figure 7. High-Side V_{CC} (HV_{CC}) Stop vs. Temperature

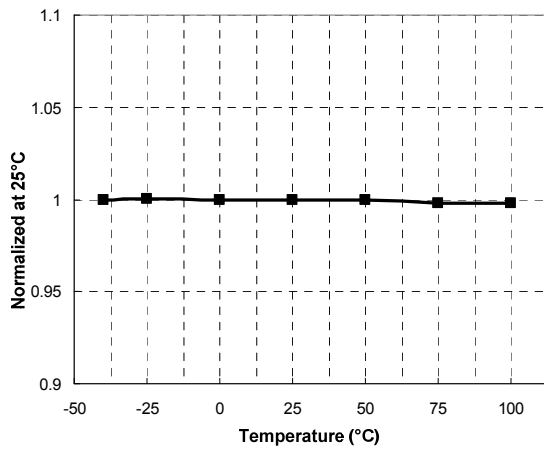


Figure 8. Low-Side V_{CC} (LV_{CC}) Start vs. Temperature

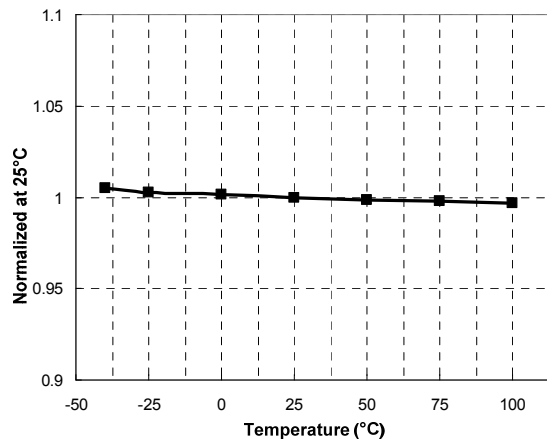


Figure 9. Low-Side V_{CC} (LV_{CC}) Stop vs. Temperature

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at $T_A=25^\circ\text{C}$.

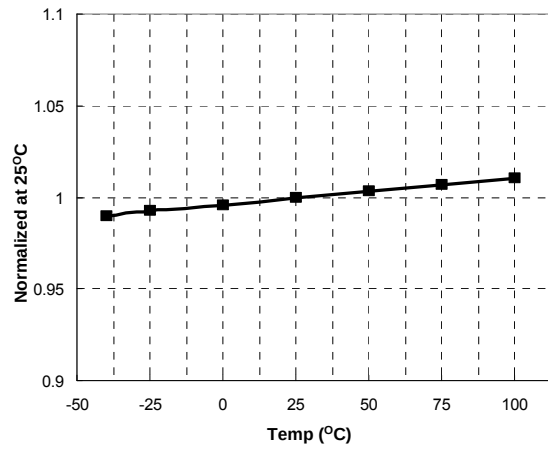


Figure 10. LV_{CC} OVP Voltage vs. Temperature

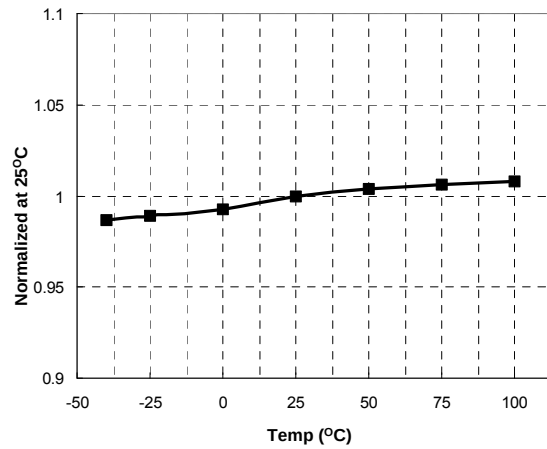


Figure 11. RT Voltage vs. Temperature

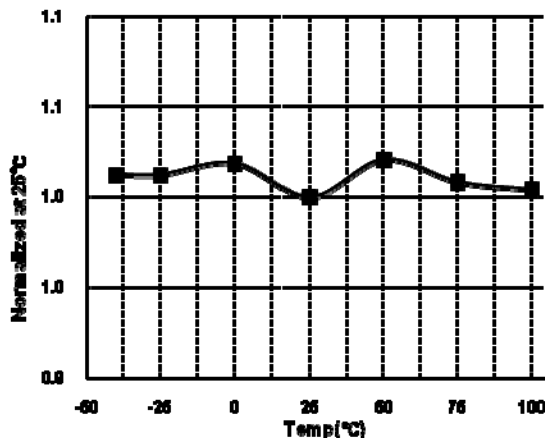


Figure 12. V_{RT,RESET} vs. Temperature

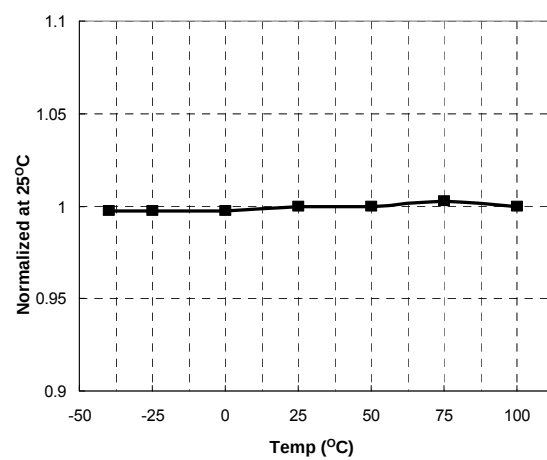


Figure 13. OCP Voltage vs. Temperature

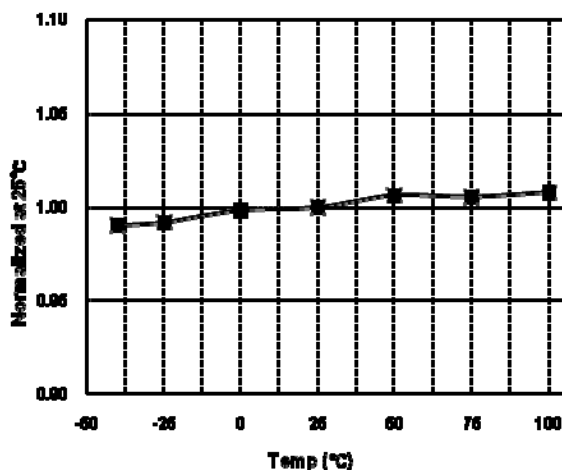


Figure 14. V_{LINE} vs. Temperature

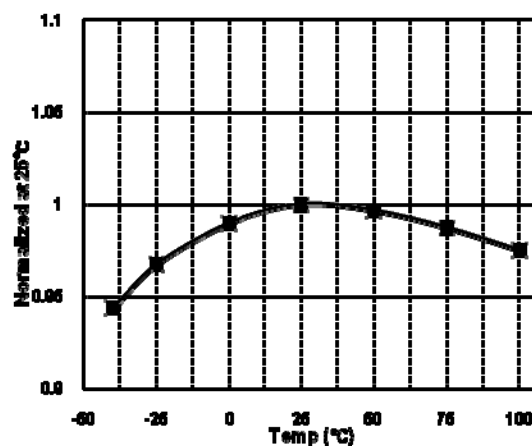


Figure 15. I_{LINE} vs. Temperature

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at $T_A=25^\circ\text{C}$.

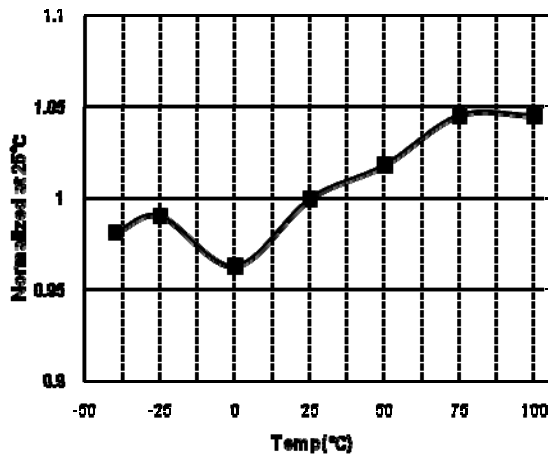


Figure 16. $t_{\text{DELAY,RESET}}$ vs. Temperature

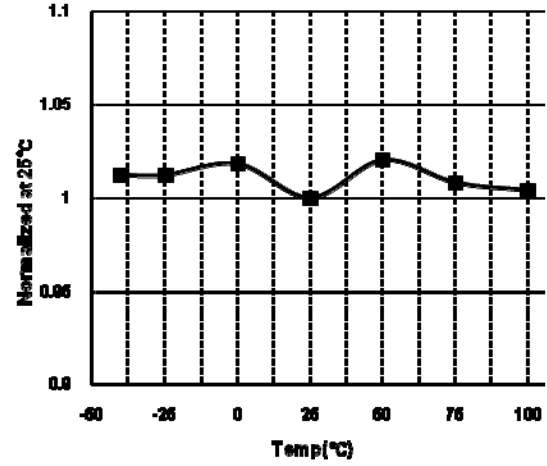


Figure 17. $V_{\text{RT,RESET}}$ vs. Temperature

Functional Description

1. Basic Operation: FSFR-HS series is designed to drive high-side and low-side MOSFETs complementarily with 50% duty cycle. A fixed dead time of 350 ns is introduced between consecutive transitions, as shown in Figure 18.

Once LV_{CC} is higher than $LV_{CC,START} = 12.5\text{ V}$, the IC starts to operate, generates the low-side gate signal, and drives the low-side MOSFET. The bootstrap diode and capacitor is charged by the low-side MOSFET's operation. After the voltage on HV_{CC} increases up to $HV_{CC,START}$, typically 9.2 V, the high-side gate signal is generated for the MOSFET.

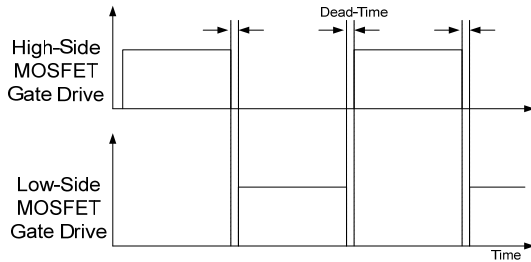


Figure 18. MOSFET Gate Drive Signals

2. Internal Oscillator: FSFR-HS series employs a current-controlled oscillator, as shown in Figure 19. Internally, the voltage of the RT pin is regulated at 2 V and the charging / discharging current for the oscillator capacitor, C_T , is obtained by copying the current flowing out of the RT pin (I_{CTC}) using a current mirror. Therefore, the switching frequency increases as I_{CTC} increases.

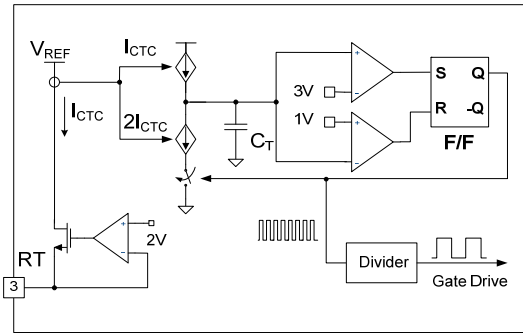


Figure 19. Current-Controlled Oscillator

3. Frequency Setting: Figure 20 shows the typical voltage gain curve of a resonant converter, where the gain is inversely proportional to the switching frequency in the ZVS region. The output voltage can be regulated by modulating the switching frequency. Figure 21 shows the typical circuit configuration for the RT pin, where the opto-coupler transistor is connected to the RT pin to modulate the switching frequency. The switching frequency may be controlled from 20 kHz to 500 kHz.

The minimum switching frequency is determined as:

$$f_{min} = \frac{1}{792 p \times R_{min} + 0.54 \mu} \text{ [Hz]} \quad (1)$$

Assuming the saturation voltage of opto-coupler transistor is 0.2 V, the maximum switching frequency is determined as:

$$f_{max} = \frac{1}{792 p \times R_{min} || R_{max} + 0.54 \mu} \text{ [Hz]} \quad (2)$$

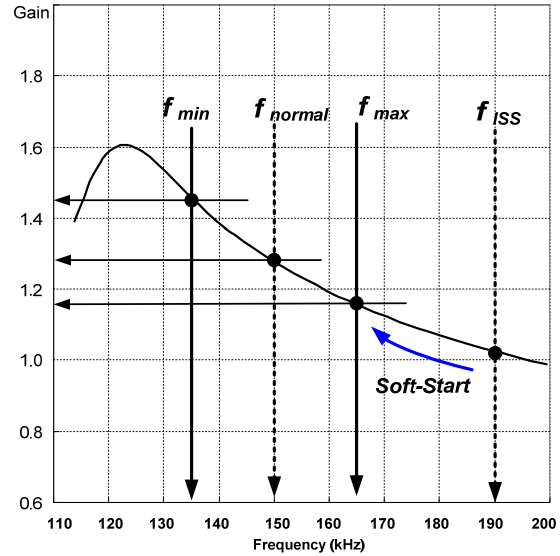


Figure 20. Resonant Converter Typical Gain Curve

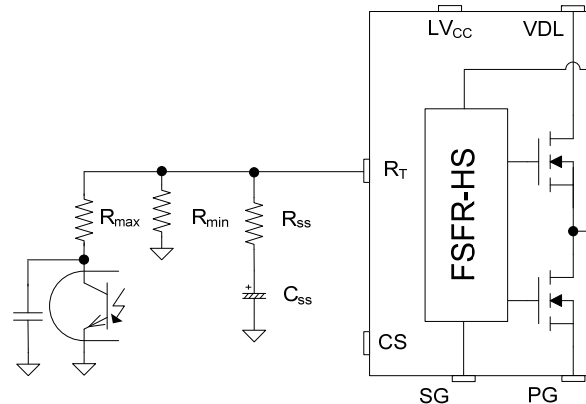


Figure 21. Frequency Control Circuit

To prevent excessive inrush current and overshoot of output voltage during startup, the IC needs to increase the voltage gain of the resonant converter progressively. Since the voltage gain of the resonant converter is inversely proportional to the switching frequency, soft-start is implemented by sweeping down the switching frequency from an initial high frequency (f_{SS}) until the output voltage is established.

The soft-start circuit is constructed by connecting R-C series network to the RT pin, as shown in Figure 21. Initially, the operating frequency is set by the parallel impedance of R_{SS} and R_{min} .

The initial maximum frequency can be set up to 600 kHz, which is given by:

$$f_{ss} = \frac{1}{792 p \times R_{\min} \| R_{ss} + 0.54 \mu} [Hz] \quad (3)$$

C_{Filter} can be used to reduce some noise induced from transformer or switching transition. Generally, hundreds of pico-farad to tens of nano-farad is adequate, depending on the quantity of noise.

The start and stop input-voltage can be calculated as:

$$V_{dc-link,STOP} = V_{LINE} \times \frac{R1 + R2}{R2} [V] \quad (6)$$

$$V_{dc-link,START} = V_{dc-link,STOP} + I_{LINE} \times R1 [V] \quad (7)$$

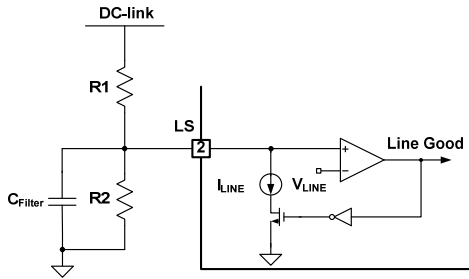


Figure 25. Half-Wave Sensing

7. Simple Remote-On/Off: The power stage can be shutdown with optional Auto-Restart Mode, as shown in Figure 26.

To configure an external protection with Auto-Restart Mode, an opto-coupler and the LS pin are used. When the voltage on the LS pin is pulled below V_{LINE} (2.5 V), the IC stops during the status holds. However, the opto-coupler stops pulling down and the IC can perform the auto-restart operation itself.

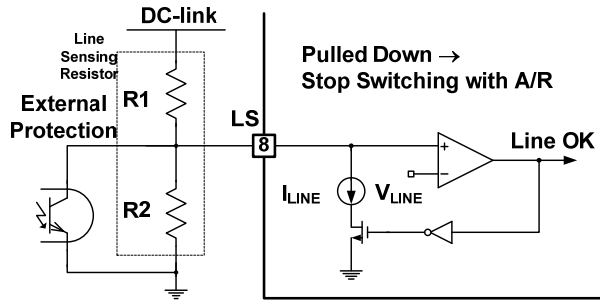


Figure 26. External Protection Circuits

8. Current-Sensing Methods: FSFR-HS series employs negative voltage sensing to detect the drain current of MOSFET, which allows a low-noise resistive sensing using a filter with low time-constant and capacitive sensing method.

8.1 Resistive Sensing Method: The IC can sense drain current as a negative voltage, as shown in Figure 27 and Figure 28. Half-wave sensing allows low power dissipation in the sensing resistor; while full-wave sensing has less switching noise in the sensing signal. For a time constant range for the filter, 3/100~1/10 of the operating frequency is reasonable.

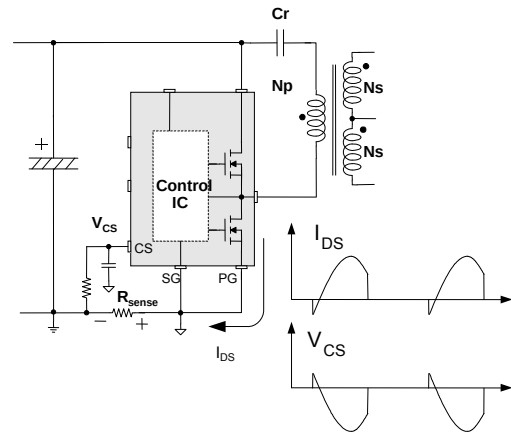


Figure 27. Half-Wave Sensing

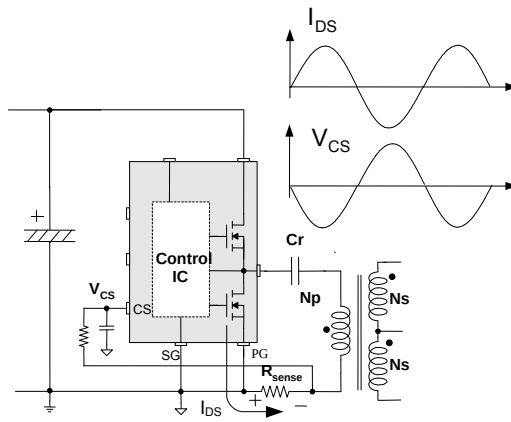


Figure 28. Full-Wave Sensing

8.2 Capacitive Sensing Method: The drain current can be sensed using an additional capacitor parallel with the resonant capacitor, as shown in Figure 29. During the low-side switch turn on, the current, i_{CB} through C_B , makes V_{SENSE} across R_{SENSE} . The i_{CB} is scale-down of i_p by the impedance ratio of C_r and C_B . Generally, 1/100~1/1000 is adequate for the ratio of C_B against C_r . R_D is used as a damper for reducing noise generated by switching transition. Several hundreds of ohm to a few of kilo-ohms can be normally used.

V_{SENSE} can be estimated as;

$$V_{sense} = I_{Cr}^{pk} \frac{C_B}{C_r} \cdot R_{sense} [V] \quad (8)$$

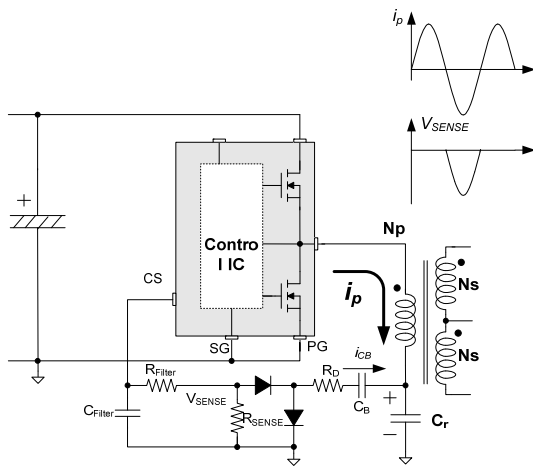
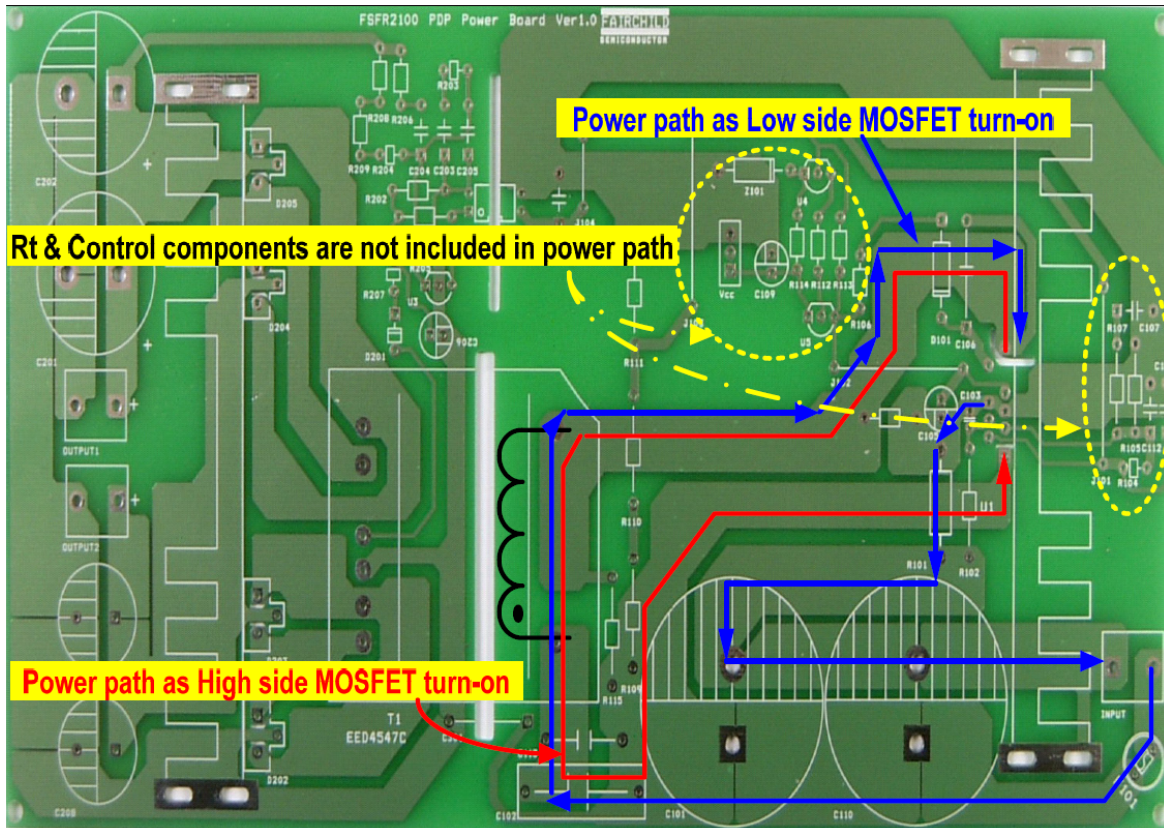
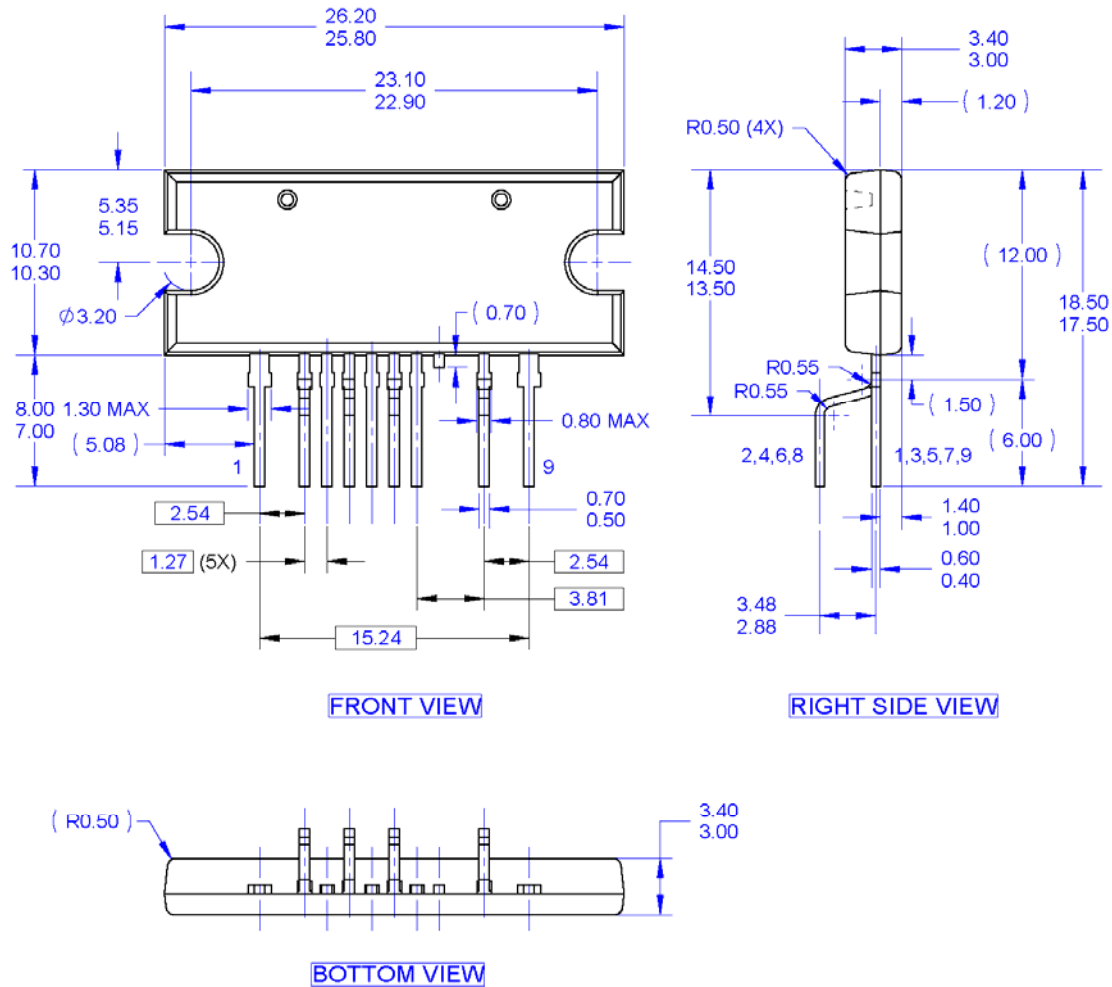


Figure 29. Capacitive Sensing

9. PCB Layout Guidelines: Duty imbalance problems may occur due to the radiated noise from the main transformer, the inequality of the secondary side leakage inductances of main transformer, and so on. This is one of the reasons that the control components in the vicinity of the RT pin are enclosed by the primary current flow pattern on PCB layout. The direction of the magnetic field on the components caused by the primary current flow is changed when the high- and low-side MOSFET turn on by turns. The magnetic fields with opposite directions induce a current through, into, or out of the RT pin, which makes the turn-on duration of each MOSFET different. It is strongly recommended to separate the control components in the vicinity of the RT pin from the primary current flow pattern in the PCB layout. Figure 30 shows an example for a duty-balanced case.



Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

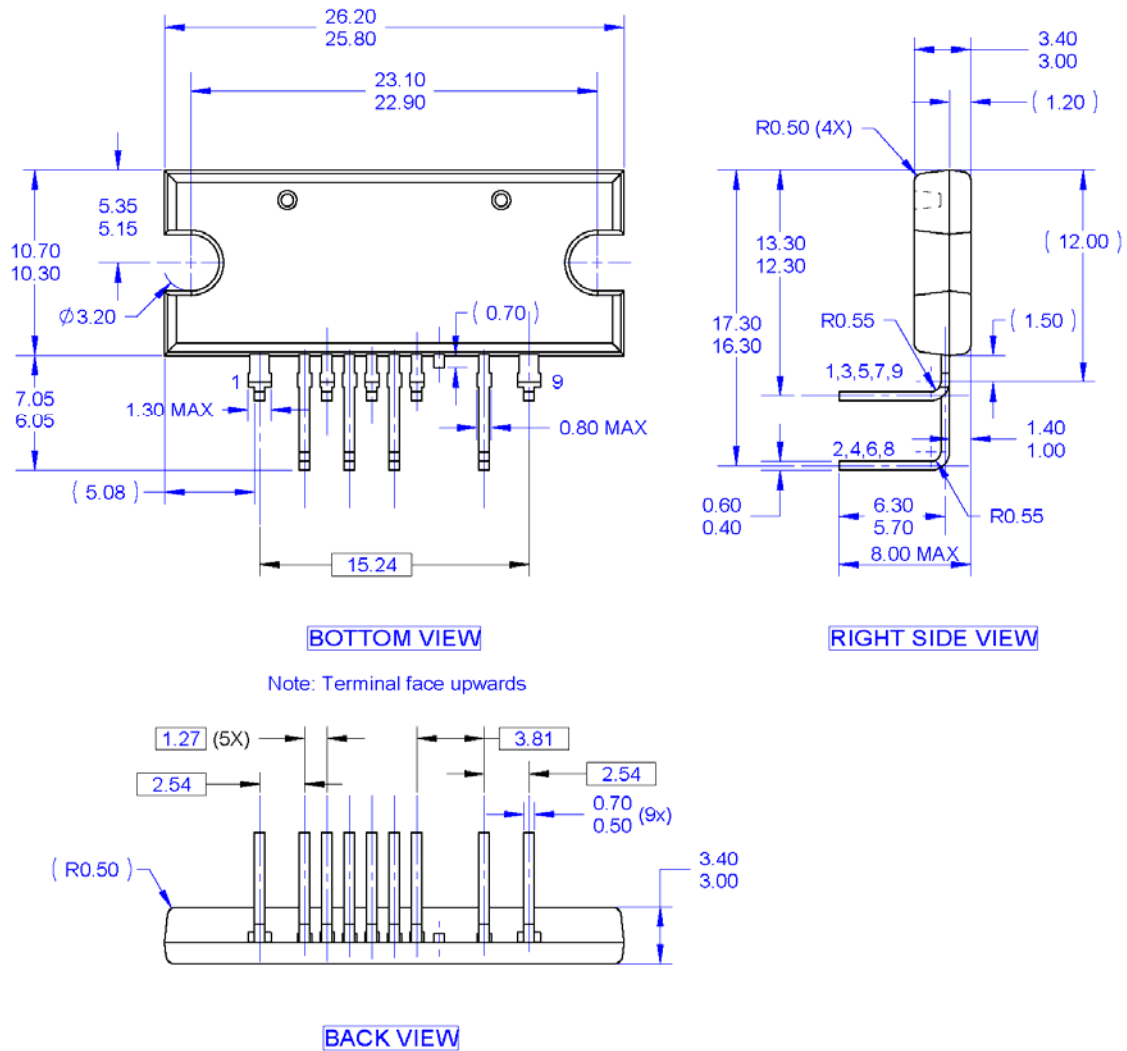
- A. THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- D. DRAWING FILE NAME: MOD09ACREV2

Figure 31. 9-Lead, Single Inline Package (SIP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
<http://www.fairchildsemi.com/packaging/>.

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A. THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- D. DRAWING FILE NAME: MOD09ADREV1.

Figure 32. 9-Lead, Single Inline Package (SIP), L-Forming

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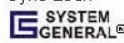
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