

FEATURES

- ❑ 2K x 8 Static RAM with Chip Select Powerdown, Output Enable
- ❑ Auto-Powerdown™ Design
- ❑ Advanced CMOS Technology
- ❑ High Speed — to 15 ns maximum
- ❑ Low Power Operation
 - Active: 425 mW typical at 25 ns
 - Standby (typical): 400 μ W (L6116)
200 μ W (L6116-L)
- ❑ Data Retention at 2 V for Battery Backup Operation
- ❑ DESC SMD No.
 - 5962-84036 — L6116
 - 5962-89690 — L6116
 - 5962-88740 — L6116-L
- ❑ Available 100% Screened to MIL-STD-883, Class B
- ❑ Plug Compatible with IDT6116, Cypress CY7C128/CY6116
- ❑ Package Styles Available:
 - 24-pin Plastic DIP
 - 24-pin CerDIP
 - 24-pin Plastic SOJ
 - 24-pin Ceramic Flatpack
 - 28-pin Ceramic LCC
 - 32-pin Ceramic LCC

DESCRIPTION

The **L6116** is a high-performance, low-power CMOS Static RAM. The storage circuitry is organized as 2048 words by 8 bits per word. The 8 Data In and Data Out signals share I/O pins. These devices are available in three speeds with maximum access times from 15 ns to 25 ns.

Inputs and outputs are TTL compatible. Operation is from a single +5 V power supply. Power consumption for the L6116 is 425 mW (typical) at 25 ns. Dissipation drops to 60 mW (typical) for the L6116 and 50 mW (typical) for the L6116-L when the memory is deselected.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L6116 and L6116-L consume only 30 μ W and 15 μ W

(typical) respectively, at 3 V, allowing effective battery backup operation.

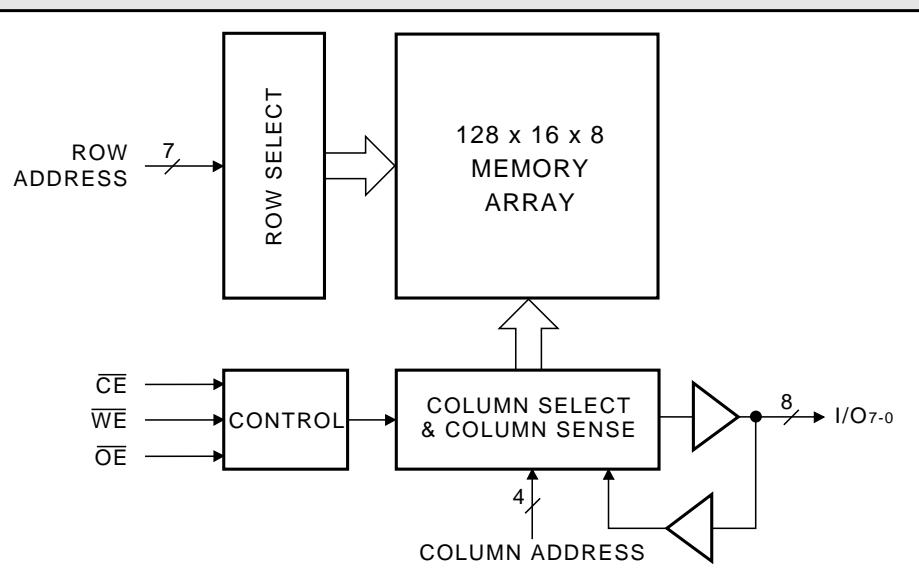
The L6116 provides asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A0 through A10. Reading from a designated location is accomplished by presenting an address and driving \overline{CE} and \overline{OE} LOW, while \overline{WE} remains HIGH. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when \overline{CE} or \overline{OE} is HIGH, or \overline{WE} is LOW.

Writing to an addressed location is accomplished when the active-low \overline{CE} and \overline{WE} inputs are both LOW. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L6116 can withstand an injection current of up to 200 mA on any pin without damage.

L6116 BLOCK DIAGRAM



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	-65°C to +150°C
Operating ambient temperature	-55°C to +125°C
V _{CC} supply voltage with respect to ground	-0.5 V to +7.0 V
Input signal with respect to ground	-3.0 V to +7.0 V
Signal applied to high impedance output	-3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics***Mode** **Temperature Range (Ambient)** **Supply Voltage**

Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V _{CC} ≤ 5.5 V
Active Operation, Industrial	-40°C to +85°C	4.5 V ≤ V _{CC} ≤ 5.5 V
Active Operation, Military	-55°C to +125°C	4.5 V ≤ V _{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V _{CC} ≤ 5.5 V
Data Retention, Industrial	-40°C to +85°C	2.0 V ≤ V _{CC} ≤ 5.5 V
Data Retention, Military	-55°C to +125°C	2.0 V ≤ V _{CC} ≤ 5.5 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

Symbol	Parameter	Test Condition	L6116			L6116-L			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output High Voltage	V _{CC} = 4.5 V, I _{OH} = -4.0 mA	2.4			2.4			V
V _{OL}	Output Low Voltage	I _{OL} = 8.0 mA			0.4			0.4	V
V _{IH}	Input High Voltage		2.2		V _{CC} +0.3	2.2		V _{CC} +0.3	V
V _{IL}	Input Low Voltage	(Note 3)	-3.0		0.8	-3.0		0.8	V
I _{IX}	Input Leakage Current	Ground ≤ V _{IN} ≤ V _{CC}	-10		+10	-10		+10	µA
I _{OZ}	Output Leakage Current	(Note 4)	-10		+10	-10		+10	µA
I _{CC2}	V _{CC} Current, TTL Inactive	(Note 7)		12	25		10	15	mA
I _{CC3}	V _{CC} Current, CMOS Standby	(Note 8)		80	300		40	150	µA
I _{CC4}	V _{CC} Current, Data Retention	V _{CC} = 3.0 V (Note 9)		10	150		5	50	µA
C _{IN}	Input Capacitance	Ambient Temp = 25°C, V _{CC} = 5.0 V			5			5	pF
C _{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7			7	pF

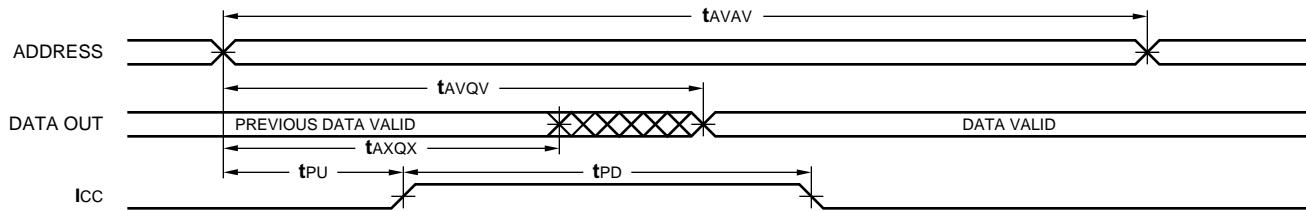
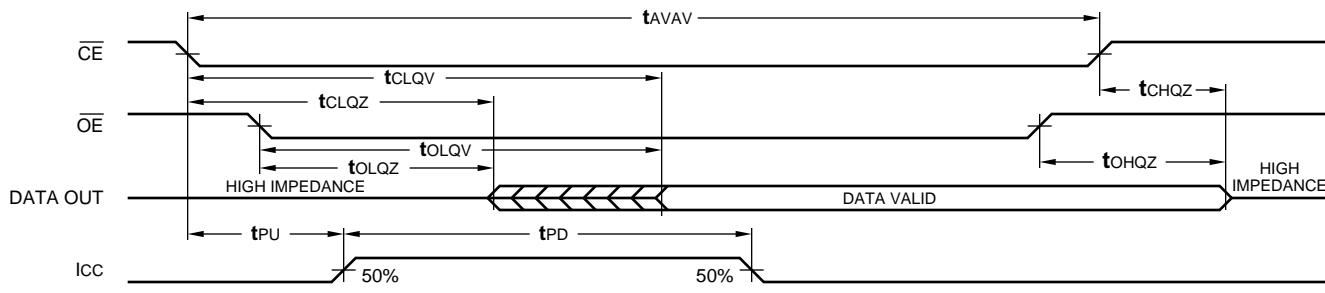
Symbol	Parameter	Test Condition	L6116-			
			25	20	15	Unit
I _{CC1}	V _{CC} Current, Active	(Note 6)	115	135	160	mA

SWITCHING CHARACTERISTICS Over Operating Range

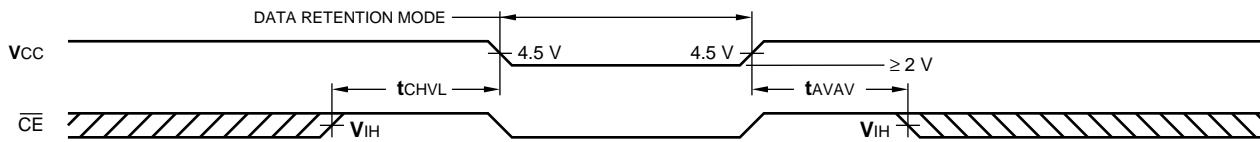
READ CYCLE Notes 5, 11, 12, 22, 23, 24 (ns)

Symbol	Parameter	L6116-					
		25		20		15	
		Min	Max	Min	Max	Min	Max
t_{AVAV}	Read Cycle Time	25		20		15	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		25		20		15
t_{AXQX}	Address Change to Output Change	3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		25		20		15
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		10		8		8
t_{OLQV}	Output Enable Low to Output Valid		12		10		8
t_{OLQZ}	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0	
t_{OHQZ}	Output Enable High to Output High Z (Notes 20, 21)		10		8		5
t_{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0	
t_{PD}	Power Up to Power Down (Notes 10, 19)		25		20		20
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0	

READ CYCLE — ADDRESS CONTROLLED Notes 13, 14

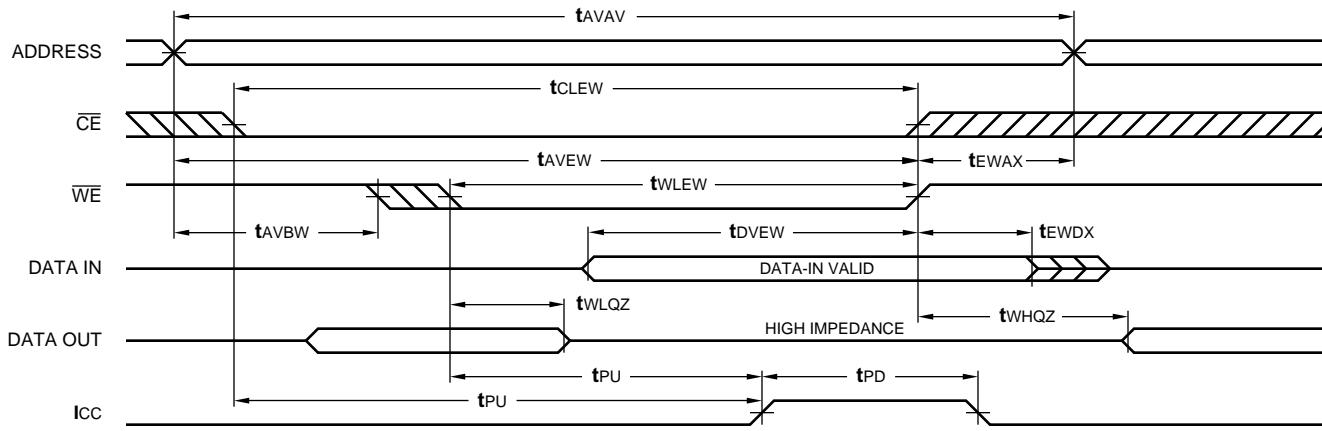
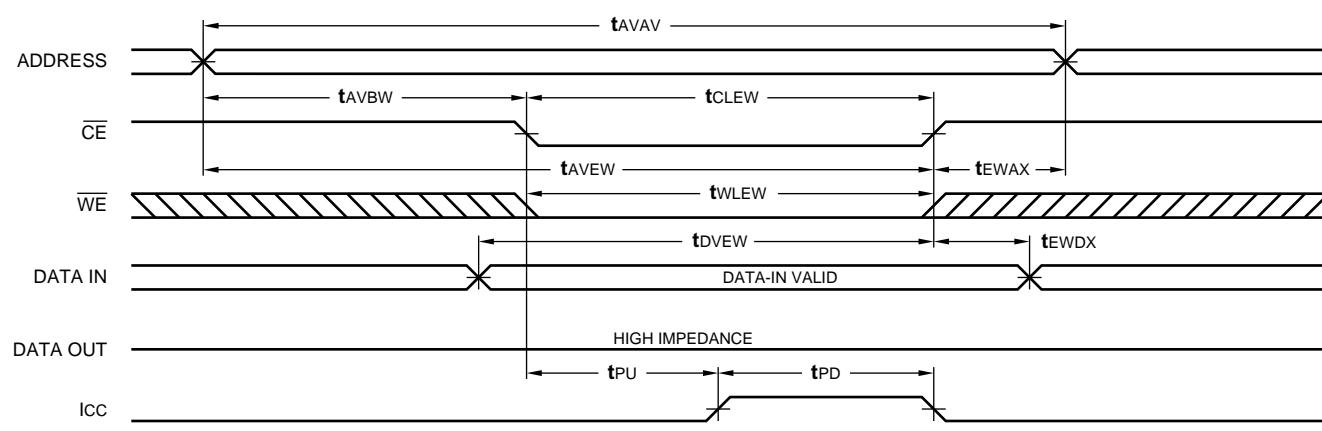
READ CYCLE — $\overline{CE}/\overline{OE}$ CONTROLLED Notes 13, 15

DATA RETENTION Note 9



SWITCHING CHARACTERISTICS *Over Operating Range*WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

Symbol	Parameter	L6116-					
		25		20		15	
		Min	Max	Min	Max	Min	Max
t_{AVAV}	Write Cycle Time	20		20		15	
t_{CLEW}	Chip Enable Low to End of Write Cycle	15		15		12	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0	
t_{AIEW}	Address Valid to End of Write Cycle	15		15		12	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	15		15		12	
t_{DVEW}	Data Valid to End of Write Cycle	10		10		7	
t_{EWDX}	End of Write Cycle to Data Change	1		1		1	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		7		7		5

WRITE CYCLE — \overline{WE} CONTROLLED *Notes 16, 17, 18, 19*WRITE CYCLE — \overline{CE} CONTROLLED *Notes 16, 17, 18, 19*

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at -0.6 V. A current in excess of 100 mA is required to reach -2.0 V. The device can withstand indefinite operation with inputs as low as -3 V subject only to power dissipation and bond wire fusing constraints.

4. Tested with $GND \leq VOUT \leq VCC$. The device is disabled, i.e., $\overline{CE} = VCC$.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE} \leq VIL$, $\overline{WE} \leq VIL$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \geq VIH$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = VCC$. Input levels are within 0.2 V of VCC or GND.

9. Data retention operation requires that VCC never drop below 2.0 V. \overline{CE} must be $\geq VCC - 0.2$ V. All other inputs must meet $VIN \geq VCC - 0.2$ V or $VIN \leq 0.2$ V to ensure full powerdown. For low power version (if applicable), this requirement applies only to \overline{CE} and \overline{WE} ; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tAVEW is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. WE is high for the read cycle.

14. The chip is continuously selected (\overline{CE} low).

15. All address lines are valid prior-to or coincident-with the \overline{CE} transition to active.

16. The internal write cycle of the memory is defined by the overlap of \overline{CE} active and WE low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If \overline{WE} goes low before or concurrent with the latter of \overline{CE} going active, the output remains in a high impedance state.

18. If \overline{CE} goes inactive before or concurrent with WE going high, the output remains in a high impedance state.

19. Powerup from $ICC2$ to $ICC1$ occurs as a result of any of the following conditions:

- Falling edge of \overline{CE} .
- Falling edge of WE (\overline{CE} active).
- Transition on any address line (\overline{CE} active).
- Transition on any data line (\overline{CE} , and WE active).

The device automatically powers down from $ICC1$ to $ICC2$ after tPD has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ± 200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. \overline{CE} or \overline{WE} must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 μ F high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

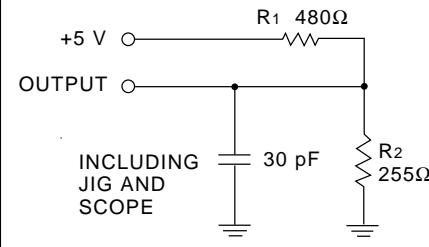


FIGURE 1b.

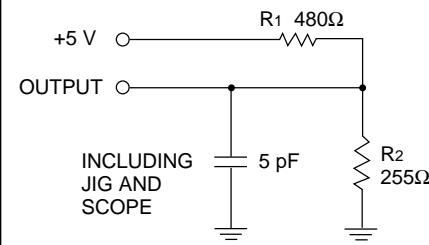
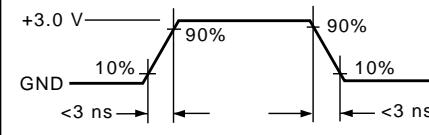
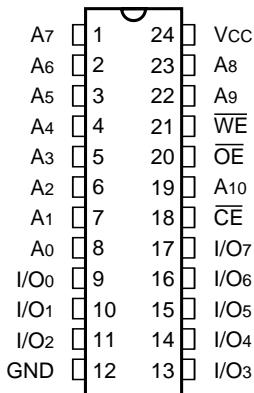


FIGURE 2.

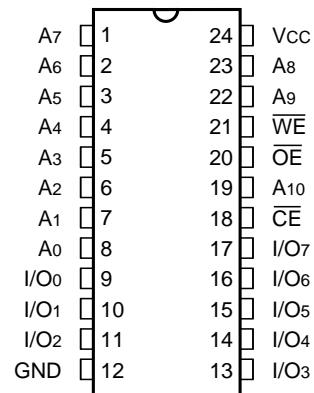


ORDERING INFORMATION

24-pin — 0.3" wide



24-pin — 0.6" wide



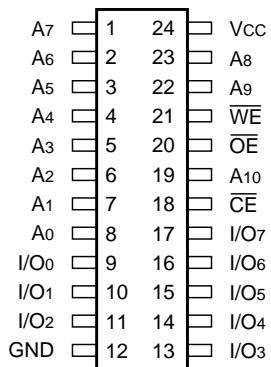
Speed	Plastic DIP (P2)	Ceramic DIP (C1)	Plastic DIP (P1)	Ceramic DIP (C4)
0°C to +70°C — COMMERCIAL SCREENING				
20 ns	L6116PC20*	L6116CC20*	L6116NC20*	L6116IC20*
15 ns	L6116PC15*	L6116CC15*	L6116NC15*	L6116IC15*
-40°C to +85°C — COMMERCIAL SCREENING				
20 ns	L6116PI20*		L6116NI20*	
15 ns	L6116PI15*		L6116NI15*	
-55°C to +125°C — COMMERCIAL SCREENING				
25 ns		L6116CM25*		L6116IM25*
20 ns		L6116CM20*		L6116IM20*
15 ns		L6116CM15*		L6116IM15*
-55°C to +125°C — MIL-STD-883 COMPLIANT				
25 ns		L6116CMB25*		L6116IMB25*
20 ns		L6116CMB20*		L6116IMB20*
15 ns		L6116CMB15*		L6116IMB15*

*The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L6116CMB15L)

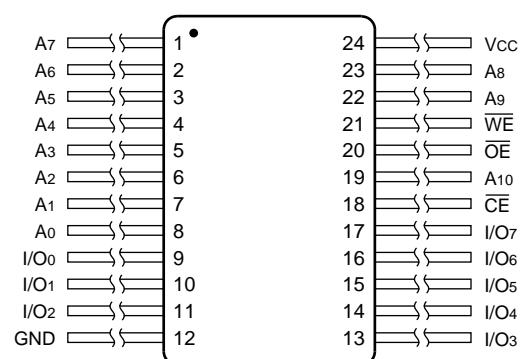
16K Static RAMs

ORDERING INFORMATION

24-pin — 0.3" wide



24-pin



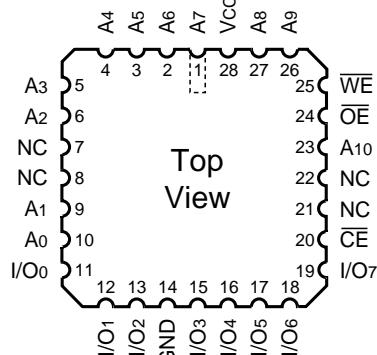
Speed	Plastic SOJ (W1)	Ceramic Flatpack (M1)
0°C to +70°C — COMMERCIAL SCREENING		
20 ns	L6116WC20*	L6116MC20*
15 ns	L6116WC15*	L6116MC15*
-40°C to +85°C — COMMERCIAL SCREENING		
20 ns	L6116WI20*	
15 ns	L6116WI15*	
-55°C to +125°C — COMMERCIAL SCREENING		
25 ns		L6116MM25*
20 ns		L6116MM20*
15 ns		L6116MM15*
-55°C to +125°C — MIL-STD-883 COMPLIANT		
25 ns		L6116MMB25*
20 ns		L6116MMB20*
15 ns		L6116MMB15*

*The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L6116MMB15L)

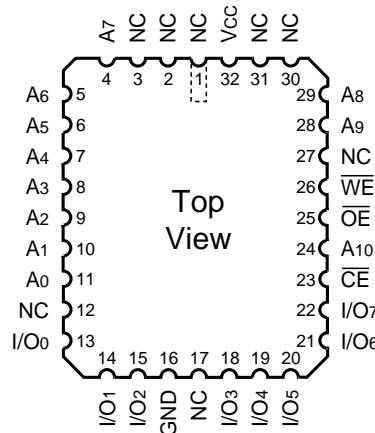
16K Static RAMs

ORDERING INFORMATION

28-pin



32-pin



Speed	Ceramic Leadless Chip Carrier (K1)	Ceramic Leadless Chip Carrier (K7)
0°C to +70°C — COMMERCIAL SCREENING		
20 ns	L6116KC20*	L6116TC20*
15 ns	L6116KC15*	L6116TC15*
-40°C to +85°C — COMMERCIAL SCREENING		
20 ns		
15 ns		
-55°C to +125°C — COMMERCIAL SCREENING		
25 ns	L6116KM25*	L6116TM25*
20 ns	L6116KM20*	L6116TM20*
15 ns	L6116KM15*	L6116TM15*
-55°C to +125°C — MIL-STD-883 COMPLIANT		
25 ns	L6116KMB25*	L6116TMB25*
20 ns	L6116KMB20*	L6116TMB20*
15 ns	L6116KMB15*	L6116TMB15*

*The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L6116KMB15L)

16K Static RAMs