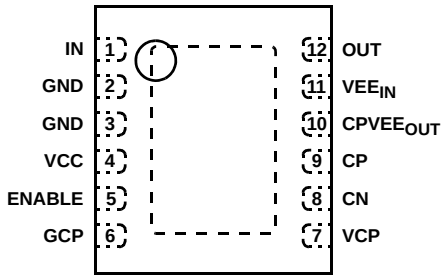
Single Supply Video Driver with Reconstruction Filter and Charge Pump

The ISL59831 is a single supply video driver with reconstruction filter and charge pump. It is designed to drive SDTV displays with luma (Y) or composite video (CV) signals. It operates on a single supply (3.0V to 3.6V) and generates its own negative supply (-1.9V) using a regulated charge pump. Input signal can be AC or DC coupled. When AC coupled, the sync tip clamp sets the blank level to ground at the output, ensuring that the sync-tip voltage level is set to approximately -300mV at the back-termination resistor of a standard video load. The ISL59831 is capable of driving two AC or DC coupled standard video loads. The device also features a 4^{th} order Butterworth reconstruction filter with nominal -3dB frequency set to 9.1MHz, providing 44dB of attenuation at 27MHz. When powered down, the device draws 2µA supply current. Nominal operational current is 15mA. The ISL59831 is available in 12 Ld TDFN package and operates from the -40°C to +85°C temperature range.

Pinout

ISL59831
(12 LD TDFN)
TOP VIEW



Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
ISL59831IRTZ	83IZ	-	12 Ld 4x3 TDFN	L12.4x3A
ISL59831IRTZ-T7	83IZ	7”	12 Ld 4x3 TDFN	L12.4x3A

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

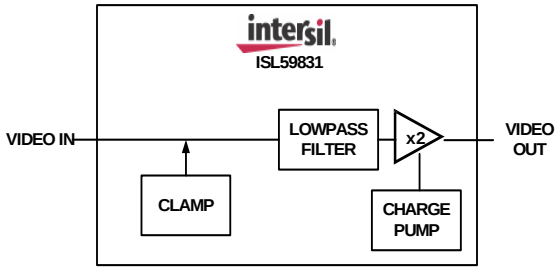
Features

- 3.3V Nominal Supply, Operates Down to 3.0V
- DC-Coupled or AC-Coupled Input or Output
- Eliminates Need for Large Output Coupling Capacitor
- Internal Sync Tip Clamp Puts the Backporch to Ground at the Output
- Drives Two Standard Video Loads
- Response Flat to 5MHz and 44dB Attenuation at 27MHz
- Pb-free Plus Anneal Available (RoHs Compliant)

Applications

- Set-Top Box Receiver
- Televisions
- DVD Players
- Digital Displays
- Cell Phones
- Digital Cameras

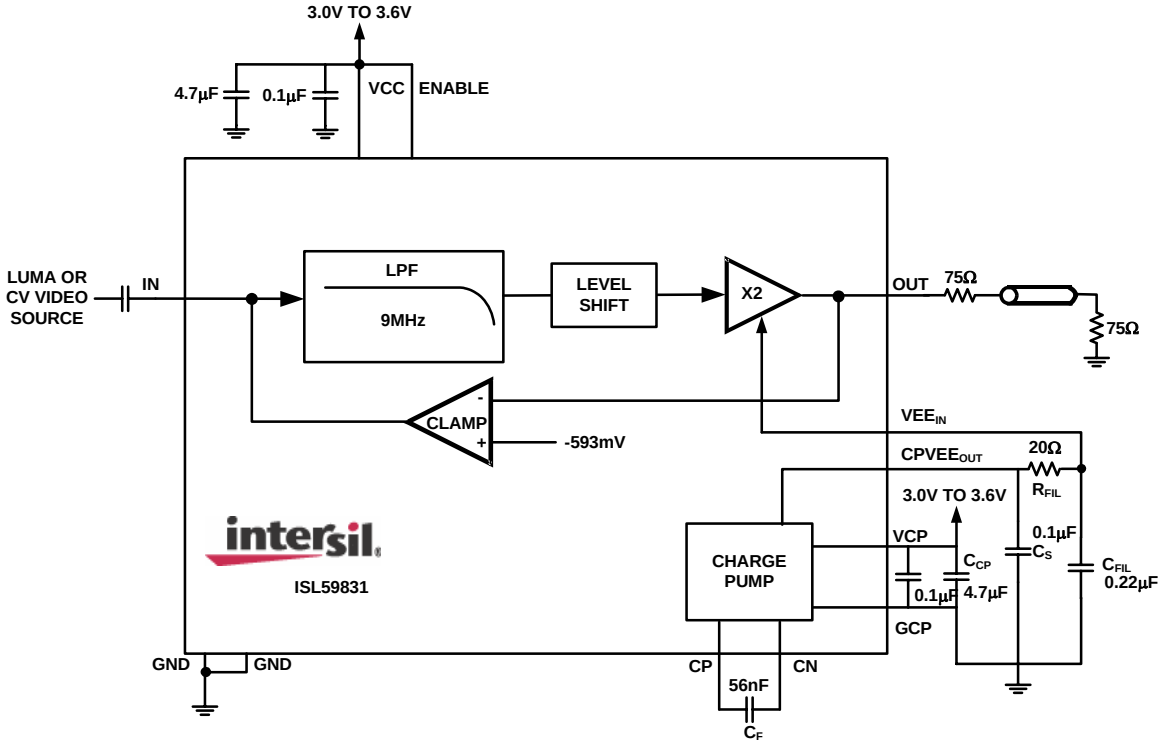
Simplified Block Diagram



Pin Descriptions

NUMBER	NAME	FUNCTION
1	IN	Video Input. AC-couple (0.1µF) or DC-couple
2, 3	GND	Ground
4	V_{CC}	Positive Power Supply. Bypass to GND with a 0.1µF capacitor.
5	ENABLE	Enable. Connect to V_{CC} to enable device.
6	GCP	Charge Pump Ground
7	VCP	Charge Pump Power Supply. Bypass with a 0.1µF capacitor to GCP.
8	CN	Charge-Pump Flying Capacitor Negative Terminal. Connect a 56nF capacitor from CP to CN.
9	CP	Charge-Pump Flying Capacitor Positive Terminal. Connect a 56nF capacitor from CP to CN.
10	$CPVEE_{OUT}$	Charge Pump Negative Output. Bypass with a 0.22µF capacitor to GCP.
11	VEE_{IN}	Negative Supply. Connect an RC filter between VEE_{IN} and $CPVEE_{OUT}$. See “Block Diagram/Typical Application Circuit” on page 2.
12	OUT	Video Output. Can be AC-coupled (220µF) or DC-coupled
	EP	Open or connect to VEE_{IN}

Block Diagram/Typical Application Circuit



Absolute Maximum Ratings (T_A = +25°C)

V_{CC} to GND 4V
V_{IN} to GND . . . . . .GND - 0.3V to V_{CC} + 0.3V
Maximum Continuous Output Current . . . . . ±50mA
Maximum Current into Any Pin . . . . . ±50mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . .3500V
Machine Model (Per EIAJ ED-4701 Method C-111) 350V

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
4x3 TDFN Package	41	3.5

Maximum Junction Temperature (Plastic Package) . . . . . .+150°C
Maximum Storage Temperature Range . . . . . .-65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . .+300°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . .-40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. θ_{JC}, "case temperature" location is at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

Electrical Specifications

$V_{CP} = V_{CC} = 3.3V$, $C_F = 56nF$ ±20%, $C_S = 0.1\mu F$ ±20%, $R_{FIL} = 20\Omega$ ±1%, $C_{FIL} = 0.22\mu F$ ±20%, $C_{IN} = 0.1\mu F$ ±20%, $R_L = 150\Omega$, $C_L = 0pF$, T_A = +27°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS						
V_{CC}, V_{CP}	Supply Range		3.0	3.3	3.6	V
CPVEE	Charge Pump Output		-1.1	-1.9	-2.4	V
I_{CC}	Supply Current	No load	4	6	8.5	mA
I_{CP}	Charge Pump Supply Current	No load	5	9	20	mA
I_{PD}	Power Down Current	ENABLE = 0.4V		2	5	µA
I_{IN}	Input Pulldown Current	V_{IN} = 0.5V	0.5	2	4.5	µA
A_V	DC Gain		1.9	2	2.06	V/V
V_{IN_MAX}	Max DC Input Range	DC-Coupled Input, guaranteed by output linearity	1.4			V
$V_{CLAMPOUT}$	Output Sync Tip Clamp Level	Sync height = 293mV, $V_{IN} \leq 0$, AC-coupled input	-500	-550	-600	mV
VCLAMPIN	Input Clamp Level	Input floating	0	40	80	mV
V_{OS}	Output Level Shift	Sync height = 293mV, $V_{IN} > 0$, output shifted relative to input, DC-coupled input	-530	-592	-650	mV
I_{CLAMP}	Clamp Restore Current	Force V_{IN} = -0.3V	2	3.9		mA
$PSRR_{DC}$	Power Supply Rejection	VCC = +3.0 to +3.6	35	50		dB
AC CHARACTERISTICS						
A_{PB}	Passband Flatness	f = 100kHz to 5MHz relative to 100kHz	0		2	dB
A_{SB}	Stopband Attenuation	f ≥ 27MHz relative to 100kHz	25	44		dB
dG	Differential Gain	5-step modulated staircase		0.4		%
dP	Differential Phase	5-step modulated staircase		0.35		°
SNR	Signal to Noise Ratio	Peak signal ($1.4V_{P-P}$) to RMS noise, f = 10Hz to 50MHz		59		dB

Electrical Specifications $V_{CP} = V_{CC} = 3.3V$, $C_F = 56nF$ ±20%, $C_S = 0.1\mu F$ ±20%, $R_{FIL} = 20\Omega$ ±1%, $C_{FIL} = 0.22\mu F$ ±20%, $C_{IN} = 0.1\mu F$ ±20%, $R_L = 150\Omega$, $C_L = 0pF$, $T_A = +27°C$, unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
tg	DC Group Delay	Group delay at 100kHz		56		ns
Δtg	Group Delay Deviation	Deviation from 100kHz to 3.58MHz		10		ns
H_{DIST}	Line Time Distortion	18µs, 100 $\overline{IRE}$		0.1		%
V_{DIST}	Field Time Distortion	130 Lines, 18µs, 100 $\overline{IRE}$		0.1		%
t_{CLAMP}	Clamp Settling Time	Back porch to ±1% of final value		50		Lines
PSRR	Power Supply Rejection	V_{CC} + 100mV_{P-P} sine, f = 100kHz to 5MHz		32		dB
LOGIC						
V_{IL}	Logic Low Input Voltage				0.8	V
V_{IH}	Logic High Input Voltage		2.0			V
I_I	Logic Input Current	Source	-10		10	µA
CHARGE PUMP						
f_{CP}	Charge Pump Clock Frequency			15		MHz
V_{OUTCP}	Charge Pump Noise Coupling	$R_{FIL} = 20\Omega$, $C_{FIL} = 0.22\mu F$, measured at output		10.8		mV_{P-P}

Typical Performance Curves

$V_{CP} = V_{CC} = 3.3V$, $C_F = 56nF \pm 20\%$, $C_S = 0.1\mu F \pm 20\%$, $R_{FIL} = 20\Omega \pm 1\%$, $C_{FIL} = 0.22\mu F \pm 20$, $C_{IN} = 0.1\mu F \pm 20\%$, $R_L = 150\Omega$, $C_L = 0pF$, unless otherwise noted.

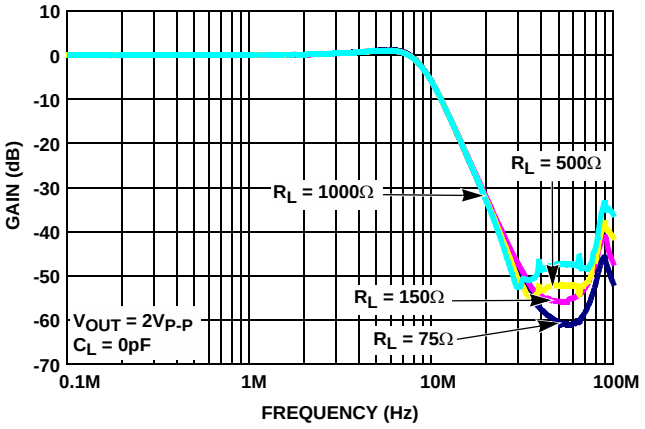


FIGURE 1. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD}

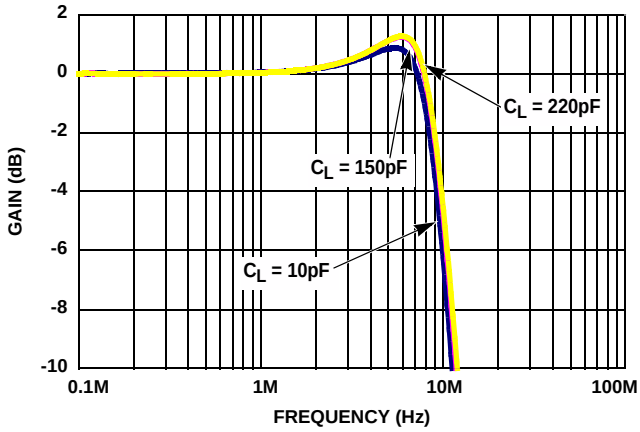


FIGURE 2. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD}

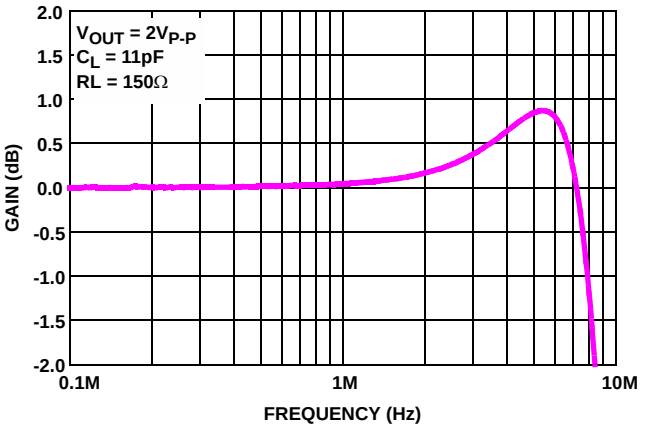


FIGURE 3. GAIN FLATNESS vs FREQUENCY

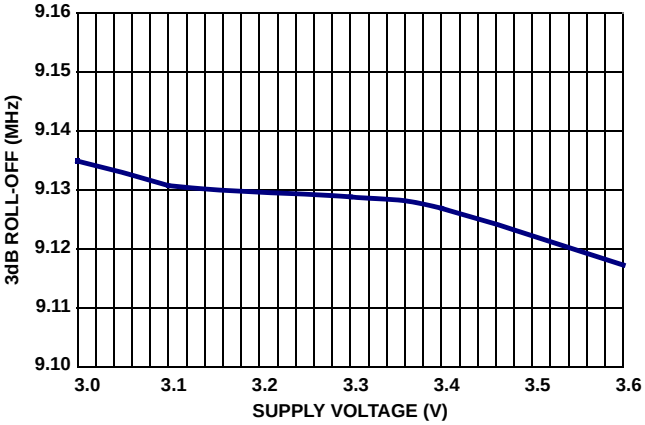


FIGURE 4. 3dB ROLL-OFF vs SUPPLY VOLTAGE

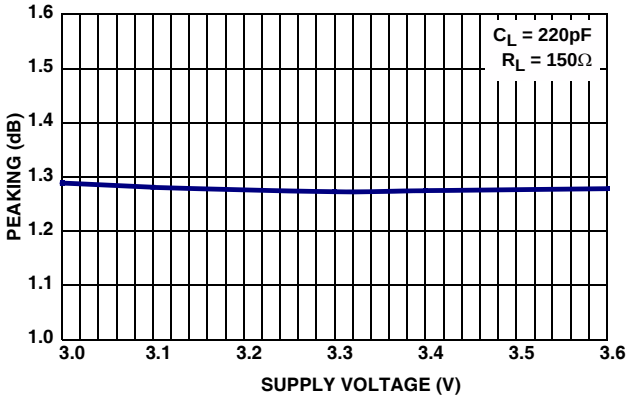


FIGURE 5. PEAKING vs SUPPLY VOLTAGE (C_L = 220pF)

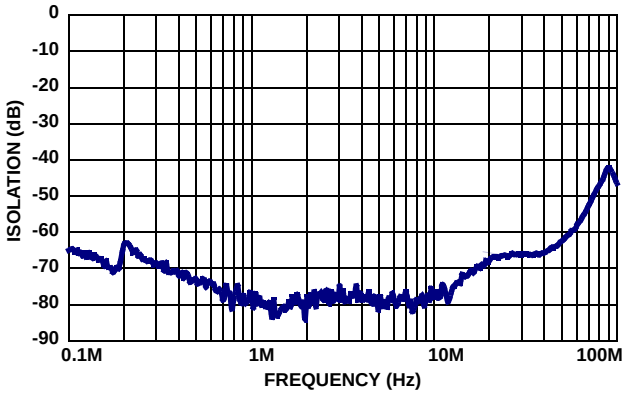


FIGURE 6. INPUT TO OUTPUT ISOLATION vs FREQUENCY

Typical Performance Curves $V_{CP} = V_{CC} = 3.3V$, $C_F = 56nF \pm 20\%$, $C_S = 0.1\mu F \pm 20\%$, $R_{FIL} = 20\Omega \pm 1\%$, $C_{FIL} = 0.22\mu F \pm 20$, $C_{IN} = 0.1\mu F \pm 20\%$, $R_L = 150\Omega$, $C_L = 0pF$, unless otherwise noted. **(Continued)**

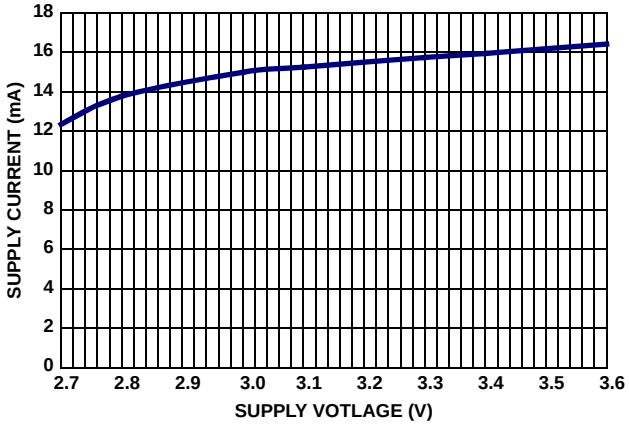


FIGURE 7. SUPPLY CURRENT vs SUPPLY VOLTAGE

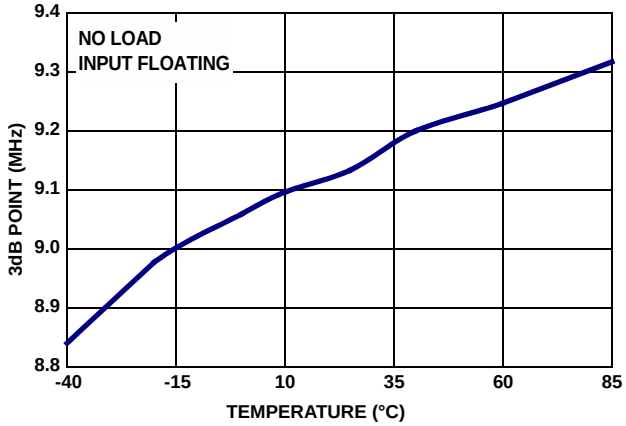


FIGURE 8. BANDWIDTH vs TEMPERATURE

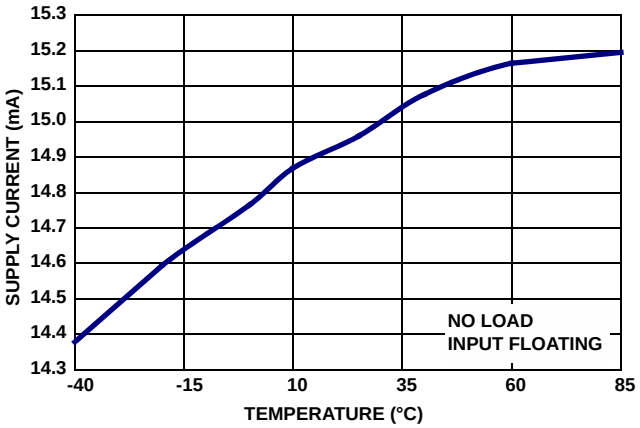


FIGURE 9. SUPPLY CURRENT vs TEMPERATURE

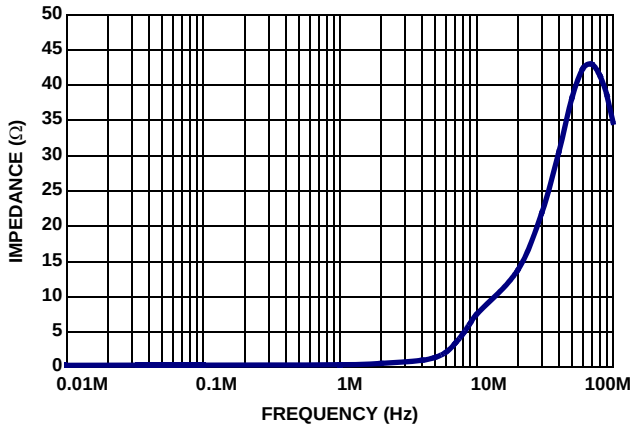


FIGURE 10. OUTPUT IMPEDANCE vs FREQUENCY

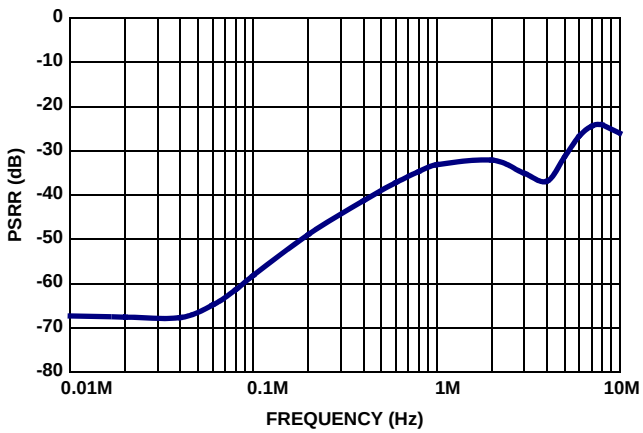


FIGURE 11. PSRR vs FREQUENCY

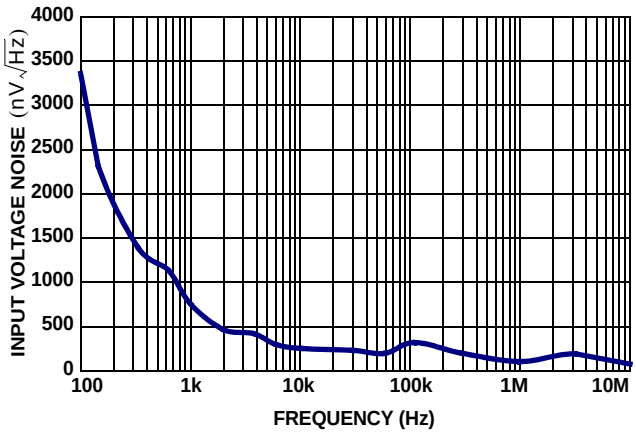


FIGURE 12. INPUT VOLTAGE NOISE vs FREQUENCY

Typical Performance Curves $V_{CP} = V_{CC} = 3.3V$, $C_F = 56nF \pm 20\%$, $C_S = 0.1\mu F \pm 20\%$, $R_{FIL} = 20\Omega \pm 1\%$, $C_{FIL} = 0.22\mu F \pm 20$, $C_{IN} = 0.1\mu F \pm 20\%$, $R_L = 150\Omega$, $C_L = 0pF$, unless otherwise noted. **(Continued)**

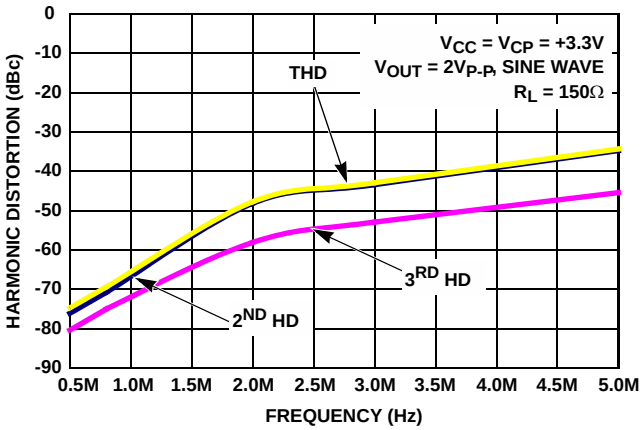


FIGURE 13. HARMONIC DISTORTION vs FREQUENCY

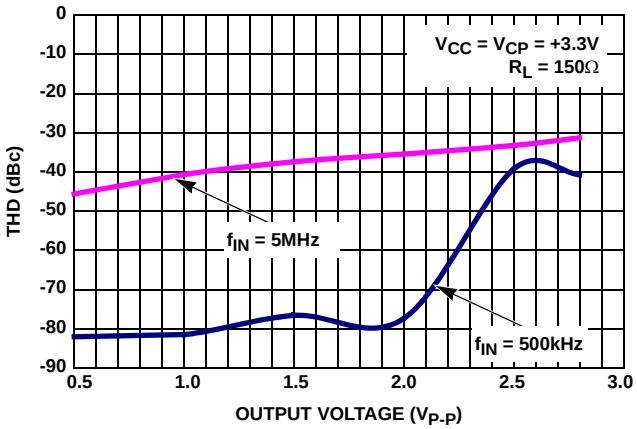


FIGURE 14. THD (dBc) vs OUTPUT VOLTAGE (V_{P-P})

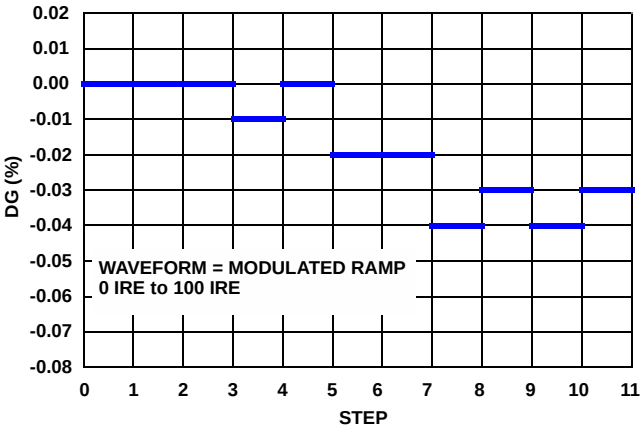


FIGURE 15. DIFFERENTIAL GAIN

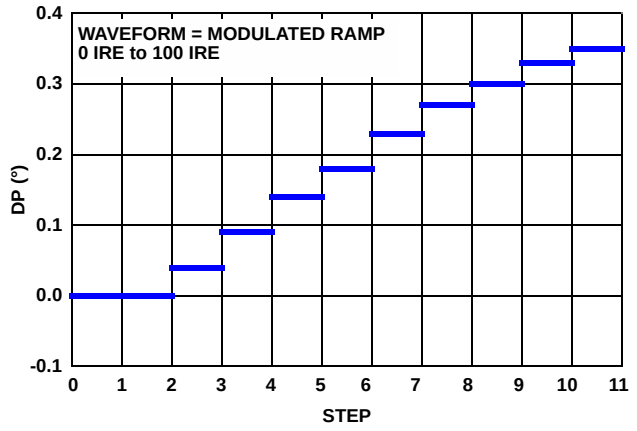


FIGURE 16. DIFFERENTIAL PHASE

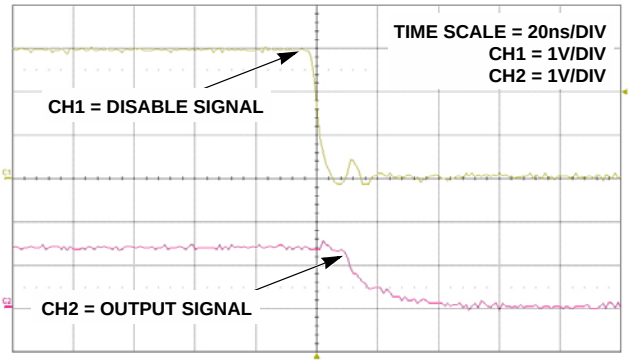


FIGURE 17. DISABLE TIME

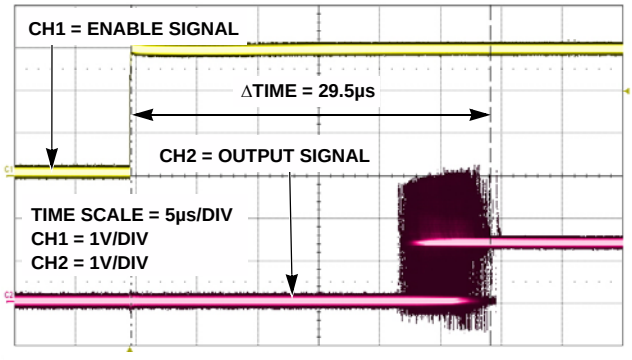


FIGURE 18. ENABLE TIME (WORST CASE)

Typical Performance Curves $V_{CP} = V_{CC} = 3.3V$, $C_F = 56nF \pm 20\%$, $C_S = 0.1\mu F \pm 20\%$, $R_{FIL} = 20\Omega \pm 1\%$, $C_{FIL} = 0.22\mu F \pm 20$, $C_{IN} = 0.1\mu F \pm 20\%$, $R_L = 150\Omega$, $C_L = 0pF$, unless otherwise noted. **(Continued)**

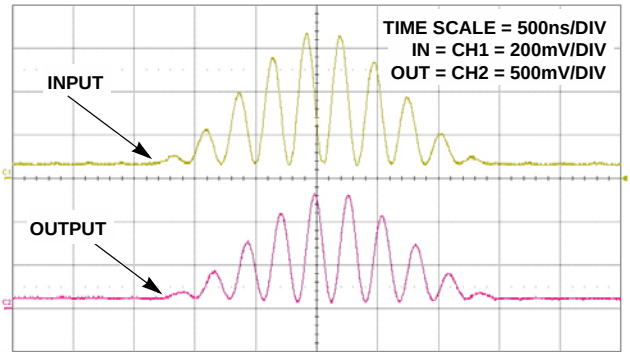


FIGURE 19. 12.5T RESPONSE

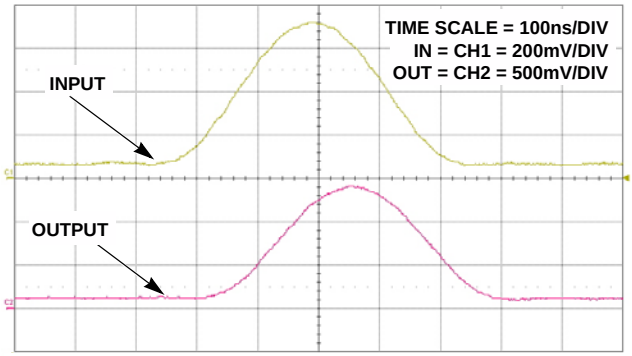


FIGURE 20. 2T RESPONSE

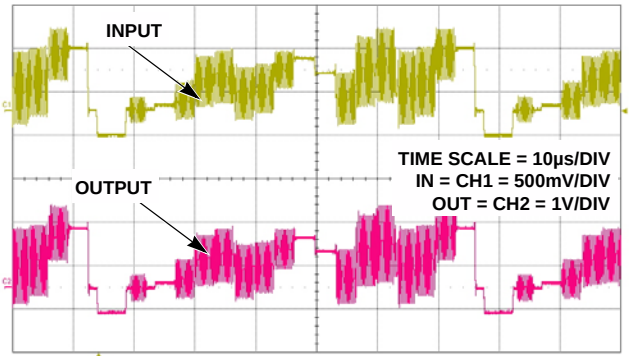


FIGURE 21. NTSC COLORBAR

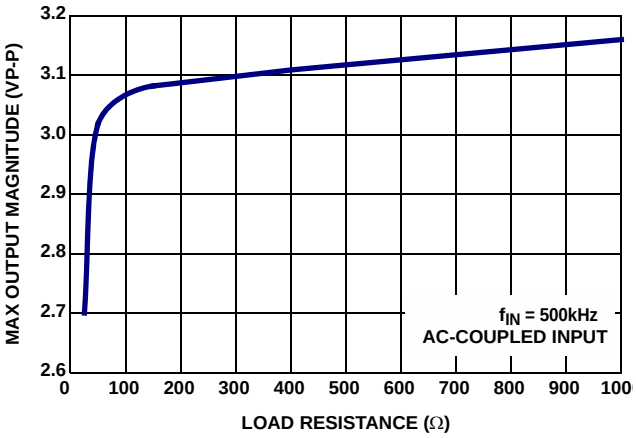


FIGURE 22. MAXIMUM OUTPUT MAGNITUDE vs LOAD RESISTANCE

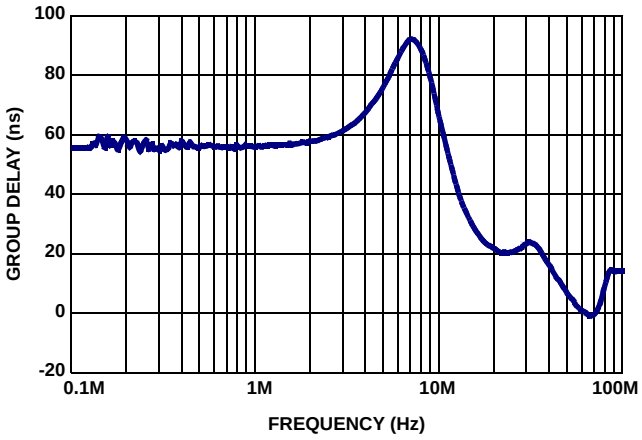


FIGURE 23. GROUP DELAY vs FREQUENCY

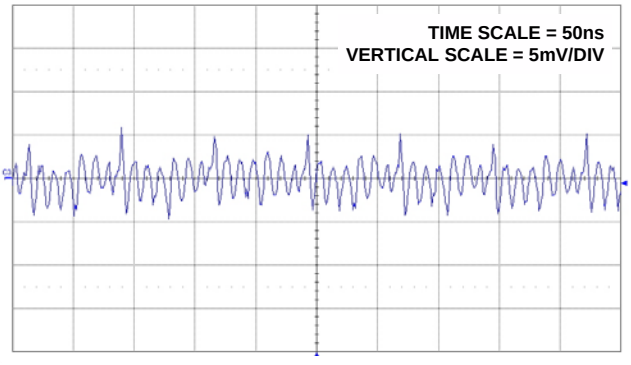


FIGURE 24. AMPLIFIER OUTPUT NOISE (CHARGE PUMP OSCILLATION)

Description of Operation and Application Information

Theory of Operation

The ISL59831 is a single supply video driver with a reconstruction filter and an on-board charge pump. It is designed to drive SDTV displays with luma (Y) or composite video (CV) signals. The input signal can be AC-coupled or DC-coupled. When AC-coupled, the sync tip clamp sets the blank level to ground at the output. The ISL59831 is capable of driving two AC-coupled or DC-coupled standard video loads and has a 4^{th} order Butterworth reconstruction filter with nominal -3dB frequency set to 9.1MHz, providing 44dB of attenuation at 27MHz. The ISL59831 is designed to operate with a single supply voltage range ranging from 3.0V to 3.6V. This eliminates the need for a split supply with the incorporation of a charge pump capable of generating a bottom rail as much as 1.9V below ground; providing a 5.2V range on a single 3.3V supply. This performance is ideal for NTSC video with negative-going sync pulses.

Output Amplifier

The ISL59831 output amplifier provides a gain of +6dB. The output amplifier is able to drive a $2.8V_{P-P}$ video signal into a 150Ω load to ground.

The output is a highly-stable, low distortion, low power, high frequency amplifier capable of driving moderate capacitive loads.

Input/Output Range

The ISL59831 has a recommended dynamic input range of $0V_{P-P}$ to $1.4V_{P-P}$. This allows the device to handle the maximum possible video signal input. As the input signal moves outside the specified range, the output signal will exhibit increasingly higher levels of harmonic distortion. As the load resistance becomes lower, the current drive capability of the device will be challenged and its ability to drive close to each rail is reduced.

The Charge Pump

The ISL59831 charge pump provides a bottom rail up to 1.9V below ground while operating on a 3.0V to 3.6V power supply. The charge pump is internally regulated and is driven by an internal 15MHz clock.

To reduce the noise on the power supply generated by the charge pump, connect a low pass RC-network between $CPVEE_{OUT}$ and VEE_{IN}. See “Block Diagram/Typical Application Circuit” on page 2 for further information.

The $CPVEE_{OUT}$ Pin

$CPVEE_{OUT}$ is the output pin for the charge pump. Keep in mind that the output of this pin is generated by the internal charge pump and a fully regulated supply that must be properly bypassed. Bypass this pin with a 0.1µF ceramic capacitor placed as close to the pin and connected to the ground plane of the board.

Video Performance

DIFFERENTIAL GAIN/PHASE

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency and phase response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω because of the change in output current with changing DC levels. Special circuitry has been incorporated into the ISL59831 for the reduction of output impedance variation with the current output. This results in outstanding differential gain and differential phase specifications of 0.04% and 0.35°, while driving 150Ω at a gain of +2V/V. Driving higher impedance loads would result in similar or better differential gain and differential phase performance.

NTSC

The ISL59831, generating a negative rail internally, is ideally suited for NTSC video with its accompanying negative-going sync signals.

Driving Capacitive Loads and Cables

The ISL59831, internally-compensated to drive 75Ω cables, will drive 220pF loads in parallel with 150Ω with less than 1.5dB of peaking.

AC-Coupled Inputs

SYNC TIP CLAMP

The ISL59831 features a sync tip clamp that sets the black level of the output video signal to ground. This ensures that the sync-tip voltage level is set to approximately -300mV at the back-termination resistor of a standard video load. The clamp is activated whenever the input voltage falls below 0V. The correction voltage required to do this is stored across the input AC-coupling capacitor. Refer to “Block Diagram/Typical Application Circuit” on page 2 for a detailed diagram.

DC-Coupled Inputs

When DC-coupling the inputs ensure that the lowest signal level is greater than +50mV to prevent the clamp from turning on and distorting the output. When DC-coupled the ISL59831 shifts the signal by -550mV from input to output.

Amplifier Disable

The ISL59831 can be disabled and its output placed in a high impedance state. The turn-off time is around 10ns and the turn-on time is around 30µs. The turn-on time is greater in length because extra time is given for the charge pump to settle before the amplifier is enabled. When disabled, the amplifier's supply current is reduced to 2µA typically, reducing power consumption. The amplifier's power-down can be controlled by standard TTL or CMOS signal levels at the ENABLE pin. The applied logic signal is relative to the GND pin. Applying a signal that is less than 0.8V above

GND will disable the amplifier. The amplifier will be enabled when the signal at ENABLE pin is 2V above GND.

Output Drive Capability

The maximum output current for the ISL59831 is set at ±50mA. Maximum reliability is maintained if the output current never exceeds ±50mA, after which the electro-migration limit of the process will be exceeded and the part will be damaged. This limit is set by the design of the internal metal interconnections.

Power Dissipation

With the high output drive capability of the ISL59831, it is possible to exceed the +150°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the amplifier in a safe operating area.

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}} \quad \text{(EQ. 1)}$$

Where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

Θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

for sourcing:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_S - V_{OUT}i) \times \frac{V_{OUT}i}{R_L i} \quad \text{(EQ. 2)}$$

for sinking:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_{OUT}i - V_S) \times I_{LOAD}i \quad \text{(EQ. 3)}$$

Where:

V_S = Supply voltage

I_{SMAX} = Maximum quiescent supply current

V_{OUT} = Maximum output voltage of the application

R_{LOAD} = Load resistance tied to ground

I_{LOAD} = Load current

i = Number of output channels

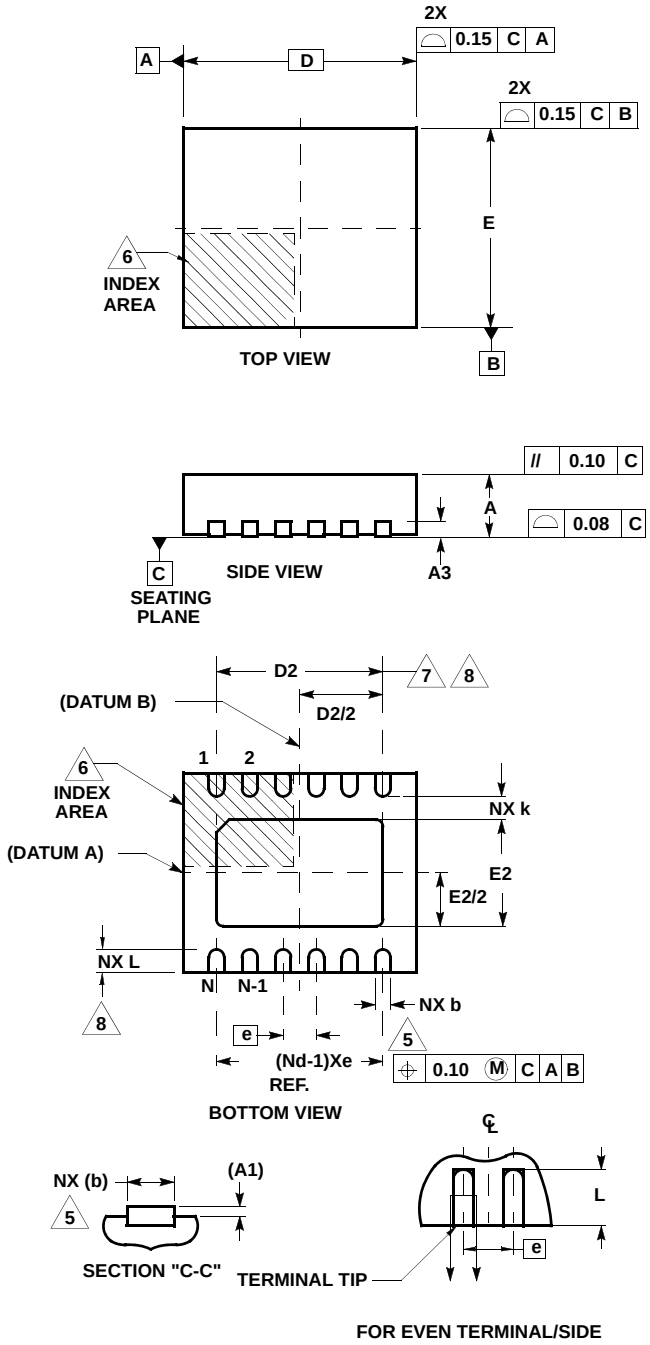
By setting the two P_{DMAX} equations equal to each other, we can solve the output current and R_{LOAD} to avoid the device overheat.

Power Supply Bypassing and Printed Circuit Board Layout

Strip line design techniques are recommended for the input and output signal traces. As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from V_{CC} and V_{CP} to GND will suffice.

For good AC performance, parasitic capacitance should be kept to a minimum. Use of wire-wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is also very important.

Thin Dual Flat No-Lead Plastic Package (TDFN)



L12.4x3A

12 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-229-WGED-4 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.18	0.23	0.30	5,8
D		4.00 BSC		-
D2	3.15	3.30	3.40	7,8
E		3.00 BSC		-
E2	1.55	1.70	1.80	7,8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		12		2
Nd		6		3

Rev. 0 1/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.