

TDA9910

12-bit, up to 80 Msample/s, Analog-to-Digital Converter (ADC)
direct/ultra high IF sampling

Rev. 04 — 12 June 2007

Product data sheet

1. General description

The TDA9910 is a 12-bit Analog-to-Digital Converter (ADC) optimized for direct Input Frequency (IF) sampling, and supporting the most demanding use conditions in ultra high IF radio transceivers for cellular infrastructure and other applications such as wireless access system, optical networking and fixed telecommunication. Thanks to its broadband input capabilities, the TDA9910 is ideal for single and multiple carriers data conversion.

Operating at a maximum sampling rate of 80 Msample/s, analog input signals are converted into 12-bit binary coded digital words. All static digital inputs are CMOS compatible. All output signals are LVCMOS compatible. The TDA9910 offers the most possible flexible acquisition control system thanks to its programmable Complete Conversion Signal (CCS) that allows to adjust the delay of the acquisition clock.

Thanks to its internal front-end buffer, the TDA9910 offers the lowest input capacitance (< 1 pF) and therefore the highest flexibility in front-end aliasing filter strategy.

2. Features

- 12-bit resolution
- 90 dB SFDR; 71 dB SNR ($f_i = 225$ MHz; $f_{CLK} = 80$ Msample/s; $B = 5$ MHz)
- High-speed sampling rate up to 80 Msample/s
- Programmable acquisition output clock (complete conversion signal)
- Single 5 V power supply
- Binary or two's-complement LVCMOS outputs
- Only 2 clock cycles latency
- HTQFP48 package
- Differential input with 375 MHz bandwidth
- 70 dB SFDR; 66.5 dB SNR ($f_i = 175$ MHz; $f_{CLK} = 80$ Msample/s; $B = \text{Nyquist}$)
- Internal front-end buffer (input capacitance < 1 pF)
- Full-scale controllable from 1.5 V to 2 V (p-p); continuous scale
- 3.3 V LVCMOS compatible digital outputs
- CMOS compatible static digital inputs
- Industrial temperature range from -40 °C to $+85$ °C

3. Applications

- 2.5G and 3G cellular base infrastructure radio transceivers
- Wireless access systems
- Fixed telecommunication
- Optical networking
- Wireless Local Area Network (WLAN) infrastructure

4. Ordering information

Table 1. Ordering information

Type number	Sampling frequency (Msample/s)	Package		Version
		Name	Description	
TDA9910HW/8/C1	80	HTQFP48	plastic thermal enhanced thin quad flat package; 48 leads; body 7 × 7 × 1 mm; exposed die pad	SOT545-2

5. Block diagram

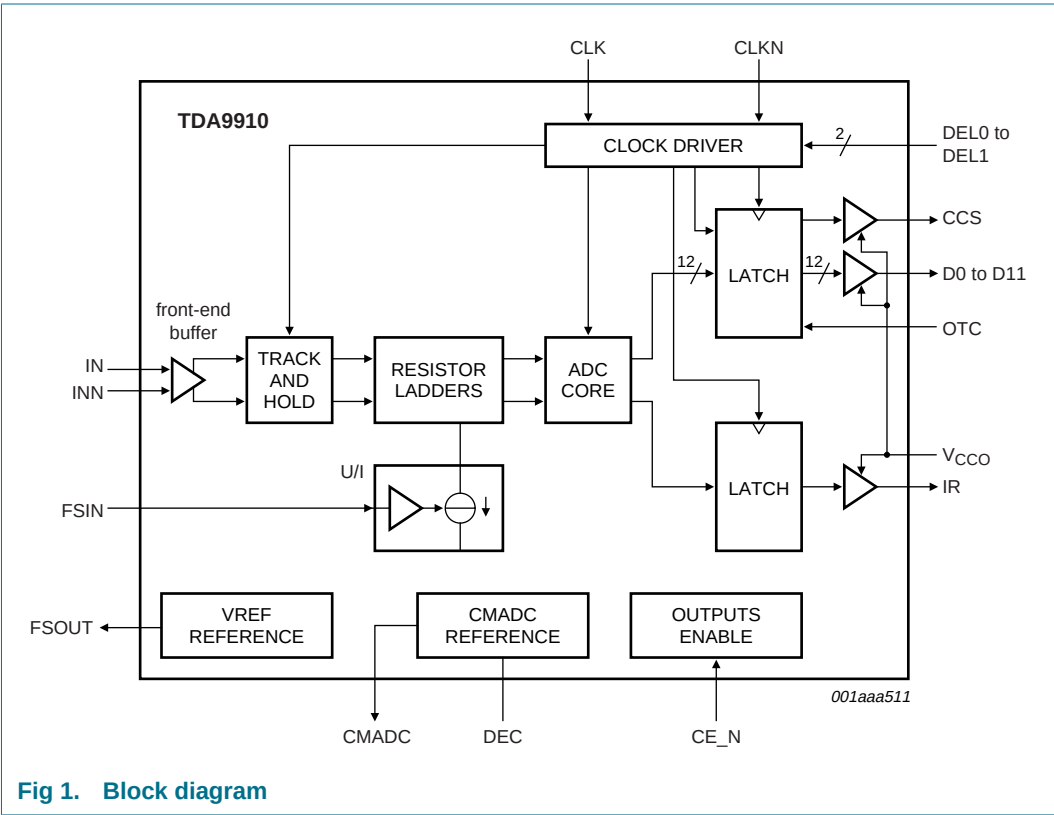
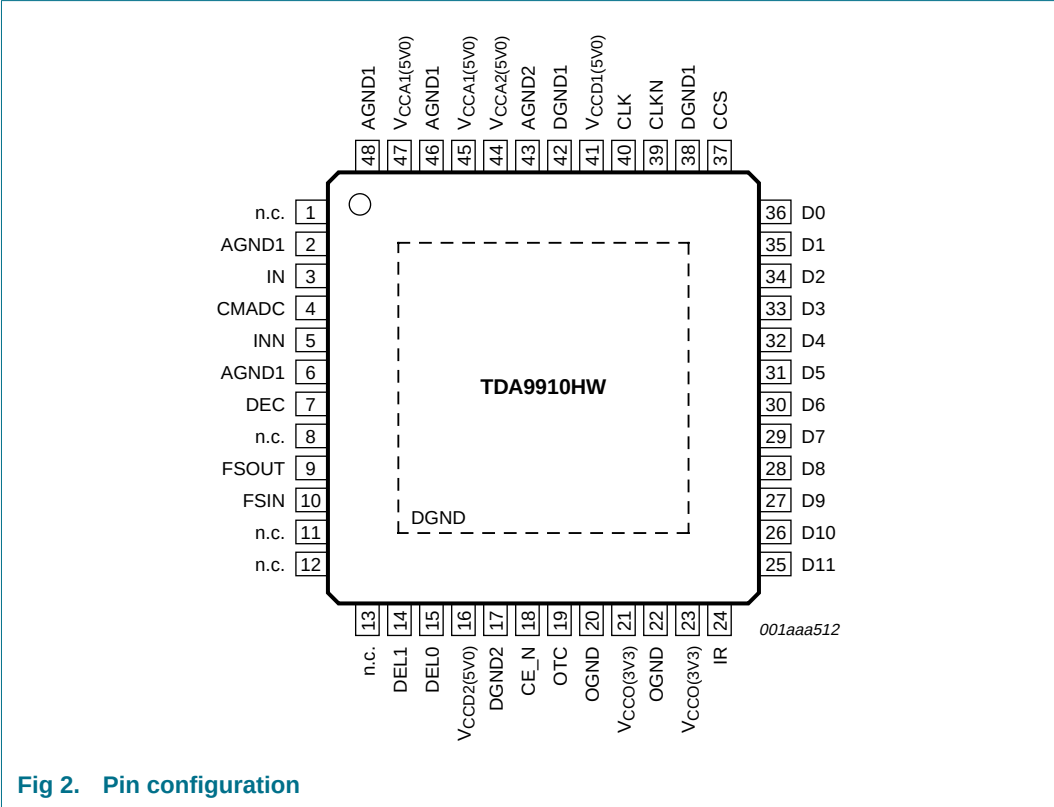


Fig 1. Block diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description			
Symbol	Pin	Type [1]	Description
n.c.	1	-	not connected
AGND1	2	G	analog ground 1
IN	3	I	analog input voltage
CMADC	4	O	regulator common mode ADC output
INN	5	I	complementary analog input voltage
AGND1	6	G	analog ground 1
DEC	7	I/O	decoupling node
n.c.	8	-	not connected
FSOUT	9	O	full-scale reference voltage output
FSIN	10	I	full-scale reference voltage input
n.c.	11	-	not connected
n.c.	12	-	not connected
n.c.	13	-	not connected
DEL1	14	I	complete conversion signal delay input 1

Table 2. Pin description ...continued

Symbol	Pin	Type [1]	Description
DEL0	15	I	complete conversion signal delay input 0
V _{CCD2(5V0)}	16	P	digital supply voltage 2 (5.0 V)
DGND2	17	G	digital ground 2
CE_N	18	I	chip enable input (CMOS level; active LOW)
OTC	19	I	control input for two's complement output (active HIGH)
OGND	20	G	data output ground
V _{CCO(3V3)}	21	P	data output supply voltage (3.3 V)
OGND	22	G	data output ground
V _{CCO(3V3)}	23	P	data output supply voltage (3.3 V)
IR	24	O	in-range output
D11	25	O	data output bit 11 (MSB)
D10	26	O	data output bit 10
D9	27	O	data output bit 9
D8	28	O	data output bit 8
D7	29	O	data output bit 7
D6	30	O	data output bit 6
D5	31	O	data output bit 5
D4	32	O	data output bit 4
D3	33	O	data output bit 3
D2	34	O	data output bit 2
D1	35	O	data output bit 1
D0	36	O	data output bit 0 (LSB)
CCS	37	O	complete conversion signal output
DGND1	38	G	digital ground 1
CLKN	39	I	complementary clock input
CLK	40	I	clock input
V _{CCD1(5V0)}	41	P	digital supply voltage 1 (5.0 V)
DGND1	42	G	digital ground 1
AGND2	43	G	analog ground 2
V _{CCA2(5V0)}	44	P	analog supply voltage 2 (5.0 V)
V _{CCA1(5V0)}	45	P	analog supply voltage 1 (5.0 V)
AGND1	46	G	analog ground 1
V _{CCA1(5V0)}	47	P	analog supply voltage 1 (5.0 V)
AGND1	48	G	analog ground 1
DGND	exposed die pad	G	digital ground

[1] P: power supply; G: ground; I: input; O: output.

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCA}	analog supply voltage	[1]	-0.5	+7.0	V
V_{CCD}	digital supply voltage	[1]	-0.5	+7.0	V
V_{CCO}	output supply voltage	[2]	-0.5	+5.0	V
ΔV_{CC}	supply voltage difference				
	$V_{CCA} - V_{CCD}$		-1.0	+1.0	V
	$V_{CCD} - V_{CCO}$		-1.0	+4.0	V
	$V_{CCA} - V_{CCO}$		-1.0	+4.0	V
$V_{I(IN)}, V_{I(INN)}$	input voltage	referenced to AGND	0	$V_{CCA} + 1$	V
V_{CLK}, V_{CLKN}	input voltage for differential clock drive	referenced to DGND	0	$V_{CCD} + 1$	V
I_O	output current		-	10	mA
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
T_j	junction temperature		-	150	°C

[1] The supply voltages V_{CCA} and V_{CCD} may have any value between -0.5 V and +7.0 V provided that the supply voltage differences ΔV_{CC} are respected.

[2] The supply voltage V_{CCO} may have any value between -0.5 V and +5.0 V provided that the supply voltage differences ΔV_{CC} are respected.

8. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	36.2	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	[1]	14.3	K/W

[1] In compliance with JEDEC test board, in free air.

9. Characteristics

Table 5. Characteristics

$V_{CCA} = 4.75\text{ V to }5.25\text{ V}$; $V_{CCD} = 4.75\text{ V to }5.25\text{ V}$; $V_{CCO} = 2.7\text{ V to }3.6\text{ V}$; AGND and DGND shorted together; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; $V_{i(IN)} - V_{i(INN)} = -0.5\text{ dBFS}$; $V_{FSIN} = V_{CCA} - 1.87\text{ V}$; $V_{i(CM)} = V_{CCA} - 1.95\text{ V}$; typical values measured at $V_{CCA} = V_{CCD} = 5\text{ V}$, $V_{CCO} = 3.3\text{ V}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$ and $C_L = 10\text{ pF}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output supply voltage		2.7	3.3	3.6	V
I_{CCA}	analog supply current		-	120	135	mA
I_{CCD}	digital supply current		-	50	65	mA
I_{CCO}	output supply current	$f_{CLK} = 80\text{ Msample/s}$; $f_i = 93\text{ MHz}$	-	10	15	mA
P_{tot}	total power dissipation	$f_{CLK} = 80\text{ Msample/s}$; DC input	-	840	990	mW
Clock inputs: pins CLK and CLKN^[2]						
V_{IL}	LOW-level input voltage	referenced to DGND; $V_{CCD} = 5\text{ V}$				
		PECL mode	3.19	-	3.52	V
		TTL mode	DGND	-	0.8	V
V_{IH}	HIGH-level input voltage	referenced to DGND; $V_{CCD} = 5\text{ V}$				
		PECL mode	3.83	-	4.12	V
		TTL mode	2.0	-	V_{CCD}	V
I_{IL}	LOW-level input current	V_{CLK} or $V_{CLKN} = 3.52\text{ V}$	^[1] -	-	28	μA
		V_{CLK} or $V_{CLKN} = 0.80\text{ V}$	1	-	-	nA
I_{IH}	HIGH-level input current	V_{CLK} or $V_{CLKN} = 3.83\text{ V}$	-	-	30	μA
		V_{CLK} or $V_{CLKN} = 2.00\text{ V}$	2	-	-	nA
ΔV_{CLK}	differential AC input voltage for switching ($V_{CLK} - V_{CLKN}$)	AC mode; DC voltage level is 2.5 V	1.3	1.5	1.7	V
R_i	input resistance	$f_{CLK} = 80\text{ Msample/s}$	^[1] -	6.3	-	k Ω
C_i	input capacitance	$f_{CLK} = 80\text{ Msample/s}$	^[1] -	1.1	-	pF

Analog inputs: pins IN and INN

I_{IL}	LOW-level input current	$V_{FSIN} = V_{CCA} - 1.75\text{ V}$	-	5	-	μA
I_{IH}	HIGH-level input current	$V_{FSIN} = V_{CCA} - 1.75\text{ V}$	-	5	-	μA
R_i	input resistance		^[1] 6.3	-	-	M Ω
C_i	input capacitance		^[1] -	-	700	fF
$V_{i(CM)}$	common mode input voltage	$V_{i(IN)} = V_{i(INN)}$; output code = 2047	$V_{CCA} - 2$	$V_{CCA} - 1.8$	$V_{CCA} - 1.6$	V

Table 5. Characteristics ...continued

$V_{CCA} = 4.75\text{ V to }5.25\text{ V}$; $V_{CCD} = 4.75\text{ V to }5.25\text{ V}$; $V_{CCO} = 2.7\text{ V to }3.6\text{ V}$; AGND and DGND shorted together; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; $V_{i(IN)} - V_{i(INN)} = -0.5\text{ dBFS}$; $V_{FSIN} = V_{CCA} - 1.87\text{ V}$; $V_{i(CM)} = V_{CCA} - 1.95\text{ V}$; typical values measured at $V_{CCA} = V_{CCD} = 5\text{ V}$, $V_{CCO} = 3.3\text{ V}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$ and $C_L = 10\text{ pF}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital inputs: pins OTC and CE_N						
V _{IL}	LOW-level input voltage		DGND	-	0.3 × V _{CCD}	V
V _{IH}	HIGH-level input voltage		0.7 × V _{CCD}	-	V _{CCD}	V
I _{IL}	LOW-level input current	V _{IL} = 0.8 V	-	1	-	μA
I _{IH}	HIGH-level input current	V _{IH} = 2.0 V	-	1	-	μA
Digital inputs: pins DEL0 and DEL1						
V _{IL}	LOW-level input voltage		DGND	-	0.3 × V _{CCD}	V
V _{IH}	HIGH-level input voltage		0.7 × V _{CCD}	-	V _{CCD}	V
I _{IL}	LOW-level input current	V _{IL} = 0.8 V	-	8	-	μA
I _{IH}	HIGH-level input current	V _{IH} = 2.0 V	-	20	-	μA
Voltage controlled regulator output: pin CMADC						
V _{o(CM)}	common mode output voltage	I _L = 0 mA	-	V _{CCA} – 1.88	-	V
		I _L = 2 mA	-	V _{CCA} – 1.95	-	V
Reference voltage input: pin FSIN ^[3]						
V _{FSIN}	full-scale fixed voltage		-	V _{CCA} – 1.80	-	V
I _{FSIN}	input current		-	0.1	-	μA
V _{i(p-p)}	peak-to-peak input voltage	see Figure 5; V _i = V _{i(IN)} – V _{i(INN)} ; V _{i(CM)} = V _{CCA} – 1.95 V	-	1.85	-	V
Full-scale voltage controlled regulator output: pin FSOUT						
V _{o(ref)}	1.9 V full-scale output voltage	I _L = I _{FSIN}	-	V _{CCA} – 1.80	-	V
		I _L = 2 mA	-	V _{CCA} – 1.82	-	V
Digital outputs: pins D11 to D0, IR and CCS						
Output levels						
V _{OL}	LOW-level output voltage	I _{OL} = 2 mA	DGND	-	DGND + 0.5	V
V _{OH}	HIGH-level output voltage	I _{OH} = –0.4 mA	V _{CCO} – 0.5	-	V _{CCO}	V
I _{OZ}	output current in 3-state	output level between 0.5 V and V _{CCO}	–0.1	0	+0.1	μA
Timing ^[4]						
t _{d(s)}	sampling delay time	C _L = 10 pF	-	0.1	0.24	ns
t _{h(o)}	output hold time	C _L = 10 pF	2.6	3.8	-	ns
t _{d(o)}	output delay time	C _L = 10 pF	-	4.7	7.8	ns
3-state output delay						
t _{dZH}	enable HIGH		-	3.6	-	ns
t _{dZL}	enable LOW		-	3.9	-	ns
t _{dHZ}	disable HIGH		-	9.2	-	ns
t _{dLZ}	disable LOW		-	7.2	-	ns

Table 5. Characteristics ...continued

$V_{CCA} = 4.75\text{ V to }5.25\text{ V}$; $V_{CCD} = 4.75\text{ V to }5.25\text{ V}$; $V_{CCO} = 2.7\text{ V to }3.6\text{ V}$; AGND and DGND shorted together; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; $V_{i(IN)} - V_{i(INN)} = -0.5\text{ dBFS}$; $V_{FSIN} = V_{CCA} - 1.87\text{ V}$; $V_{i(CM)} = V_{CCA} - 1.95\text{ V}$; typical values measured at $V_{CCA} = V_{CCD} = 5\text{ V}$, $V_{CCO} = 3.3\text{ V}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$ and $C_L = 10\text{ pF}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock timing inputs: pins CLK and CLKN						
δ	duty cycle	$f_{\text{CLK}} = 80 \text{ Msample/s};$ $f_i = 175 \text{ MHz}$	45	-	55	%
$f_{\text{CLK}(\text{min})}$	minimum clock frequency		-	-	9.5	Msample/s
$f_{\text{CLK}(\text{max})}$	maximum clock frequency	$\delta = 45 \text{ \% to } 55 \text{ \%}$	80	-	-	Msample/s
Timing complete conversion signal: pin CCS; see Figure 6						
$t_{\text{cd}(\text{o})}$	complete conversion signal delay time	$C_L = 10 \text{ pF};$ DEL0 = LOW; DEL1 = HIGH	-	0.3	-	ns
		$C_L = 10 \text{ pF};$ DEL0 = HIGH; DEL1 = LOW	-	1.3	-	ns
		$C_L = 10 \text{ pF};$ DEL0 = HIGH; DEL1 = HIGH	-	2.3	-	ns
Analog signal processing (clock duty cycle 50 %)						
INL	integral non-linearity	$f_{\text{CLK}} = 20 \text{ Msample/s};$ $f_i = 21.4 \text{ MHz}$	-	± 2.0	-	LSB
DNL	differential non-linearity	$f_{\text{CLK}} = 20 \text{ Msample/s};$ $f_i = 21.4 \text{ MHz};$ no missing code guaranteed	-	± 0.6	-	LSB
E_{offset}	offset error	$V_{\text{CCA}} = V_{\text{CCD}} = 5 \text{ V};$ $V_{\text{CCO}} = 3.3 \text{ V};$ $T_{\text{amb}} = 25 \text{ }^\circ\text{C};$ output code = 2047	-4	+8	+24	mV
E_G	gain error amplitude (spread from device to device)	$V_{\text{CCA}} = V_{\text{CCD}} = 5 \text{ V};$ $V_{\text{CCO}} = 3.3 \text{ V};$ $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	2.5	-	%FS
B	analog bandwidth ^[5]	$f_{\text{CLK}} = 80 \text{ Msample/s};$ -3 dB; full-scale input	320	375	-	MHz
$\alpha_{2\text{H}}$	second harmonic level	$f_i = 21.4 \text{ MHz}$	-	-79	-	dBc
		$f_i = 93 \text{ MHz}$	-	-78	-	dBc
		$f_i = 175 \text{ MHz}$	-	-74	-	dBc
$\alpha_{3\text{H}}$	third harmonic level	$f_i = 21.4 \text{ MHz}$	-	-84	-	dBc
		$f_i = 93 \text{ MHz}$	-	-80	-	dBc
		$f_i = 175 \text{ MHz}$	-	-76	-	dBc
THD	total harmonic distortion ^[6]	$f_i = 21.4 \text{ MHz}$	-	-75	-	dBc
		$f_i = 93 \text{ MHz}$	-	-73	-	dBc
		$f_i = 175 \text{ MHz}$	-	-68	-	dBc
$N_{\text{th}(\text{RMS})}$	RMS thermal noise	$V_{i(\text{IN})} = V_{i(\text{INN})};$ $f_{\text{CLK}} = 80 \text{ Msample/s}$	-	0.45	-	LSB

Table 5. Characteristics ...continued

$V_{CCA} = 4.75\text{ V to }5.25\text{ V}$; $V_{CCD} = 4.75\text{ V to }5.25\text{ V}$; $V_{CCO} = 2.7\text{ V to }3.6\text{ V}$; AGND and DGND shorted together; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; $V_{i(IN)} - V_{i(INN)} = -0.5\text{ dBFS}$; $V_{FSIN} = V_{CCA} - 1.87\text{ V}$; $V_{i(CM)} = V_{CCA} - 1.95\text{ V}$; typical values measured at $V_{CCA} = V_{CCD} = 5\text{ V}$, $V_{CCO} = 3.3\text{ V}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$ and $C_L = 10\text{ pF}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SNR	signal-to-noise ratio ^[7]	$f_i = 21.4\text{ MHz}$	-	67.4	-	dBc
		$f_i = 93\text{ MHz}$	63	67.2	-	dBc
		$f_i = 175\text{ MHz}$	-	66.5	-	dBc
SFDR	spurious free dynamic range	$f_i = 21.4\text{ MHz}$	-	76	-	dBc
		$f_i = 93\text{ MHz}$	68	78	-	dBc
		$f_i = 175\text{ MHz}$	-	74	-	dBc
ACPR	adjacent channel power rejection	$f_i = 93\text{ MHz}$; 5 MHz channel spacing; $B = 3.84\text{ MHz}$	-	70	-	dB
$d2_{(IM2)}$	second order intermodulation distortion ^[8]	$f_{i1} = 21\text{ MHz}$; $f_{i2} = 22\text{ MHz}$	-	-89	-	dBFS
		$f_{i1} = 91.5\text{ MHz}$; $f_{i2} = 94.5\text{ MHz}$	-	-86	-	dBFS
		$f_{i1} = 174\text{ MHz}$; $f_{i2} = 176\text{ MHz}$	-	-83	-	dBFS
$d3_{(IM3)}$	third order intermodulation distortion ^[8]	$f_{i1} = 21\text{ MHz}$; $f_{i2} = 22\text{ MHz}$	-	-88	-	dBFS
		$f_{i1} = 91.5\text{ MHz}$; $f_{i2} = 93.5\text{ MHz}$	-	-82	-	dBFS
		$f_{i1} = 174\text{ MHz}$; $f_{i2} = 176\text{ MHz}$	-	-83	-	dBFS

- [1] Guaranteed by design.
- [2] The circuit has two clock inputs: CLK and CLKN. There are 5 modes of operation:
- PECL mode 1: (DC levels vary 1:1 with V_{CCD}) CLK and CLKN inputs are at differential PECL levels.
 - PECL mode 2: (DC levels vary 1:1 with V_{CCD}) CLK input is at PECL level and sampling is taken on the falling edge of the clock input signal. A DC level of 3.65 V has to be applied on CLKN decoupled to GND via a 100 nF capacitor.
 - PECL mode 3: (DC levels vary 1:1 with V_{CCD}) CLKN input is at PECL level and sampling is taken on the rising edge of the clock input signal. A DC level of 3.65 V has to be applied on CLK decoupled to GND via a 100 nF capacitor.
 - Differential AC driving mode 4: When driving the CLK input directly and with any AC signal of minimum 1 V (p-p) and with a DC level of 2.5 V, the sampling takes place at the falling edge of the clock signal.
When driving the CLKN input with the same signal, sampling takes place at the rising edge of the clock signal. It is recommended to decouple the CLKN or CLK input to DGND via a 100 nF capacitor.
 - TTL mode 5: CLK input is at TTL level and sampling is taken on the falling edge of the clock input signal.
In that case CLKN pin has to be connected to the ground.
- [3] The ADC input range can be adjusted with an external reference connected to FSIN pin. This voltage has to be referenced to V_{CCA} .
- [4] Output data acquisition: the output data is available after the maximum delay of $t_{d(O)}$.
- [5] The -3 dB analog bandwidth is determined by the 3 dB reduction in the reconstructed output, the input being a full-scale sine wave.
- [6] The total harmonic distortion is obtained with the addition of the first five harmonics.
- [7] The signal-to-noise ratio takes into account all harmonics above five and noise up to Nyquist frequency.
- [8] Intermodulation measured relative to either tone with analog input frequencies f_{i1} and f_{i2} . The two input signals have the same amplitude and the total amplitude of both signals provides full-scale to the converter (-6 dB below full-scale for each input signal). $d3_{(IM3)}$ is the ratio of the RMS value of either input tone to the RMS value of the worst case third order intermodulation product; $d2_{(IM2)}$ is the ratio of the RMS value of either input tone to the RMS value of the worst case second order intermodulation product.

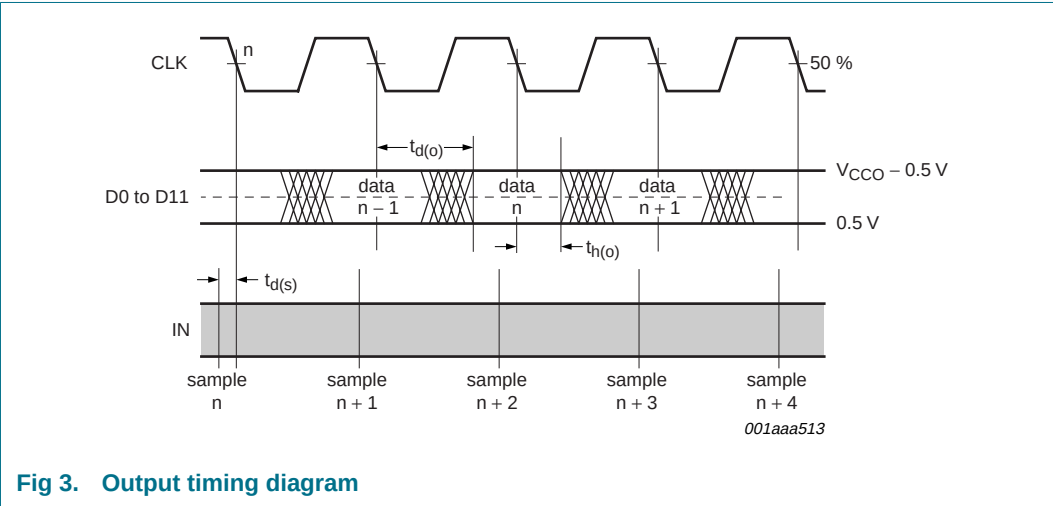
Table 6. Output coding with differential inputs
 $V_{i(IN)} - V_{i(INN)} = 1.9\text{ V}$; $V_{FSIN} = V_{CCA1} - 1.87\text{ V}$; typical values to AGND.

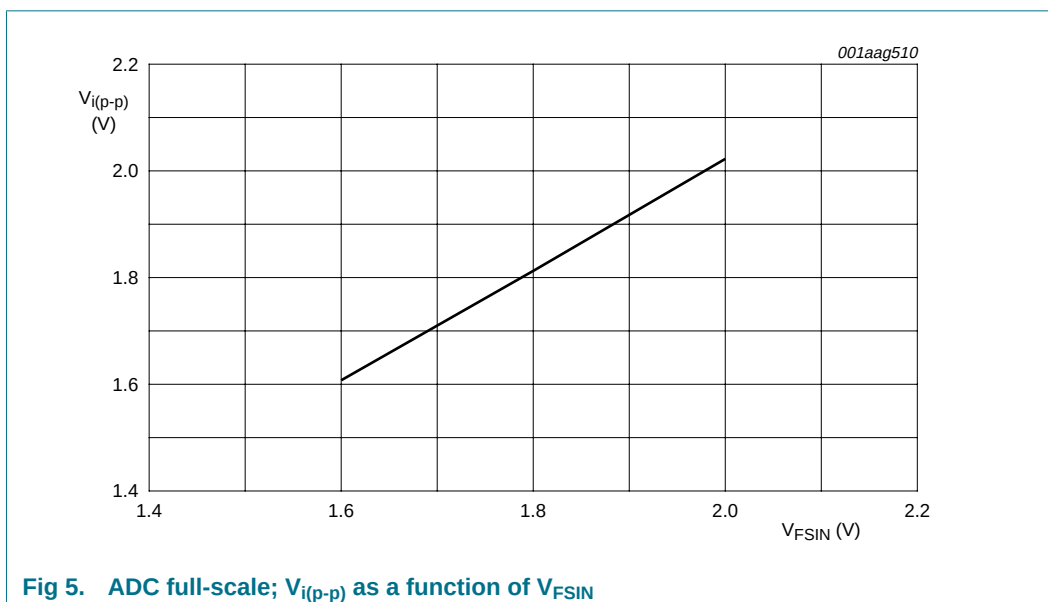
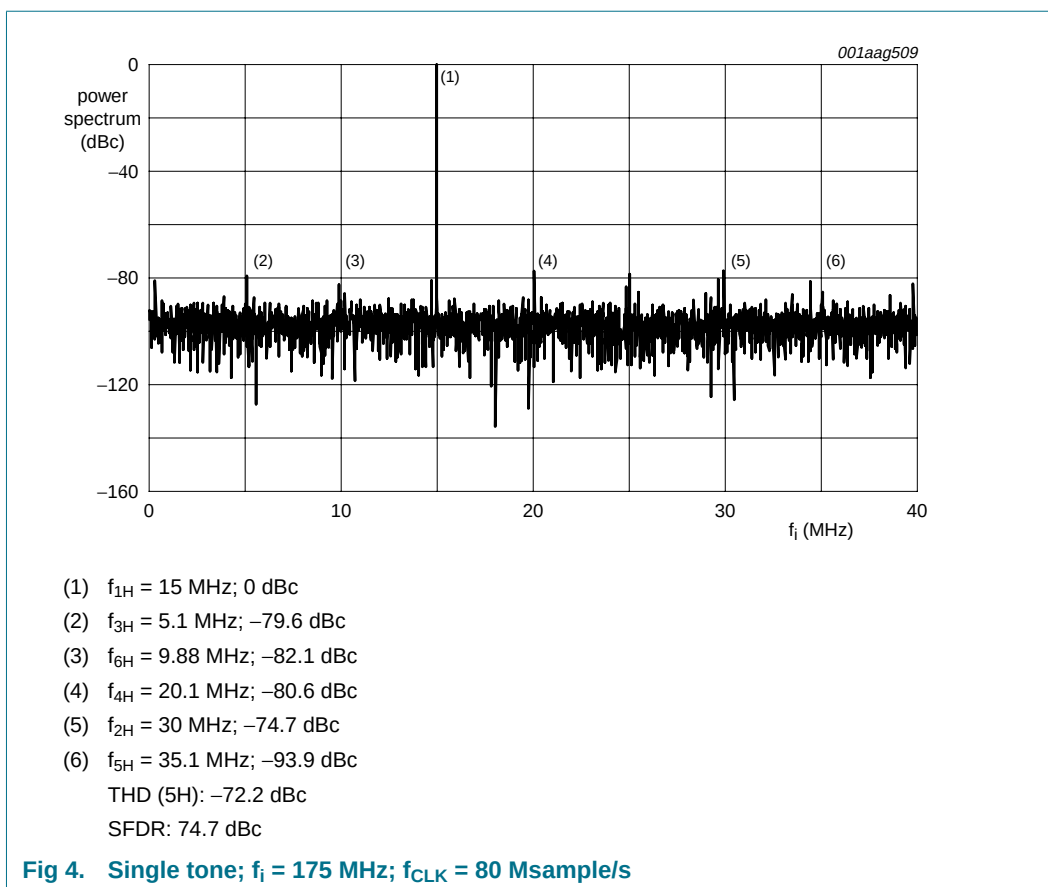
Code	$V_{i(IN)}\text{ (V)}$	$V_{i(INN)}\text{ (V)}$	IR	Binary outputs (D11 to D0)	Two's complement outputs (D11 to D0)
Underflow	< 2.675	> 3.625	0	0000 0000 0000	1000 0000 0000
0	2.675	3.625	1	0000 0000 0000	1000 0000 0000
1	-	-	1	0000 0000 0001	1000 0000 0001
...	...	...	...	...	...
2047	3.15	3.15	1	0111 1111 1111	1111 1111 1111
...	...	...	...	...	...
4094	-	-	1	1111 1111 1110	0111 1111 1110
4095	3.625	2.675	1	1111 1111 1111	0111 1111 1111
Overflow	> 3.625	< 2.675	0	1111 1111 1111	0111 1111 1111

Table 7. Mode selection

Two's complement output (OTC)	Chip enable input (CE_N)	Data output (D0 to D11; IR)
0	0	binary; active
1	0	two's complement; active
X ^[1]	1	high-impedance

[1] X = don't care.



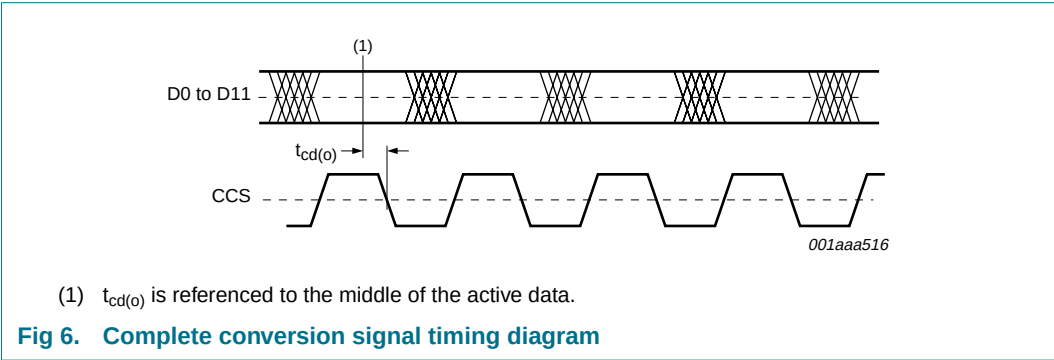


The TDA9910 allows to modify the ADC full-scale. This could be done with FSIN (full-scale input) according to [Figure 5](#).

The TDA9910 generates an adjustable clock output called Complete Conversion Signal (CCS), which can be used to control the acquisition of converted output data by the digital circuit connected to the TDA9910 output data bus. Two logic inputs, DEL0 and DEL1 pins, allow to adjust the delay of the edge of the CCS signal to achieve an optimal position in the stable, usable zone of the data.

Table 8. Complete conversion signal selection

DEL1	DEL0	CCS output
0	0	high-impedance
0	1	active, typical delay 0.3 ns
1	0	active, typical delay 1.3 ns
1	1	active, typical delay 2.3 ns



10. Definitions

10.1 Static parameters

10.1.1 INL (integral non-linearity)

It is defined as the deviation of the transfer function from a best fit straight line (linear regression computation). The INL of the code i is obtained from the equation:

$$INL(i) = \frac{V_{in}(i) - V_{in}(ideal)}{S}$$

where: S is corresponding to the slope of the ideal straight line (code width); i is corresponding to the code value; V_{in} is the input voltage.

10.1.2 DNL (differential non-linearity)

It is the deviation in code width from the value of 1 LSB.

$$DNL(i) = \frac{V_{in}(i+1) - V_{in}(i)}{S}$$

where: V_{in} is the input voltage; i from 0 to $(2^n - 2)$.

10.2 Dynamic parameters

[Figure 7](#) shows the spectrum of a single tone full-scale input sine wave with frequency f_t , conforming to coherent sampling ($f_t/f_s = M/N$, with M number of cycles and N number of samples, M and N being relatively prime), and digitized by the ADC under test.

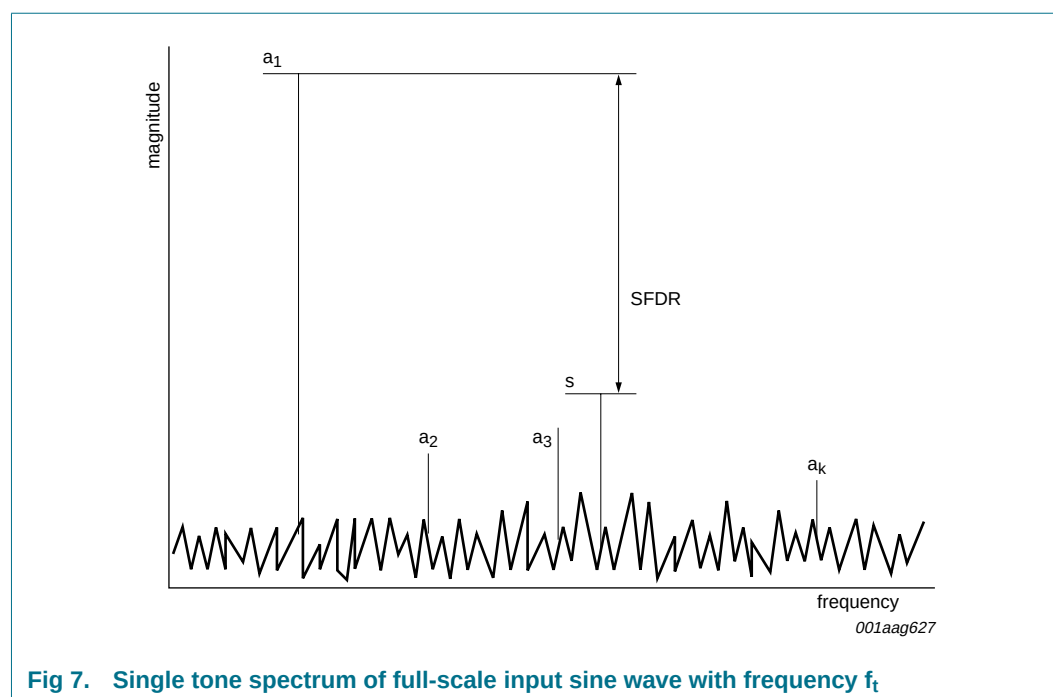


Fig 7. Single tone spectrum of full-scale input sine wave with frequency f_t

Remark: In the following equations, P_{noise} is the power of the terms which include the effects of random noise, non-linearities, sampling time errors, and 'quantization noise'.

10.2.1 SINAD (signal-to-noise and distortion)

The ratio of the output signal power to the noise plus distortion power for a given sample rate and input frequency, excluding the DC component:

$$\text{SINAD}[\text{dB}] = 10 \log_{10} \left(\frac{P_{\text{signal}}}{P_{\text{noise} + \text{distortion}}} \right)$$

10.2.2 ENOB (effective number of bits)

It is derived from SINAD and gives the theoretical resolution an ideal ADC would require to obtain the same SINAD measured on the real ADC. A good approximation gives:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02}$$

10.2.3 THD (total harmonic distortion)

The ratio of the power of the harmonics to the power of the fundamental. For $k - 1$ harmonics the THD is:

$$\text{THD}[\text{dB}] = 10 \log_{10} \left(\frac{P_{\text{harmonics}}}{P_{\text{signal}}} \right)$$

where:

$$P_{\text{harmonics}} = a_2^2 + a_3^2 + \dots + a_k^2$$

$$P_{\text{signal}} = a_1^2$$

The value of k is usually 6 (i.e. calculation of THD is done on the first 5 harmonics).

10.2.4 SNR (signal-to-noise ratio)

The ratio of the output signal power to the noise power, excluding the harmonics and the DC component is:

$$\text{SNR}[\text{dB}] = 10 \log_{10} \left(\frac{P_{\text{signal}}}{P_{\text{noise}}} \right)$$

10.2.5 SFDR (spurious free dynamic range)

The number SFDR specifies available signal range as the spectral distance between the amplitude of the fundamental and the amplitude of the largest spurious harmonic and non-harmonic, excluding DC component:

$$\text{SFDR}[\text{dB}] = 20 \log_{10} \left(\frac{a_1}{\max(S)} \right)$$

10.2.6 IMD2 (IMD3)

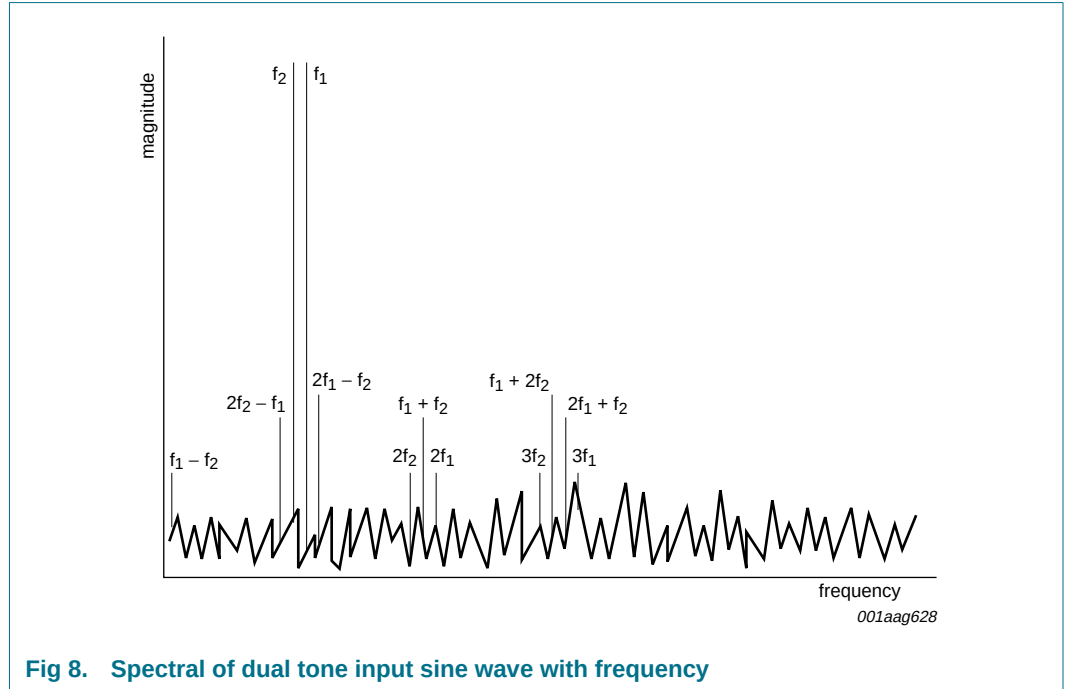


Fig 8. Spectral of dual tone input sine wave with frequency

From a dual tone input sinusoid (f_{t1} and f_{t2} , these frequencies being chosen according to the coherence criterion), the intermodulation distortion products IMD2 and IMD3 (respectively, 2nd and 3rd order components) are defined, as follows.

The ratio of the RMS value of either tone to the RMS value of the worst second (third) order intermodulation product.

The total InterModulation Distortion (IMD) is given by:

$$IMD[dB] = 10 \log_{10} \left(\frac{P_{intermod}}{P_{signal}} \right)$$

where:

$$P_{intermod} = a_{im(f_{t1} - f_{t2})}^2 + a_{im(f_{t1} + f_{t2})}^2 + a_{im(f_{t1} - 2f_{t2})}^2 + a_{im(f_{t1} + 2f_{t2})}^2 + \dots \\ \dots + a_{im(2f_{t1} - f_{t2})}^2 + a_{im(2f_{t1} + f_{t2})}^2$$

with $a_{im(f_{t1})}^2$ corresponding to the power in the intermodulation component at frequency f_t .

$$P_{signal} = a_{f_{t1}}^2 + a_{f_{t2}}^2$$

11. Application information

11.1 TDA9910 in 3G radio receivers

The TDA9910 has been proven in many 3G radio receivers with various operating conditions regarding Input Frequency (IF), signal IF bandwidth and sampling frequency. The TDA9910 provides with a maximum analog input signal frequency of 400 MHz. It allows a significant cost-down of the RF front-end, from two mixers to only one, even in multi-carriers architecture.

[Table 9](#) describes some possible applications with the TDA9910 in high IF sampling mode.

Table 9. Examples of possible f_i , f_{CLK} , IF BW combinations supported

f_i (MHz)	f_{CLK} (Msample/s)	IF BW (MHz) ^[1]	SNR (dB)	SFDR (dBc)
350	80	5.00	65	71
243.95	9.60	0.25	71	80
96	76.80	1.60	72	76
96	76.80	4.80	71	77
96	76.80	20.00	68	76
80	61.44	10.00	70	85
78.4	44.80	3.50	71	76
70	40.00	1.25	72	79

[1] IF bandwidth corresponds to the observed area on the ADC output spectrum.

For a dual carrier W-CDMA receiver, the most important parameters are sensitivity and Adjacent Channel Selectivity (ACS). The sensitivity is defined as the lowest detectable signal level. In W-CDMA, it can be far below the noise floor. This difference, between the sensitivity and the noise floor, is defined by the Sensitivity-to-Noise Ratio (SENr). Its value is negative due to the gain processing. The Adjacent Channel Power Ratio (ACPR) is the difference between the full-scale -3 dB peak and the noise floor. It represents the ratio of the adjacent-channel power and the average power level of the channel. The ACS is defined by the sum of SENr and ACPR.

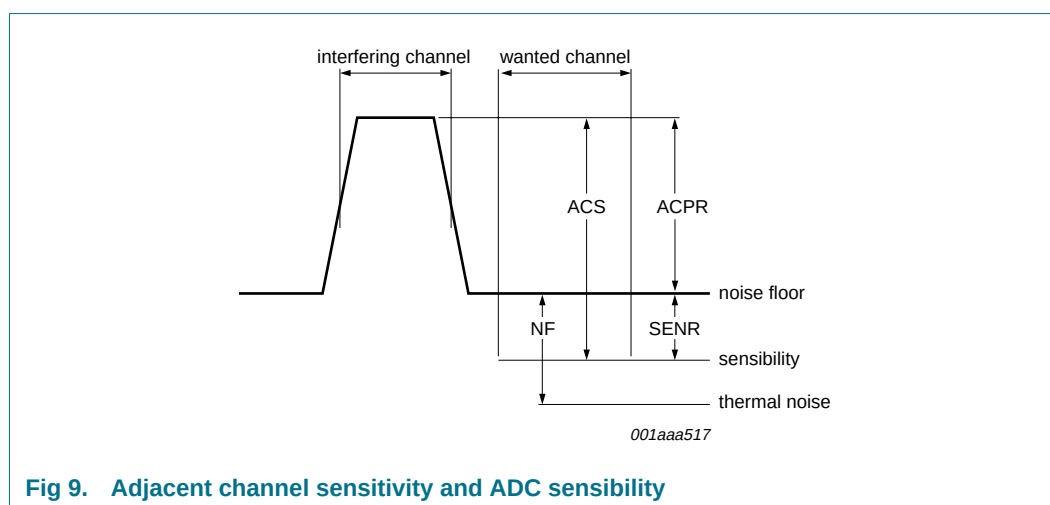
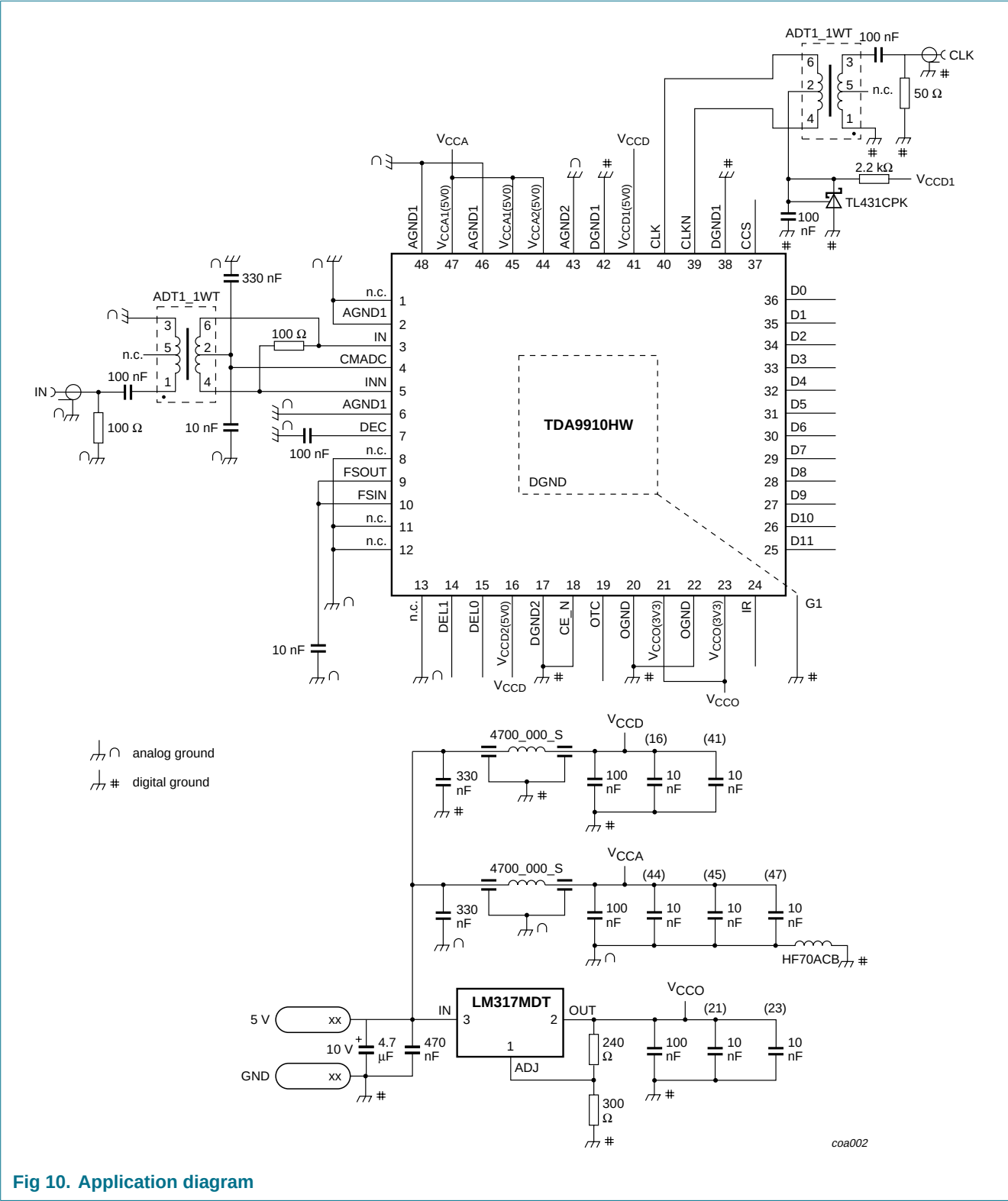


Fig 9. Adjacent channel sensitivity and ADC sensibility

11.2 Application diagram



SOT545-2



13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA9910_4	20070612	Product data sheet	-	TDA9910_3
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. Section 2 "Features": updated second feature - Type number TDA9910HW/6 removed from the data sheet Section 7 "Limiting values": output current Max. value updated Section 9 "Characteristics": values updated Figure 4: updated Figure 5: updated			
TDA9910_3	20060517	Preliminary data sheet	-	TDA9910_2
TDA9910_2 (9397 750 14418)	20041209	Objective data sheet	-	TDA9910_1
TDA9910_1 (9397 750 12905)	20041008	Objective data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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