74LV125

Quad buffer/line driver; 3-state

Rev. 03 — 7 April 2009　　　　　　　　　　　　　　　　**Product data sheet**

1. General description

The 74LV125 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC125 and 74HCT125.

The 74LV125 provides four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (n$\overline{OE}$). A HIGH at n$\overline{OE}$ causes the outputs to assume a high-impedance OFF-state.
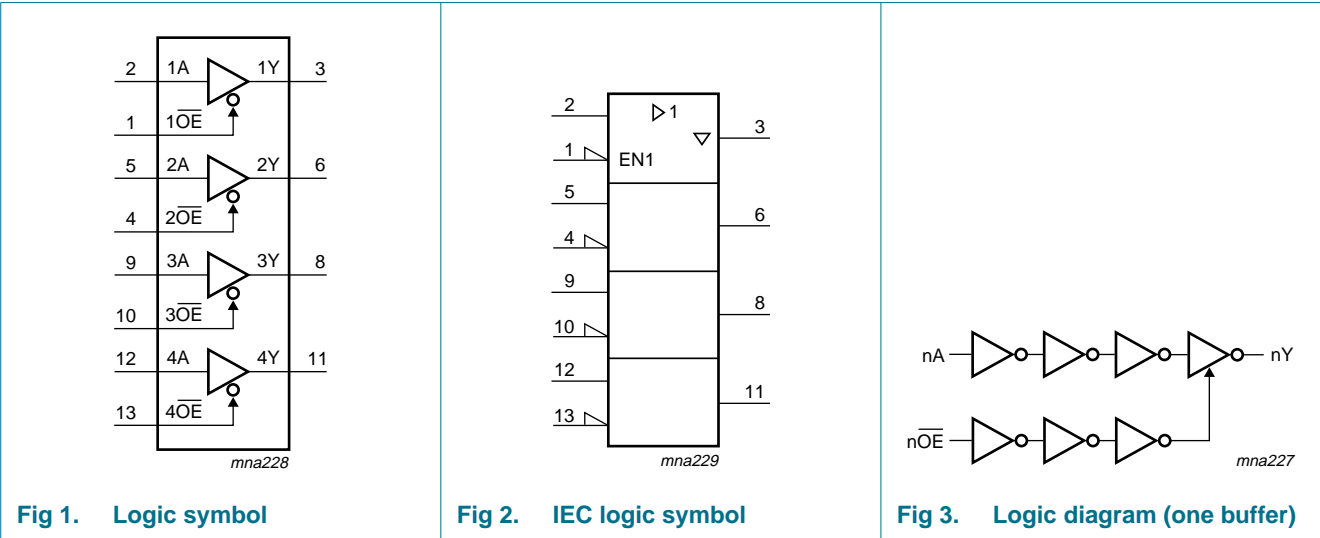
2. Features

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical output ground bounce < 0.8 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Typical HIGH-level output voltage (V_{OH}) undershoot: > 2 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2 000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C

3. Ordering information
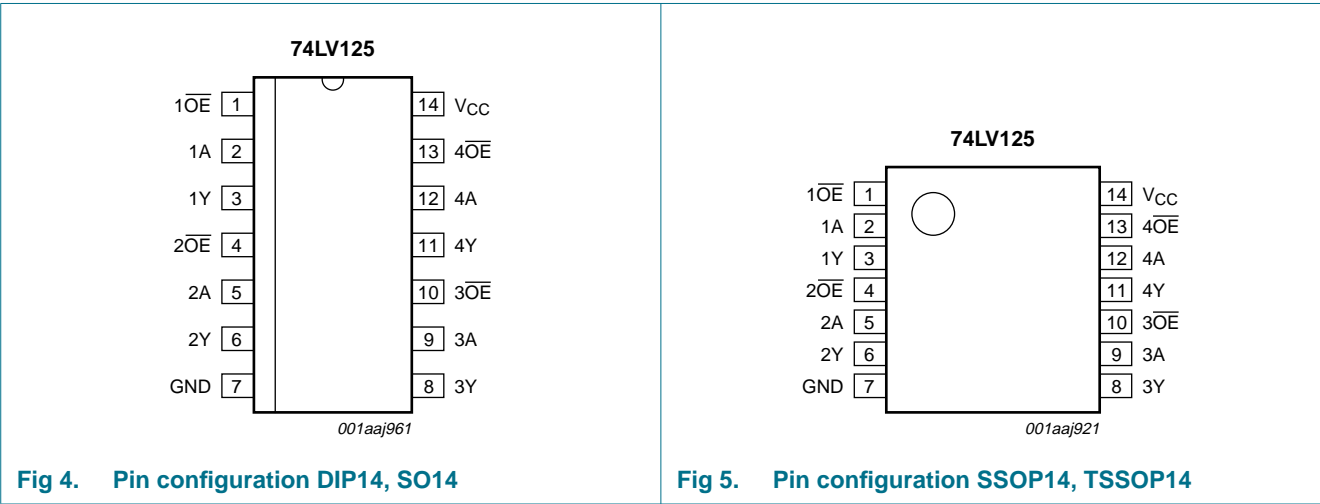
Table 1.　Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV125N	−40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74LV125D	−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV125DB	−40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LV125PW	−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

NXP
founded by Philips

4. Functional diagram

Fig 1.   Logic symbol

Fig 2.   IEC logic symbol

Fig 3.   Logic diagram (one buffer)

5. Pinning information

5.1 Pinning

Fig 4.   Pin configuration DIP14, SO14

Fig 5.   Pin configuration SSOP14, TSSOP14

5.2 Pin description

Table 2.   Pin description

Symbol	Pin	Description
1$\overline{\text{OE}}$, 2$\overline{\text{OE}}$, 3$\overline{\text{OE}}$, 4$\overline{\text{OE}}$,	1, 4, 10, 13	output enable input (active LOW)
1A, 2A, 3A, 4A	2, 5, 9, 12	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3.   Function table[1]

Control	Input	Output
n$\overline{\text{OE}}$	nA	nY
L	L	L
L	H	H
H	X	Z

[1]   H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4.   Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+7.0	V
I_{IK}	input clamping current	V_I < −0.5 V or V_I > V_{CC} + 0.5 V	[1]	-	±20	mA
I_{OK}	output clamping current	V_O < −0.5 V or V_O > V_{CC} + 0.5 V	[1]	-	±50	mA
I_O	output current	V_O = −0.5 V to (V_{CC} + 0.5 V)		-	±35	mA
I_{CC}	supply current			-	70	mA
I_{GND}	ground current			−70	-	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to +125 °C	[2]			
		DIP14		-	750	mW
		SO14, SSOP14, TSSOP14		-	500	mW

[1]   The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]   For DIP14 packages: above 70 °C the value of P_{tot} derates linearly with 12 mW/K.
　　　For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
　　　For (T)SSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

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8. Recommended operating conditions

Table 5.   Recommended operating conditions
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage[1]		1.0	3.3	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		−40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.0 V to 2.0 V	-	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V	-	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V	-	-	100	ns/V
		V_{CC} = 3.6 V to 5.5 V	-	-	50	ns/V

[1]   The static characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V, but LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

9. Static characteristics

Table 6.   Static characteristics
At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V_{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V_{CC} = 4.5 V to 5.5 V	$0.7V_{CC}$	-	-	$0.7V_{CC}$	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	$0.3V_{CC}$	-	$0.3V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = −100 μA; V_{CC} = 1.2 V	-	1.2	-	-	-	V
		I_O = −100 μA; V_{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		I_O = −100 μA; V_{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		I_O = −100 μA; V_{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		I_O = −100 μA; V_{CC} = 4.5 V	4.3	4.5	-	4.3	-	V
		I_O = −8 mA; V_{CC} = 3.0 V	2.4	2.82	-	2.2	-	V
		I_O = −16 mA; V_{CC} = 4.5 V	3.6	4.2	-	3.5	-	V

Table 6.   Static characteristics *...continued*
At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		$I_O = 100$ µA; $V_{CC} = 1.2$ V	-	0	-	-	-	V
		$I_O = 100$ µA; $V_{CC} = 2.0$ V	-	0	0.2	-	0.2	V
		$I_O = 100$ µA; $V_{CC} = 2.7$ V	-	0	0.2	-	0.2	V
		$I_O = 100$ µA; $V_{CC} = 3.0$ V	-	0	0.2	-	0.2	V
		$I_O = 100$ µA; $V_{CC} = 4.5$ V	-	0	0.2	-	0.2	V
		$I_O = 8$ mA; $V_{CC} = 3.0$ V	-	0.20	0.40	-	0.50	V
		$I_O = 16$ mA; $V_{CC} = 4.5$ V	-	0.35	0.55	-	0.65	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	1.0	-	1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	5	-	10	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	20	-	160	µA
ΔI_{CC}	additional supply current	per input; $V_I = V_{CC} - 0.6$ V; $V_{CC} = 2.7$ V to 3.6 V	-	-	500	-	850	µA
C_I	input capacitance		-	3.5	-	-	-	pF

[1]   Typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7.   Dynamic characteristics
*Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 8.*

| Symbol	Parameter	Conditions		−40 °C to +85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nY; see Figure 6	[2]						
		$V_{CC} = 1.2$ V		-	55	-	-	-	ns
		$V_{CC} = 2.0$ V		-	19	24	-	31	ns
		$V_{CC} = 2.7$ V		-	14	18	-	23	ns
		$V_{CC} = 3.0$ V to 3.6 V; $C_L = 15$ pF	[3]	-	9	-	-	-	ns
		$V_{CC} = 3.0$ V to 3.6 V	[3]	-	10	14	-	18	ns
		$V_{CC} = 4.5$ V to 5.5 V		-	-	12	-	15	ns
t_{en}	enable time	nOE to nY; see Figure 7	[2]						
		$V_{CC} = 1.2$ V		-	75	-	-	-	ns
		$V_{CC} = 2.0$ V		-	26	31	-	39	ns
		$V_{CC} = 2.7$ V		-	19	23	-	29	ns
		$V_{CC} = 3.0$ V to 3.6 V	[3]	-	14	18	-	23	ns
		$V_{CC} = 4.5$ V to 5.5 V		-	-	15	-	19	ns

Table 7.   Dynamic characteristics *…continued*
Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 8.

Symbol	Parameter	Conditions		−40 °C to +85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{dis}	disable time	n$\overline{OE}$ to nY; see Figure 7	[2]						
		V_{CC} = 1.2 V		-	65	-	-	-	ns
		V_{CC} = 2.0 V		-	24	32	-	39	ns
		V_{CC} = 2.7 V		-	18	24	-	29	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	14	20	-	24	ns
		V_{CC} = 4.5 V to 5.5 V		-	-	17	-	21	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC}; V_{CC} = 3.3 V	[4]	-	22	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V).

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_I = input frequency in MHz, f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. Waveforms
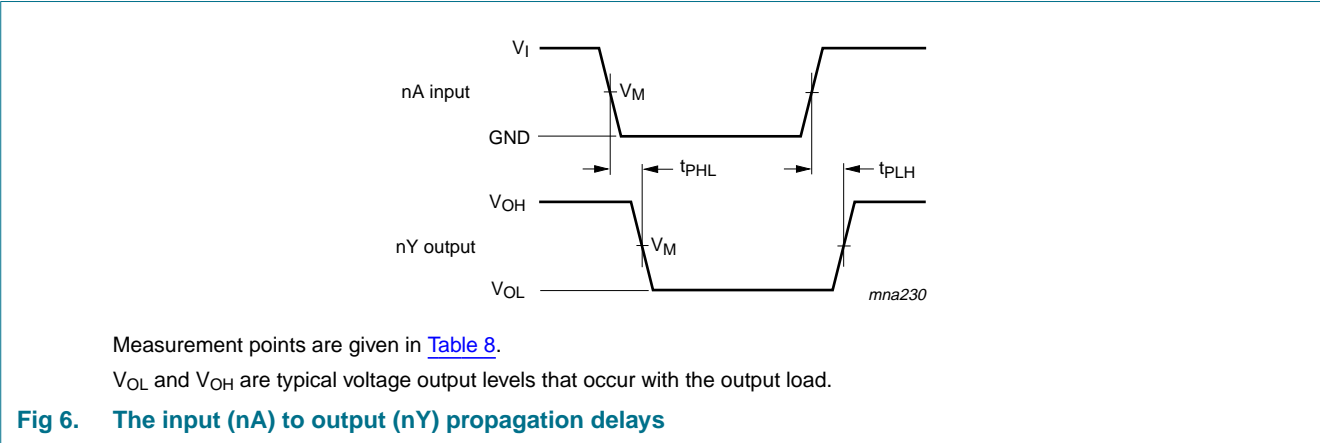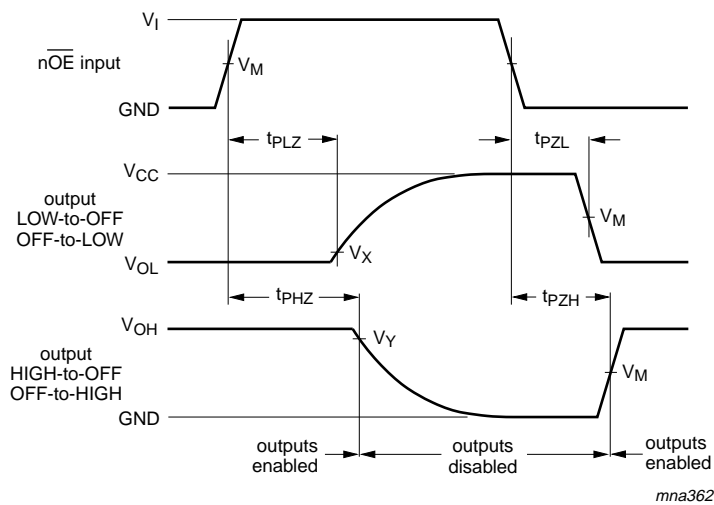
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6.   The input (nA) to output (nY) propagation delays

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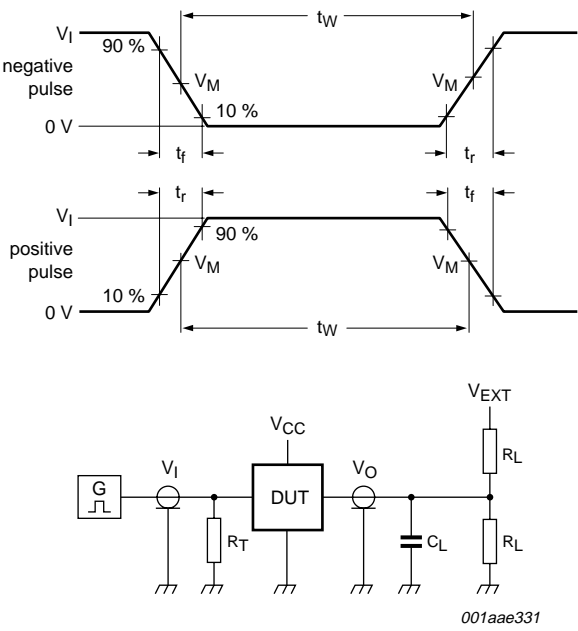**Product data sheet** **Rev. 03 — 7 April 2009** 6 of 15

Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7.   Enable and disable times

Table 8.   Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V
≥ 4.5 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$

Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 8.   Load circuit for measuring switching times

Table 9.   Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
< 2.7 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	open	GND	$2V_{CC}$
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns	15 pF, 50 pF	1 kΩ	open	GND	$2V_{CC}$
≥ 4.5 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	open	GND	$2V_{CC}$

12. Package outline

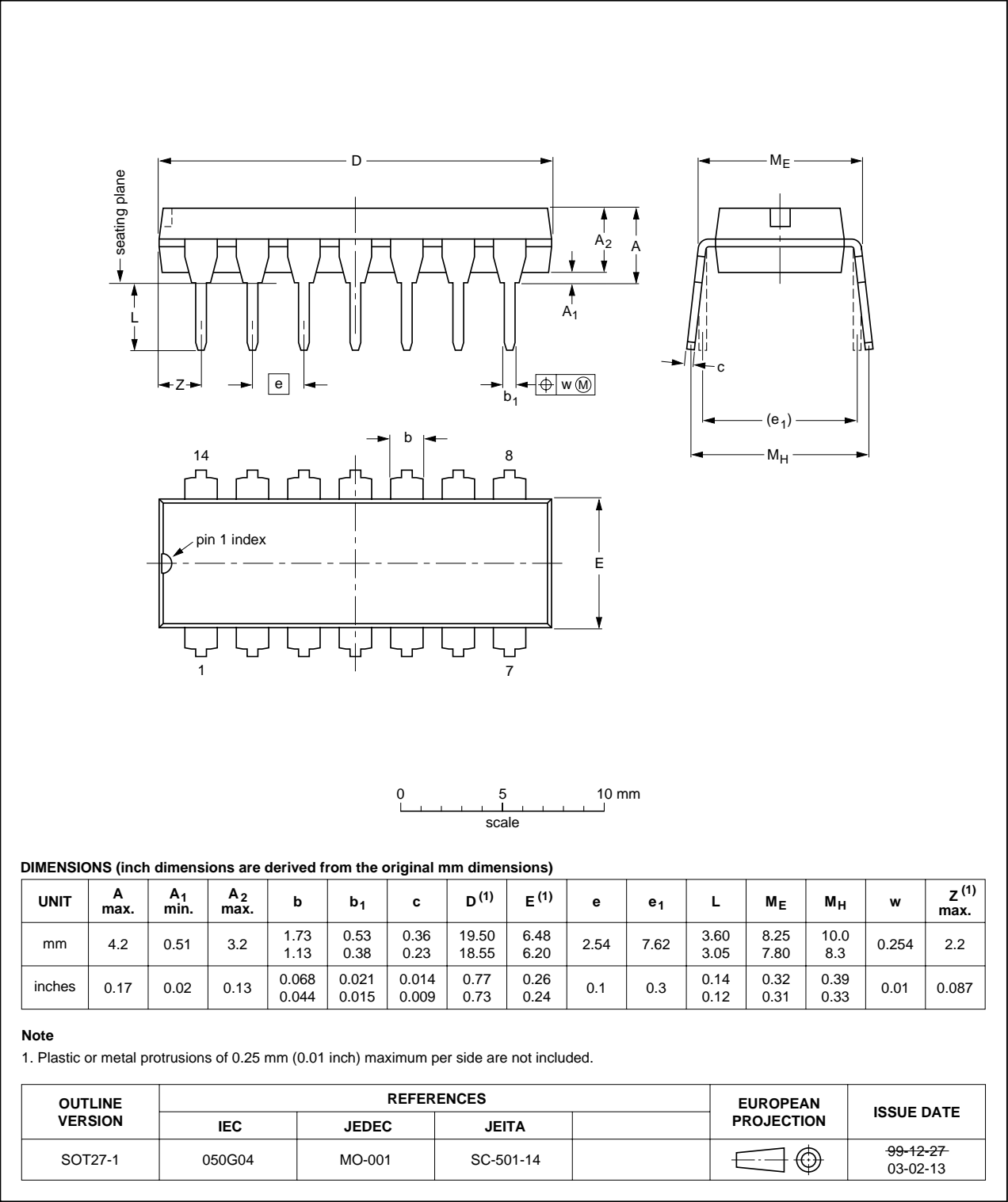**DIP14: plastic dual in-line package; 14 leads (300 mil)** SOT27-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁ min.	A₂ max.	b	b₁	c	D (1)	E (1)	e	e₁	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

Fig 9.   Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm SOT108-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	bp	c	D[1]	E[1]	e	HE	L	Lp	Q	v	w	y	Z[1]	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				99-12-27 03-02-19

Fig 10. Package outline SOT108-1 (SO14)

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm SOT337-1

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D(1)	E(1)	e	HₑE	L	Lₚ	Q	v	w	y	Z(1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19
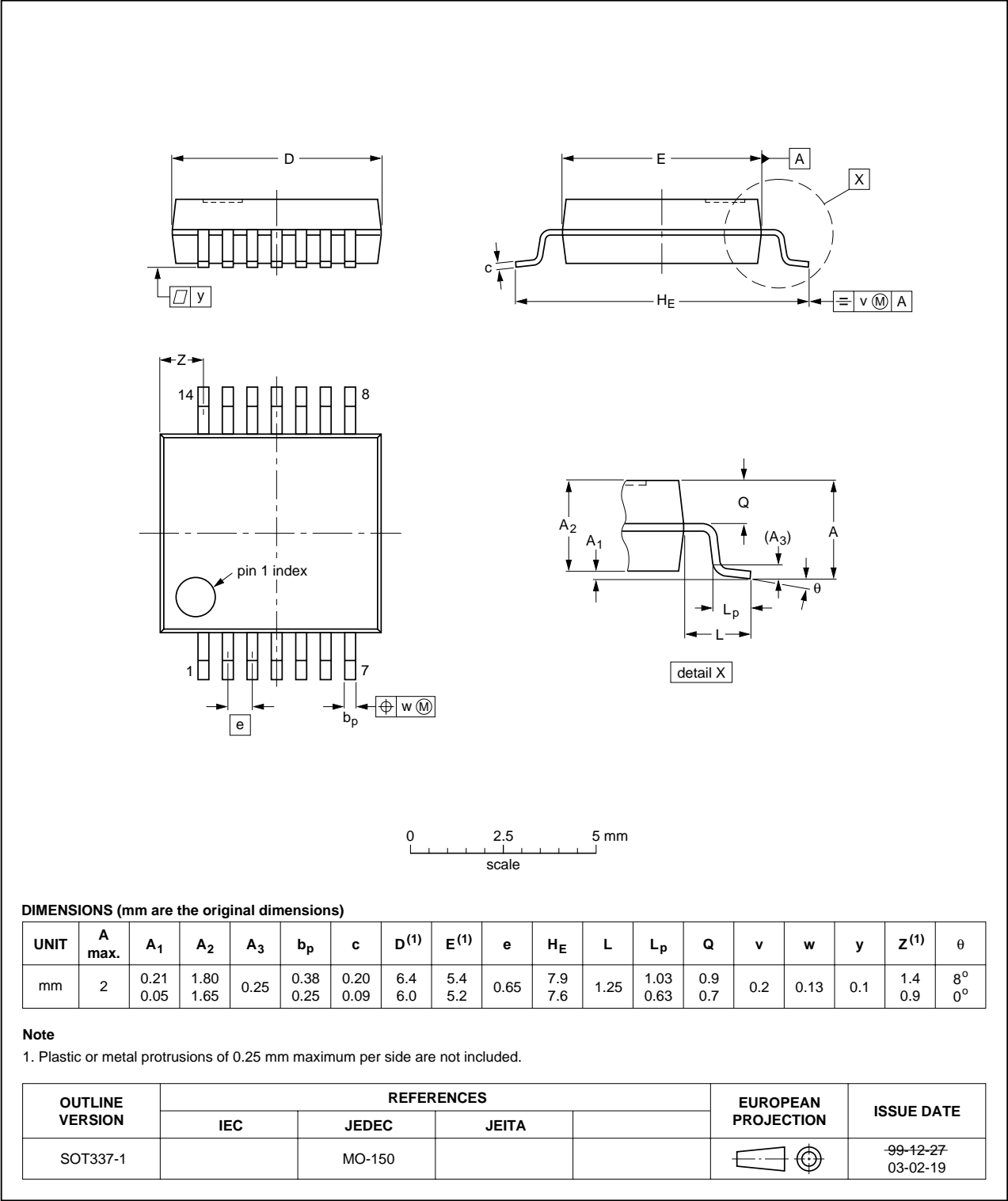
Fig 11. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm   **SOT402-1**

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D⁽¹⁾	E⁽²⁾	e	H_E	L	Lₚ	Q	v	w	y	Z⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 12. Package outline SOT402-1 (TSSOP14)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV125_3	20090407	Product data sheet	-	74LV125_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name when appropriate.			
74LV125_2	19980428	Product specification	-	74LV125_1
74LV125_1	19970203	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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