

# MTS Stereo Encoder

The MC44C402 Multi-Channel Television Sound (MTS) Stereo Encoder is based on the industry's first, single-chip, CMOS implementation of a Broadcast Television Systems Committee (BTSC)-compatible stereo encoder, the MC44C400.

The MC44C402 MTS Stereo Encoder is designed for use in set-top boxes, VCRs, DVD players/recorders, game stations, and other applications that are required to output high-quality stereo sound through a single RF coaxial cable.

The digital audio processing used in the MC44C402 preserves the full fidelity of surround sound and other audio coding schemes while ensuring overall system performance is not impacted by copy protection technologies.

The MC44C402 is engineered to process right and left analog audio signals and baseband composite video to generate a stereophonic composite signal in accordance with BTSC system standards. The MC44C402 is designed to output this signal to a Freescale RF modulator, which in turn produces a stereo encoded RF channel for use with any BTSC stereo television receiver.

## Features

- Integrated A/D converter input and D/A converter output circuitry
- CEX™ digital audio processing encodes and transports stereo signals
- Surround sound and Macrovision™ compatible
- Extended low frequency response (The MC44C402 frequency response extends below 25 Hz)
- Simple passive interface to Freescale's MC44BS373/4 (UHF/VHF) and MC44BC375 (VHF) modulators
- Preservation of original surround sound fidelity
- System performance not impacted by copy protection technologies
- Low system component count, small board size, and significantly low overall system cost
- No manual alignment of filters or phase controls

## Reference Documentation

"Multichannel Television Sound Transmission and Audio Processing Requirements for the BTSC System", FCC OET Bulletin No. 60, February 1986.

## MC44C402

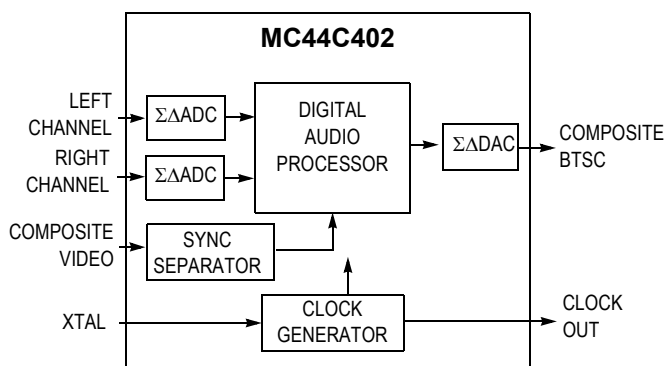
## MTS STEREO ENCODER



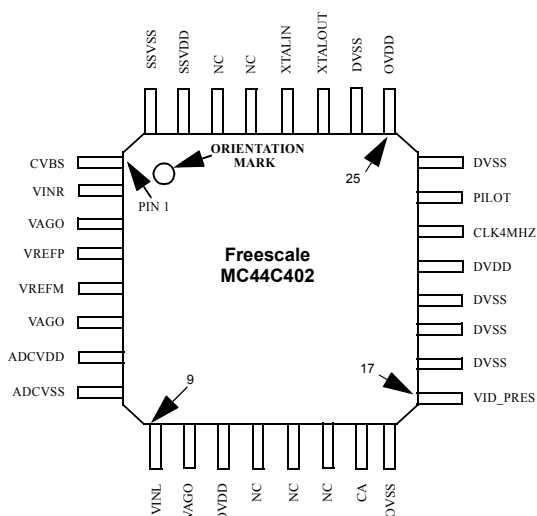
**AC SUFFIX**  
**32-LEAD LQFP PACKAGE**  
**CASE 873A-04**

## ORDERING INFORMATION

| Device       | Temp. Range    | Package     | RoHS |
|--------------|----------------|-------------|------|
| MC44C402AC   | −40°C to +85°C | 32LQFP      | yes  |
| MC44C402ACR2 |                | Tape & Reel | yes  |



Functional Block Diagram



MC44C402 32LQFP Package

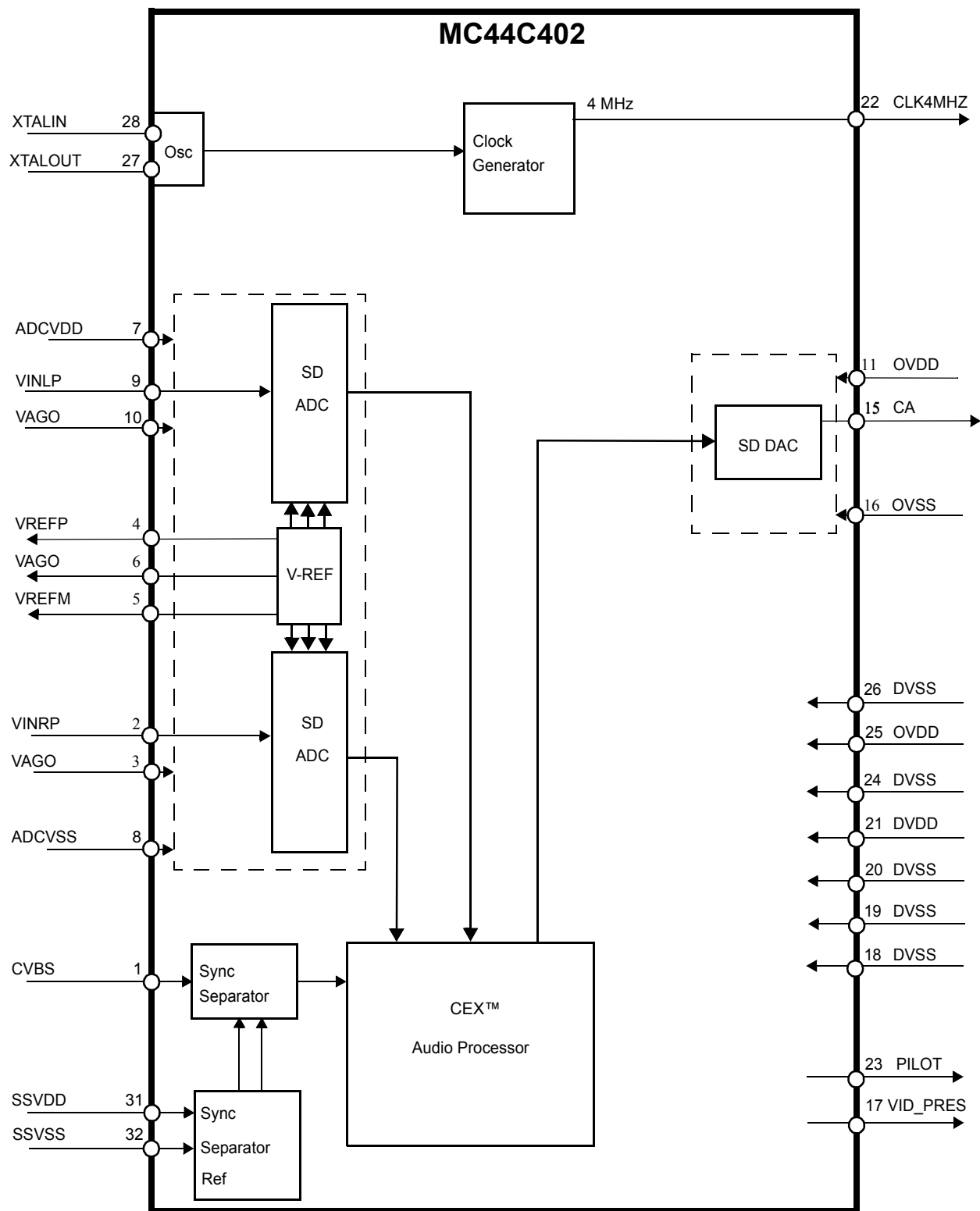


Figure 1. MC44C402 Block Diagram

## PIN DESCRIPTION

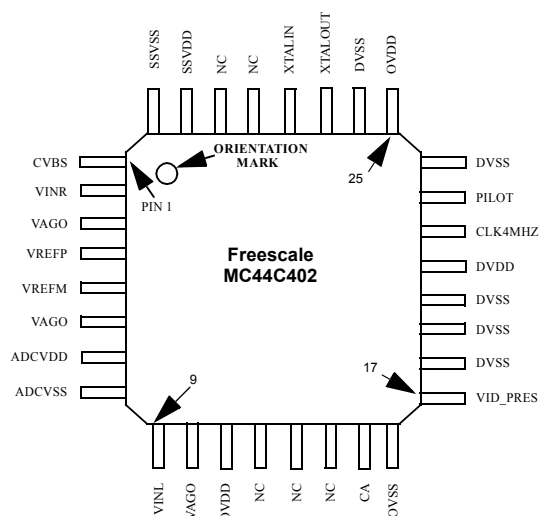


Figure 2. MC44C402 32LQFP Package

Table 1. Pin Descriptions (Listed by Function)

| Signal Name         | Pin #                  | Description                                                   |
|---------------------|------------------------|---------------------------------------------------------------|
| <b>Analog</b>       |                        |                                                               |
| VINL                | 9                      | Left channel input                                            |
| VREFP               | 4                      | ADC Voltage Ref. Bypass plus                                  |
| VAGO                | 3, 6, 10               | Analog virtual ground                                         |
| VREFM               | 5                      | ADC Voltage Ref. Bypass minus                                 |
| VINR                | 2                      | Right channel input                                           |
| CVBS                | 1                      | Composite video input to sync separator                       |
| <b>Digital</b>      |                        |                                                               |
| CA                  | 15                     | Composite Audio output                                        |
| VID_PRES            | 17                     | Video present flag, 0 = no video, hi-z = video present        |
| PILOT               | 23                     | 15.734 KHz square wave output phased locked to incoming video |
| NC                  | 12, 13, 14, 29, 30     | No Connection                                                 |
| <b>Clocks</b>       |                        |                                                               |
| XTALIN              | 28                     | Crystal oscillator input                                      |
| XTALOUT             | 27                     | Crystal oscillator output                                     |
| CLK4MHZ             | 22                     | 4 MHz clock output for Audio/Video modulator IC               |
| <b>Power Supply</b> |                        |                                                               |
| SSV <sub>DD</sub>   | 31                     | Sync Separator analog supply voltage, 3.3 V                   |
| SSV <sub>SS</sub>   | 32                     | Sync Separator analog ground                                  |
| ADCV <sub>DD</sub>  | 7                      | ADC analog supply voltage, 3.3 V                              |
| ADCV <sub>SS</sub>  | 8                      | ADC analog ground                                             |
| DV <sub>DD</sub>    | 21                     | Digital Logic supply voltage, 1.8 V                           |
| DV <sub>SS</sub>    | 16, 18, 19, 20, 24, 26 | Digital Logic and I/O grounds                                 |
| OV <sub>DD</sub>    | 11, 25                 | I/O supply voltage, 3.3 V                                     |

## ELECTRICAL SPECIFICATIONS

**Table 2. Absolute Maximum Ratings**

Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

| Characteristic                 | Symbol             | Min  | Max                     | Units |
|--------------------------------|--------------------|------|-------------------------|-------|
| Digital Logic Supply Voltage   | DV <sub>DD</sub>   | -0.3 | +2.0                    | V     |
| Digital Output Supply Voltage  | OV <sub>DD</sub>   | -0.3 | +4.0                    | V     |
| ADC Supply Voltage             | ADCV <sub>DD</sub> | -0.3 | +4.0                    | V     |
| Sync. Separator Supply Voltage | SSV <sub>DD</sub>  | -0.3 | +4.0                    | V     |
| Input Voltage                  | V <sub>in</sub>    | -0.3 | xxV <sub>DD</sub> + 0.3 | V     |
| Storage Temperature Range      | T <sub>stg</sub>   | -55  | +150                    | °C    |

**Table 3. General Specifications**

| Characteristic                    | Symbol | Min  | Typ | max | Units |
|-----------------------------------|--------|------|-----|-----|-------|
| ESD Protection (Machine Model)    | MM     | 200  |     |     | V     |
| ESD Protection (Human Body Model) | HBM    | 2000 |     |     | V     |
| Latch-Up Immunity                 | LU     | 200  |     |     | mA    |

**Table 4. Recommended Operating Conditions**

| Characteristic                             | Symbol                              | Min   | Typ  | Max   | Units           |
|--------------------------------------------|-------------------------------------|-------|------|-------|-----------------|
| Digital Logic Supply Voltage               | DV <sub>DD</sub>                    | +1.62 | +1.8 | +1.98 | V               |
| Digital Output Supply Voltage              | OV <sub>DD</sub>                    | +2.97 | +3.3 | +3.63 | V               |
| ADC Supply Voltage                         | ADCV <sub>DD</sub>                  | +2.97 | +3.3 | +3.63 | V               |
| Sync. Separator Supply Voltage             | SSV <sub>DD</sub>                   | +2.97 | +3.3 | +3.63 | V               |
| Left/Right Channel Input Level             | V <sub>INL</sub> , V <sub>INR</sub> |       |      | 1.8   | V <sub>pp</sub> |
| Composite Video Input Level (See Figure 8) | CVBS                                | 0.5   | 1.0  | 2.0   | V <sub>pp</sub> |
| Ambient Temperature                        | T <sub>A</sub>                      | -40   |      | +85   | °C              |

**Table 5. DC Characteristics**

| Characteristic <sup>(1)</sup>      | Symbol              | Min  | Typ  | Max  | Units |
|------------------------------------|---------------------|------|------|------|-------|
| Digital Logic Supply Current       | IDV <sub>DD</sub>   |      | 7.5  | 8.5  | mA    |
| Digital Output Supply Current      | IOV <sub>DD</sub>   |      | 2.0  | 8.0  | mA    |
| ADC Supply Current                 | IADCV <sub>DD</sub> |      | 7.0  | 9.0  | mA    |
| Sync. Separator Supply Current     | ISSV <sub>DD</sub>  |      | 2.0  |      | mA    |
| CLK4MHZ, Clock Output @ I = 0.6 mA | V <sub>ol</sub>     | 2.97 |      |      | V     |
| ADC Voltage Ref. Bypass plus       | VREFP               |      | +2.0 |      | V     |
| ADC Voltage Ref. Bypass minus      | VREFM               |      | +1.0 |      | V     |
| ADC Voltage Ref. Ground            | VAGO                |      | +1.5 |      | V     |
| CLK4MHZ, Clock Output @ I = 0.6 mA | V <sub>oh</sub>     |      |      | 3.63 | V     |

1. Unless other wise noted; DV<sub>DD</sub> = 1.8 ± 0.18 Vdc, OV<sub>DD</sub> = ADCV<sub>DD</sub> = SSV<sub>DD</sub> = 3.3 ± 0.33 Vdc, GND = 0 Vdc, -40 ≤ T<sub>A</sub> ≤ 85°C.

**Table 6. AC Characteristics**

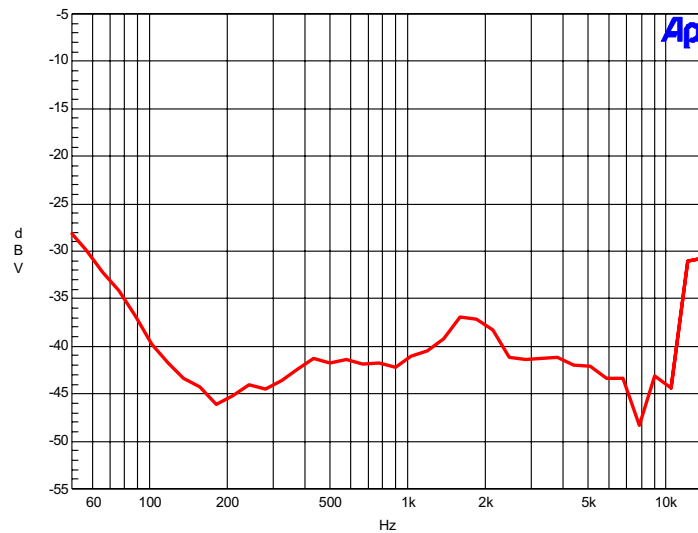
| Characteristic <sup>(1)</sup>                    | Symbol   | Min | Typ | Max   | Units     |
|--------------------------------------------------|----------|-----|-----|-------|-----------|
| Input Impedance (Left/Right Input)               | $R_{in}$ |     | 75  |       | $k\Omega$ |
| Composite Audio Output Level <sup>(2)</sup>      | CA       |     | 1.0 |       | $V_{pp}$  |
| Composite Output Level                           | CA       |     |     | 2.2   | $V_{pp}$  |
| Signal to Noise Ratio <sup>(2),(3)</sup>         | SNR      | 72  | 75  |       | dB        |
| Total Harmonic Distortion <sup>(2),(3)</sup>     | THD      |     | 0.1 | 0.3   | %         |
| -1 dB Bandwidth                                  | BW       | 20  |     | 14500 | Hz        |
| Stereo Separation 500 Hz - 5 KHz <sup>(4)</sup>  |          |     | 35  |       | dB        |
| Stereo Separation 100 Hz - 10 KHz <sup>(4)</sup> |          | 30  | 35  |       | dB        |

1. Unless other wise noted;  $DV_{DD} = 1.8 \pm 0.18$  Vdc,  $OV_{DD} = ADCV_{DD} = SSV_{DD} = 3.3 \pm 0.33$  Vdc, GND = 0 Vdc,  $-40 \leq T_A \leq 85^\circ\text{C}$ .

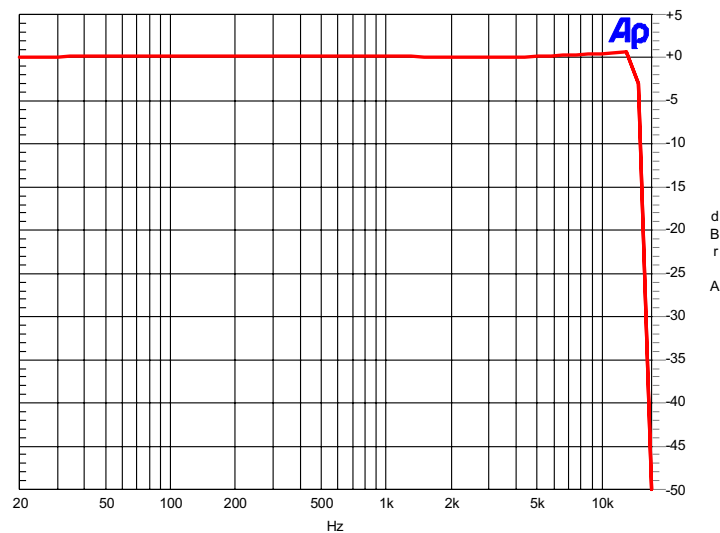
2. Test conditions, mono, 1 kHz @ 1.5  $V_{pp}$

3. Measured in 20 Hz to 13.5 kHz bandwidth

4. Measured -10 dB input level



**Figure 3. Stereo Separation**



**Figure 4. Amplitude Response**

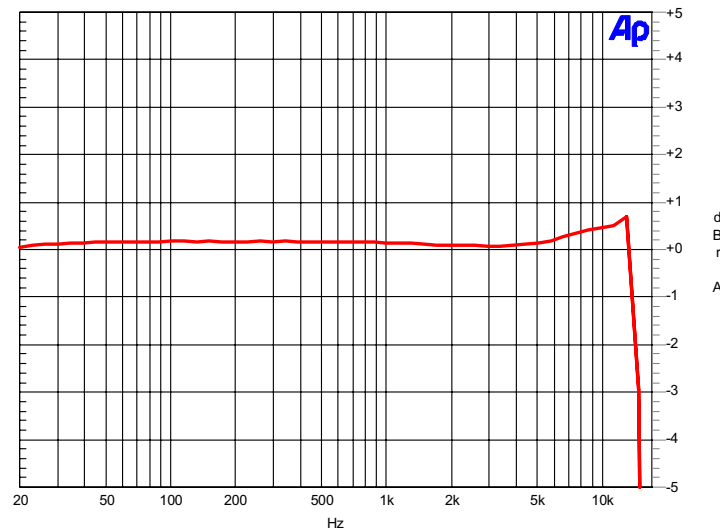


Figure 5. Amplitude Ripple

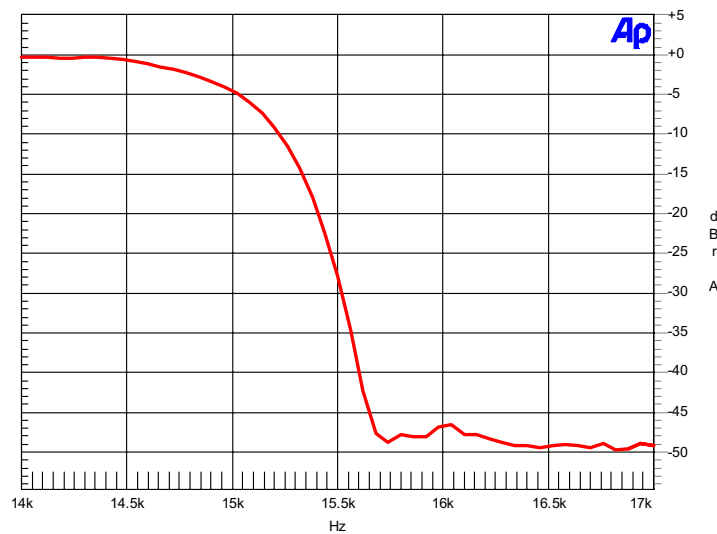


Figure 6. Amplitude-Notch

## SYSTEM APPLICATION NOTES

### DESIGN CONSIDERATIONS

When developing application using the MC44C402 Stereo Encoder, the user can significantly improve the performance by following the suggestions below:

1. Disable the pre-emphasis on the modulator
2. There must be a 4.5 MHz notch in the video because Video spectra that fall into the 4.5 MHz range will severely impact the audio performance. See the notch filter shown in Figure 7.
3. Measurements must be made with a precision demodulator followed by a precision decoder, measuring audio performance using mono or wide band output will give erroneous results. We suggest the setup as described below
4. A low pass filter is required on the CA (baseband) output. The filter shown in Figure 7 note 1 is recommended. It is a Bessel filter with uniform group delay to 50 kHz and an input impedance of 500Ω and high output impedance.
5. Crystal frequency is critical. It MUST be within +/- 2 kHz (100 PPM) under all conditions. Recommend 30 PPM or better at room temperature. Measure the frequency, being careful not to load the crystal oscillator pins or alternatively the frequency can be determined by measuring the 4 MHz using (spectrum analyzer), being careful not to load the crystal oscillator pins, or with a frequency counter on the 4 MHz port to +/- 400 Hz max or 100 Hz at room temp. A symptom of the crystal being off frequency is stereo separation changing at about a 1 Hz rate (Pulsing).

Equipment suggestions

|              |                     |        |
|--------------|---------------------|--------|
| Demodulator: | Tektronix           | TV1450 |
| Decoder:     | Modulation Sciences | SRD-1  |

### MC44C402

## MODULATOR INTERFACE

1. The 4 MHz clock drive to the MC44BS373 must be filtered and the level set correctly. This can be achieved simply by using a 1  $\mu$ H inductor and 1500 pF and series 750 ohm resistor and 100 pF blocking cap, as shown in [Figure 7](#) note 2.
2. The MC44BS373 SPLL filter must be changed to a single 2.2  $\mu$ F capacitor to ground. Please see [Figure 7](#) note 3. (note some caps exhibit microphonic problems in this application).
3. Input impedance of the MC44BS373 is around 70 Kohms and to preserve the low frequency performance the coupling caps should be greater than 0.1  $\mu$ F

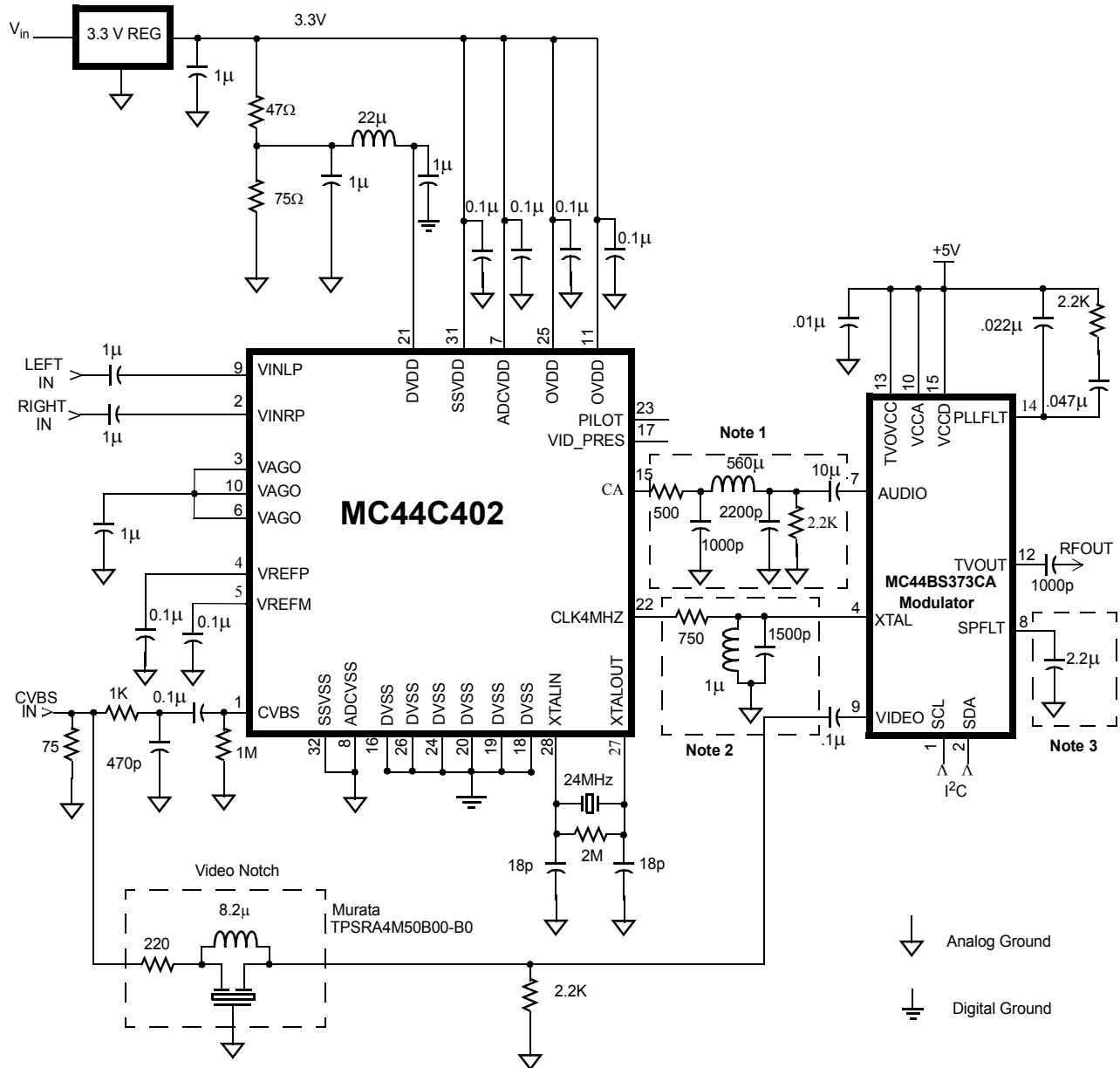
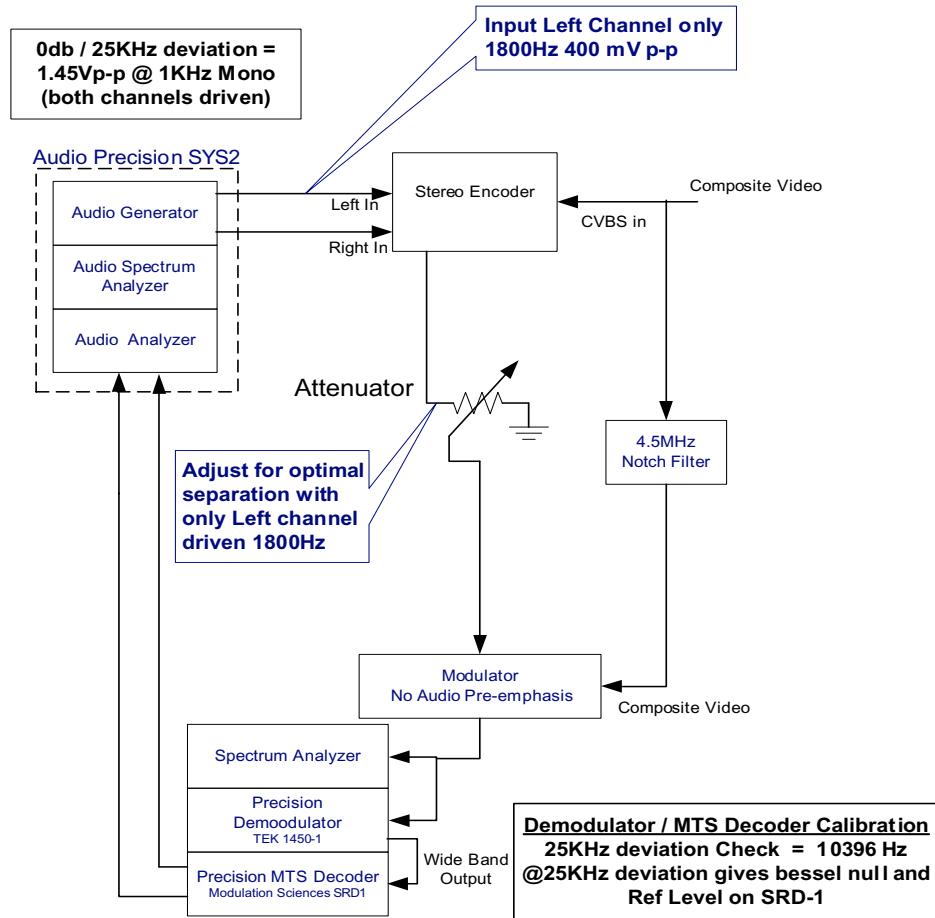


Figure 7. MC44C402 Typical Application Circuit

## SETTING LEVEL FOR MODULATOR/ENCODER INTERFACE

1. Verify calibration of the equipment. This requires a modulator and precision signal source. The audio signal cannot be passed through the stereo encoder for this setup. Suggest using 10396.48 Hz audio test signal directly into first Bessel null on a spectrum analyzer.
2. Input 1800 Hz @ 0.4 V p-p into left channel and set adjust attenuation between stereo encoder and the modulator for optimum separation using calibrated demodulator and decoder.



- 1) Calibrate MTS Decoder to Demodulator connection using Bessel Null Technique
- 2) input 1.8KHz 0.4 V p-p on left channel only and optimize stereo separation with attenuator.

Figure 8. MC44C402 Level Setup

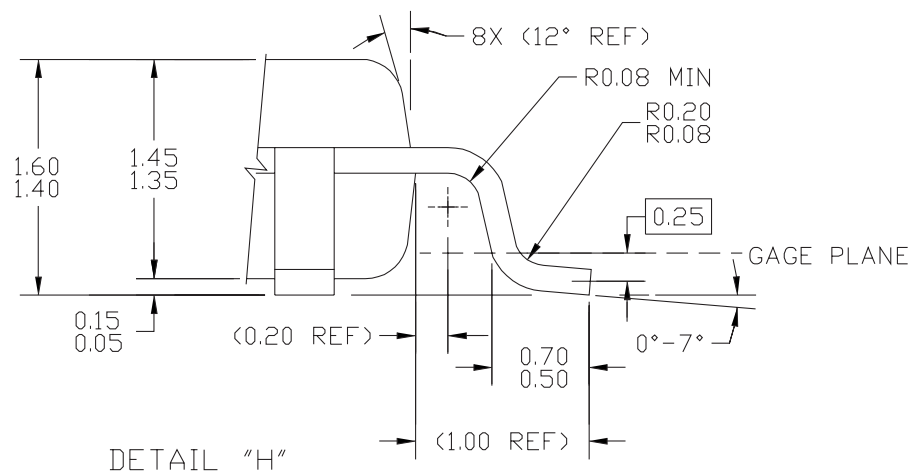
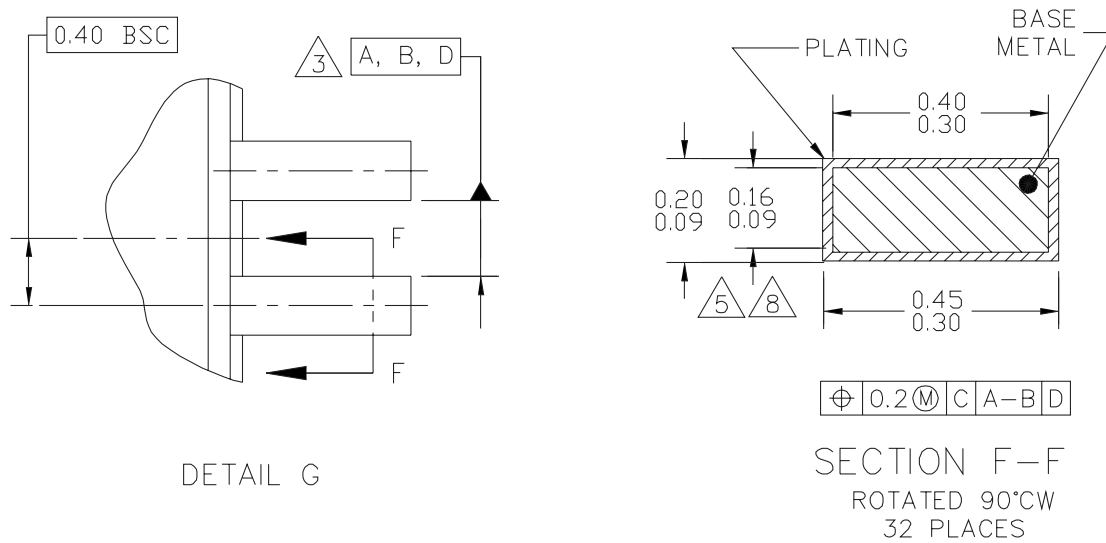


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PAGE 1 OF 3

MC44C402

## PACKAGE DATA



|                                                                                 |                            |                            |             |
|---------------------------------------------------------------------------------|----------------------------|----------------------------|-------------|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED.                         | MECHANICAL OUTLINE         | PRINT VERSION NOT TO SCALE |             |
| TITLE:<br>LOW PROFILE QUAD FLAT PACK (LQFP)<br>32 LEAD, 0.8 PITCH (7 X 7 X 1.4) | DOCUMENT NO: 98ASH70029A   |                            | REV: C      |
|                                                                                 | CASE NUMBER: 873A-04       |                            | 01 APR 2005 |
|                                                                                 | STANDARD: JEDEC MS-026 BBA |                            |             |

PAGE 2 OF 3

Figure 9. 32QLFP Package Mechanical Data (continued)

## PACKAGE DATA

### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5-1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

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PAGE 3 OF 3

**Figure 9. 32QLFP Package Mechanical Data (continued)**

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