

FEATURES

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.1 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} Supports Partial-Power-Down Mode Operation
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

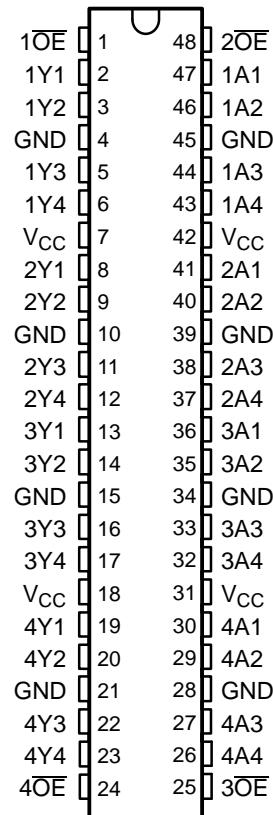
This 16-bit buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC16244A is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

**DGG, DGV, OR DL PACKAGE
(TOP VIEW)**



ORDERING INFORMATION

| T _A | PACKAGE ⁽¹⁾ | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|-----------------------|------------------|
| –40°C to 85°C | FBGA – GRD | Tape and reel | LD244A |
| | FBGA – ZRD (Pb-free) | | |
| | SSOP – DL | Tube | LVC16244A |
| | | Tape and reel | |
| | TSSOP – DGG | Tape and reel | LVC16244A |
| | | | |
| TVSOP – DGV | Tape and reel | SN74LVC16244ADGVR | LD244A |
| | | 74LVC16244ADGVR | |
| VFBGA – GQL | Tape and reel | SN74LVC16244AGQLR | LD244A |
| | | 74LVC16244AGQLR | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

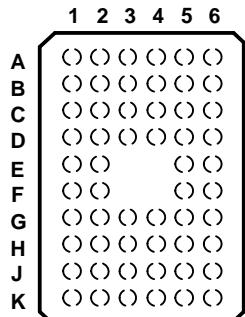
Widebus is a trademark of Texas Instruments.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**GQL OR ZQL PACKAGE
(TOP VIEW)**

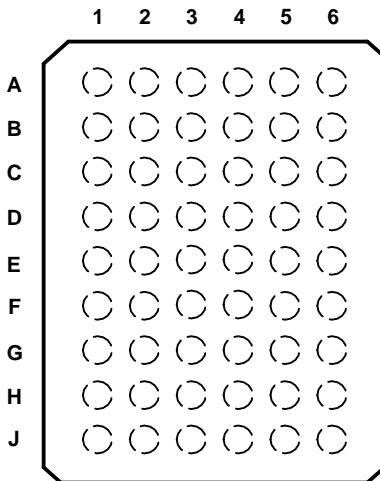


**TERMINAL ASSIGNMENTS⁽¹⁾
(56-Ball GQL Package)**

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|------------------|-----|----------|----------|-----|------------------|
| A | $1\overline{OE}$ | NC | NC | NC | NC | $2\overline{OE}$ |
| B | 1Y2 | 1Y1 | GND | GND | 1A1 | 1A2 |
| C | 1Y4 | 1Y3 | V_{CC} | V_{CC} | 1A3 | 1A4 |
| D | 2Y2 | 2Y1 | GND | GND | 2A1 | 2A2 |
| E | 2Y4 | 2Y3 | | | 2A3 | 2A4 |
| F | 3Y1 | 3Y2 | | | 3A2 | 3A1 |
| G | 3Y3 | 3Y4 | GND | GND | 3A4 | 3A3 |
| H | 4Y1 | 4Y2 | V_{CC} | V_{CC} | 4A2 | 4A1 |
| J | 4Y3 | 4Y4 | GND | GND | 4A4 | 4A3 |
| K | $4\overline{OE}$ | NC | NC | NC | NC | $3\overline{OE}$ |

(1) NC – No internal connection

**GRD OR ZRD PACKAGE
(TOP VIEW)**



**TERMINAL ASSIGNMENTS⁽¹⁾
(54-Ball GRD/ZRD Package)**

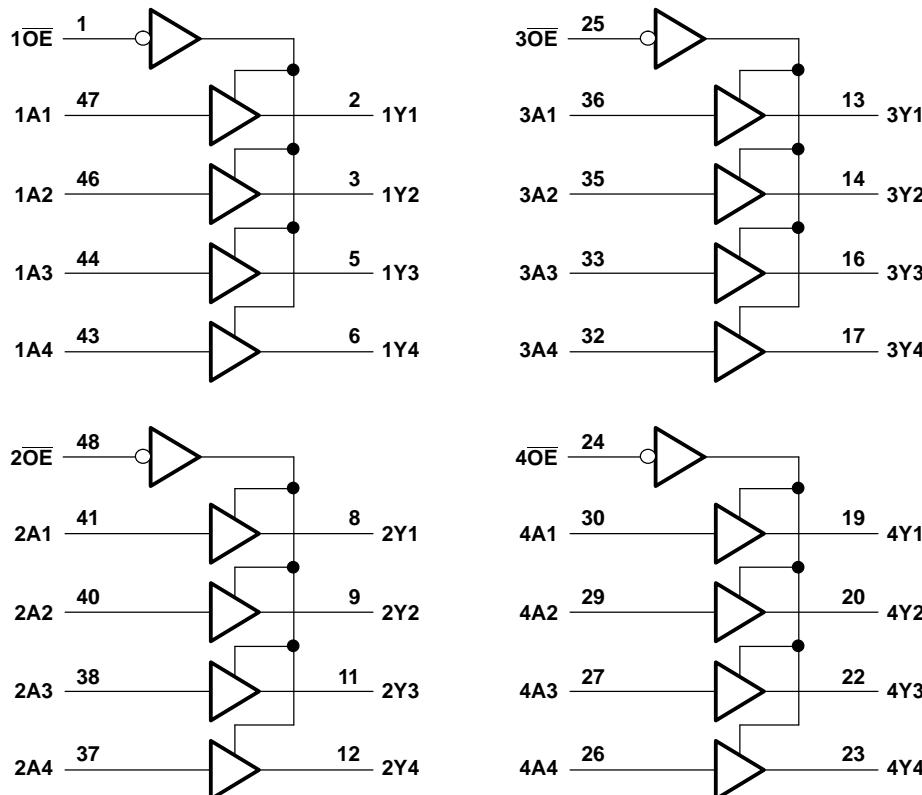
| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|-----|-----|------------------|------------------|-----|-----|
| A | 1Y1 | NC | $1\overline{OE}$ | $2\overline{OE}$ | NC | 1A1 |
| B | 1Y3 | 1Y2 | NC | NC | 1A2 | 1A3 |
| C | 2Y1 | 1Y4 | V_{CC} | V_{CC} | 1A4 | 2A1 |
| D | 2Y3 | 2Y2 | GND | GND | 2A2 | 2A3 |
| E | 3Y1 | 2Y4 | GND | GND | 2A4 | 3A1 |
| F | 3Y3 | 3Y2 | GND | GND | 3A2 | 3A3 |
| G | 4Y1 | 3Y4 | V_{CC} | V_{CC} | 3A4 | 4A1 |
| H | 4Y3 | 4Y2 | NC | NC | 4A2 | 4A3 |
| J | 4Y4 | NC | $4\overline{OE}$ | $3\overline{OE}$ | NC | 4A4 |

(1) NC – No internal connection

**FUNCTION TABLE
(EACH 4-BIT BUFFER)**

| INPUTS | | OUTPUT Y |
|-----------------|---|-------------|
| \overline{OE} | A | |
| L | H | H |
| L | L | L |
| H | X | Z |

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DGV, and DL packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|---|-----------------|----------------|------|
| V_{CC} | Supply voltage range | -0.5 | 6.5 | V |
| V_I | Input voltage range ⁽²⁾ | -0.5 | 6.5 | V |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 6.5 | V |
| V_O | Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾ | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current $V_I < 0$ | | -50 | mA |
| I_{OK} | Output clamp current $V_O < 0$ | | -50 | mA |
| I_O | Continuous output current | | ± 50 | mA |
| | Continuous current through each V_{CC} or GND | | ± 100 | mA |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | DGG package | 70 | °C/W |
| | | DGV package | 58 | |
| | | DL package | 63 | |
| | | GQL package | 42 | |
| | | GRD/ZRD package | 36 | |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the recommended operating conditions table.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

SN74LVC16244A
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCAS699A—AUGUST 2003—REVISED OCTOBER 2005

 **TEXAS**
INSTRUMENTS
www.ti.com

Recommended Operating Conditions⁽¹⁾

| | | | MIN | MAX | UNIT |
|---------------------|------------------------------------|---|----------------------|----------|------|
| V_{CC} | Supply voltage | Operating | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| V_{IH} | High-level input voltage | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | $0.65 \times V_{CC}$ | | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.7 | | |
| | | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | 2 | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | $0.35 \times V_{CC}$ | | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 0.7 | | |
| | | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | 0.8 | | |
| V_I | Input voltage | | 0 | 5.5 | V |
| V_O | Output voltage | High or low state | 0 | V_{CC} | V |
| | | 3-state | 0 | 5.5 | |
| I_{OH} | High-level output current | $V_{CC} = 1.65\text{ V}$ | | -4 | mA |
| | | $V_{CC} = 2.3\text{ V}$ | | -8 | |
| | | $V_{CC} = 2.7\text{ V}$ | | -12 | |
| | | $V_{CC} = 3\text{ V}$ | | -24 | |
| I_{OL} | Low-level output current | $V_{CC} = 1.65\text{ V}$ | | 4 | mA |
| | | $V_{CC} = 2.3\text{ V}$ | | 8 | |
| | | $V_{CC} = 2.7\text{ V}$ | | 12 | |
| | | $V_{CC} = 3\text{ V}$ | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 10 | ns/V |
| T_A | Operating free-air temperature | | -40 | 85 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------|--|--------------------|-----------------|--------------------|-----|------|
| V _{OH} | I _{OH} = -100 µA | 1.65 V to 3.6 V | V _{CC} | -0.2 | | V |
| | I _{OH} = -4 mA | 1.65 V | | 1.2 | | |
| | I _{OH} = -8 mA | 2.3 V | | 1.7 | | |
| | I _{OH} = -12 mA | 2.7 V | | 2.2 | | |
| | I _{OH} = -24 mA | 3 V | | 2.4 | | |
| V _{OL} | I _{OL} = 100 µA | 1.65 V to 3.6 V | | 0.2 | | V |
| | I _{OL} = 4 mA | 1.65 V | | 0.45 | | |
| | I _{OL} = 8 mA | 2.3 V | | 0.7 | | |
| | I _{OL} = 12 mA | 2.7 V | | 0.4 | | |
| | I _{OL} = 24 mA | 3 V | | 0.55 | | |
| I _I | V _I = 0 to 5.5 V | 3.6 V | | ±5 | µA | |
| I _{off} | V _I or V _O = 5.5 V | 0 | | ±10 | µA | |
| I _{OZ} | V _O = 0 to 5.5 V | 3.6 V | | ±10 | µA | |
| I _{CC} | V _I = V _{CC} or GND | I _O = 0 | 3.6 V | | 20 | µA |
| | 3.6 V ≤ V _I ≤ 5.5 V ⁽²⁾ | | | | 20 | |
| ΔI _{CC} | One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND | | 2.7 V to 3.6 V | | 500 | µA |
| C _i | V _I = V _{CC} or GND | | 3.3 V | | 5.5 | pF |
| C _o | V _O = V _{CC} or GND | | 3.3 V | | 6 | pF |

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This applies in the disabled state only.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

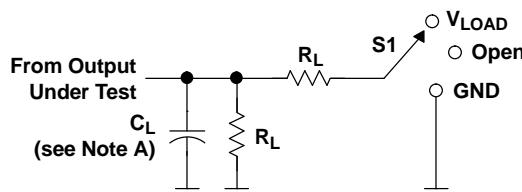
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V ± 0.15 V | V _{CC} = 2.5 V ± 0.2 V | V _{CC} = 2.7 V | V _{CC} = 3.3 V ± 0.3 V | UNIT | | | | |
|--------------------|-----------------|----------------|-------------------------------------|------------------------------------|-------------------------|------------------------------------|------|-----|-----|-----|----|
| | | | MIN | MAX | MIN | MAX | | | | | |
| t _{pd} | A | Y | 1.5 | 6.6 | 1 | 3.9 | 1 | 4.7 | 1.1 | 4.1 | ns |
| t _{en} | OE | Y | 1.5 | 7.5 | 1 | 4.7 | 1 | 5.8 | 1 | 4.6 | ns |
| t _{dis} | OE | Y | 1.5 | 10.3 | 1 | 5.3 | 1 | 6.2 | 1.8 | 5.8 | ns |
| t _{sk(o)} | | | | | | | | | 1 | ns | |

Operating Characteristics

T_A = 25°C

| PARAMETER | TEST CONDITIONS | V _{CC} = 1.8 V | V _{CC} = 2.5 V | V _{CC} = 3.3 V | UNIT | |
|-----------------|---|-------------------------|-------------------------|-------------------------|------|----|
| | | TYP | TYP | TYP | | |
| C _{pd} | Power dissipation capacitance per buffer/driver | f = 10 MHz | 33 | 35 | 39 | pF |
| | | | 2 | 3 | 4 | |

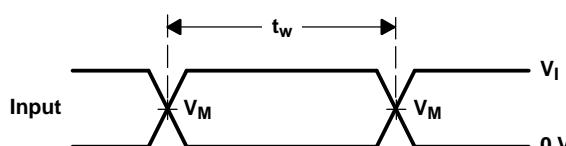
PARAMETER MEASUREMENT INFORMATION



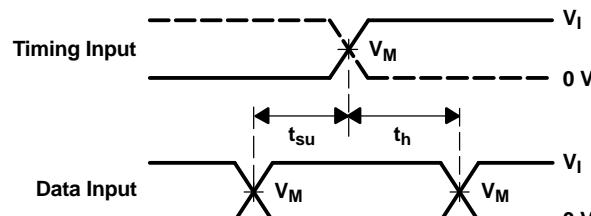
| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

LOAD CIRCUIT

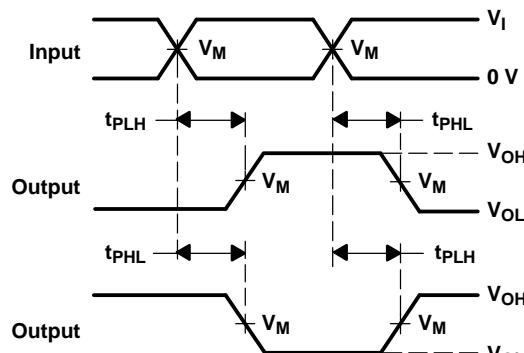
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_Δ |
|------------------------------------|----------|-----------------------|------------|-------------------|-------|--------------|------------|
| | V_I | t_r/t_f | | | | | |
| $1.8 \text{ V} \pm 0.15 \text{ V}$ | V_{CC} | $\leq 2 \text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5 \text{ V} \pm 0.2 \text{ V}$ | V_{CC} | $\leq 2 \text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | $\leq 2.5 \text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $3.3 \text{ V} \pm 0.3 \text{ V}$ | 2.7 V | $\leq 2.5 \text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



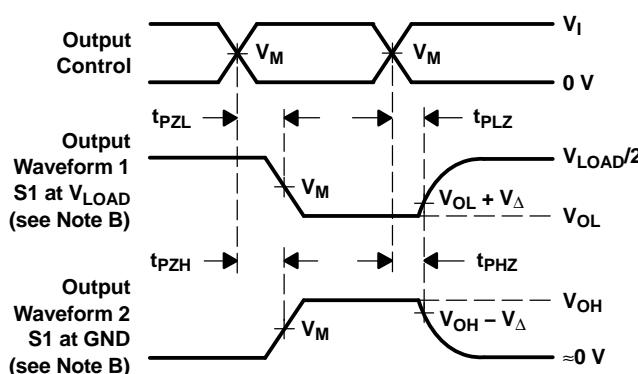
**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|--------------------|-----------------------|-------------------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 74LVC16244ADGGRG4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74LVC16244ADGVRE4 | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC16244ADGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74LVC16244ADGVR | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC16244ADL | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC16244ADLG4 | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC16244ADLR | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC16244ADLRG4 | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC16244AGQLR | ACTIVE | BGA MI CROSTA R JUNI OR | GQL | 56 | 1000 | TBD | SNPB | Level-1-240C-UNLIM |
| SN74LVC16244AGRDR | ACTIVE | BGA MI CROSTA R JUNI OR | GRD | 54 | 1000 | TBD | SNPB | Level-1-240C-UNLIM |
| SN74LVC16244AZQLR | ACTIVE | BGA MI CROSTA R JUNI OR | ZQL | 56 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM |
| SN74LVC16244AZRDR | ACTIVE | BGA MI CROSTA R JUNI OR | ZRD | 54 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder

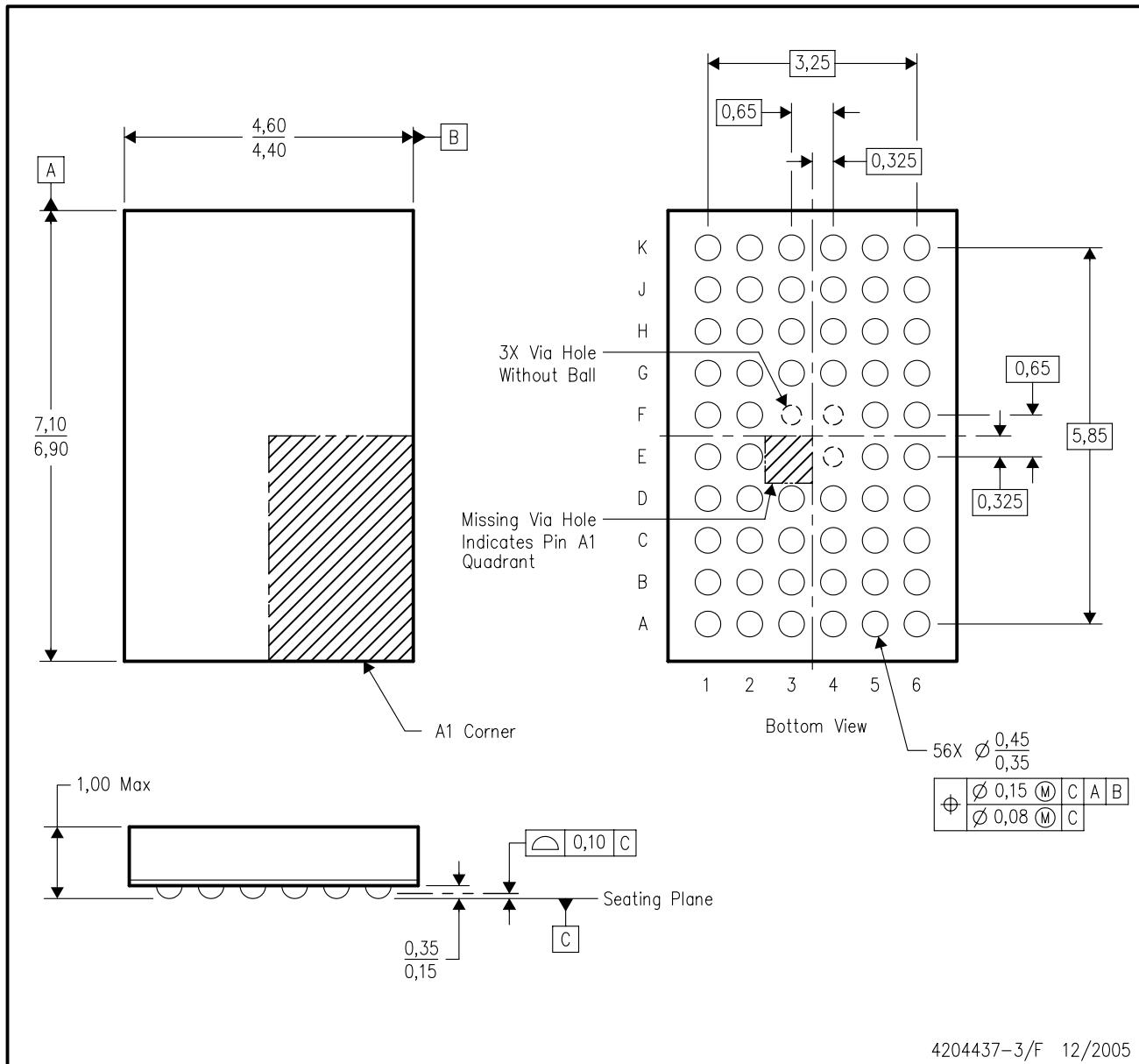
temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



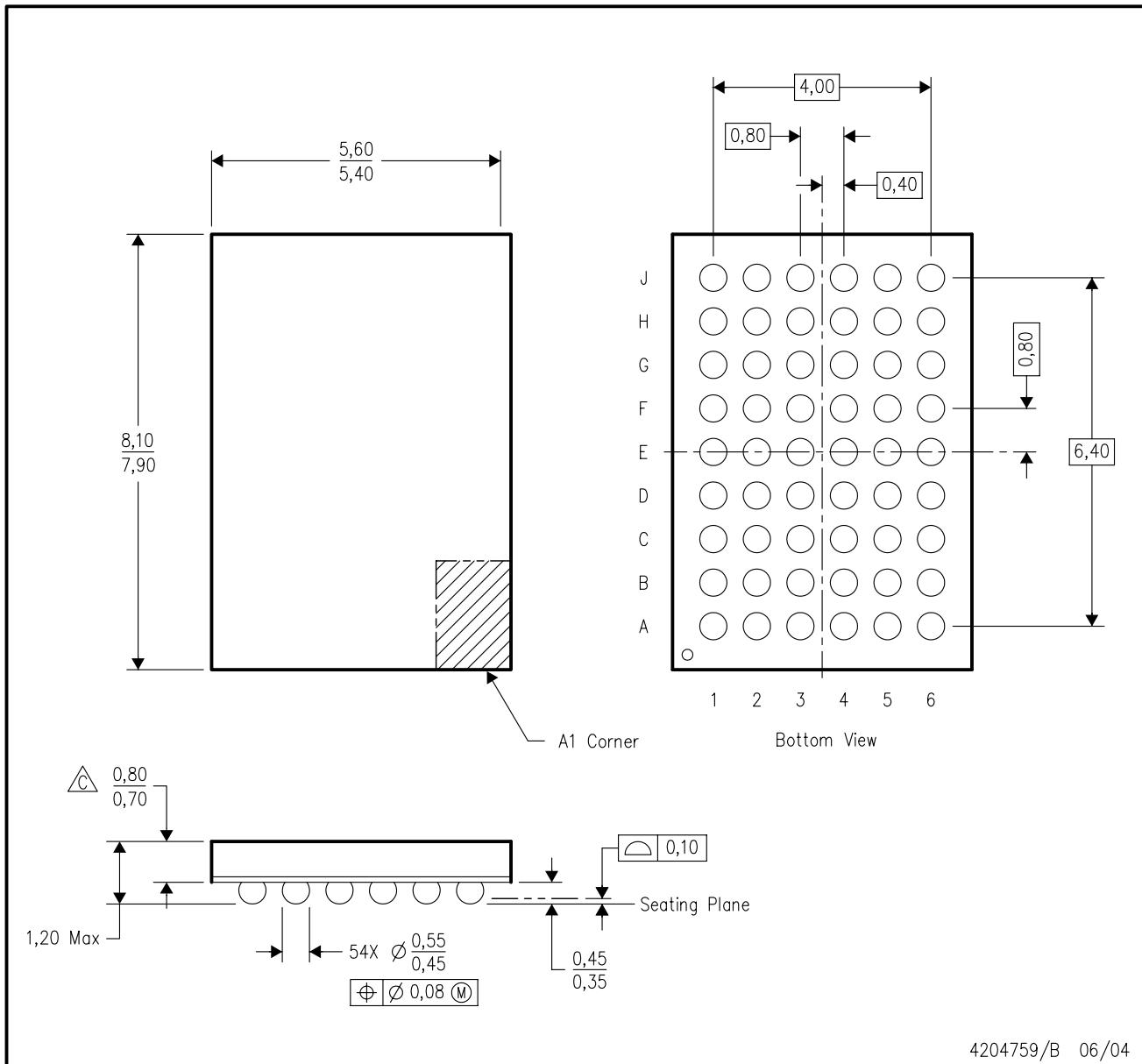
4204437-3/F 12/2005

NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Falls within JEDEC MO-225 variation BA.
- This package is lead-free. Refer to the 56 QGL package (drawing 4200583) for tin-lead (SnPb).

GRD (R-PBGA-N54)

PLASTIC BALL GRID ARRAY



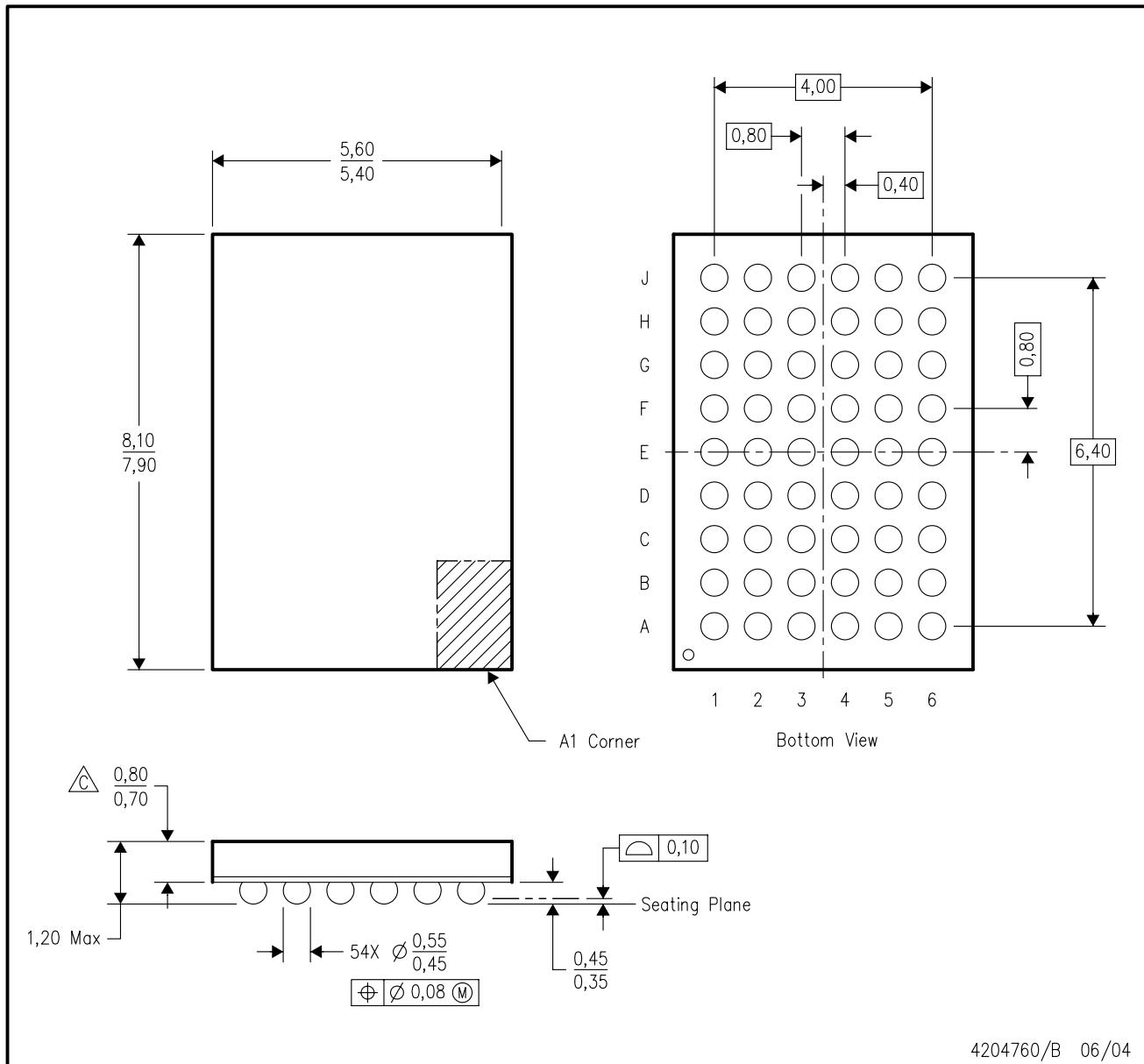
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

Falls within JEDEC MO-205 variation DD.

D. This package is tin-lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead-free.

ZRD (R-PBGA-N54)

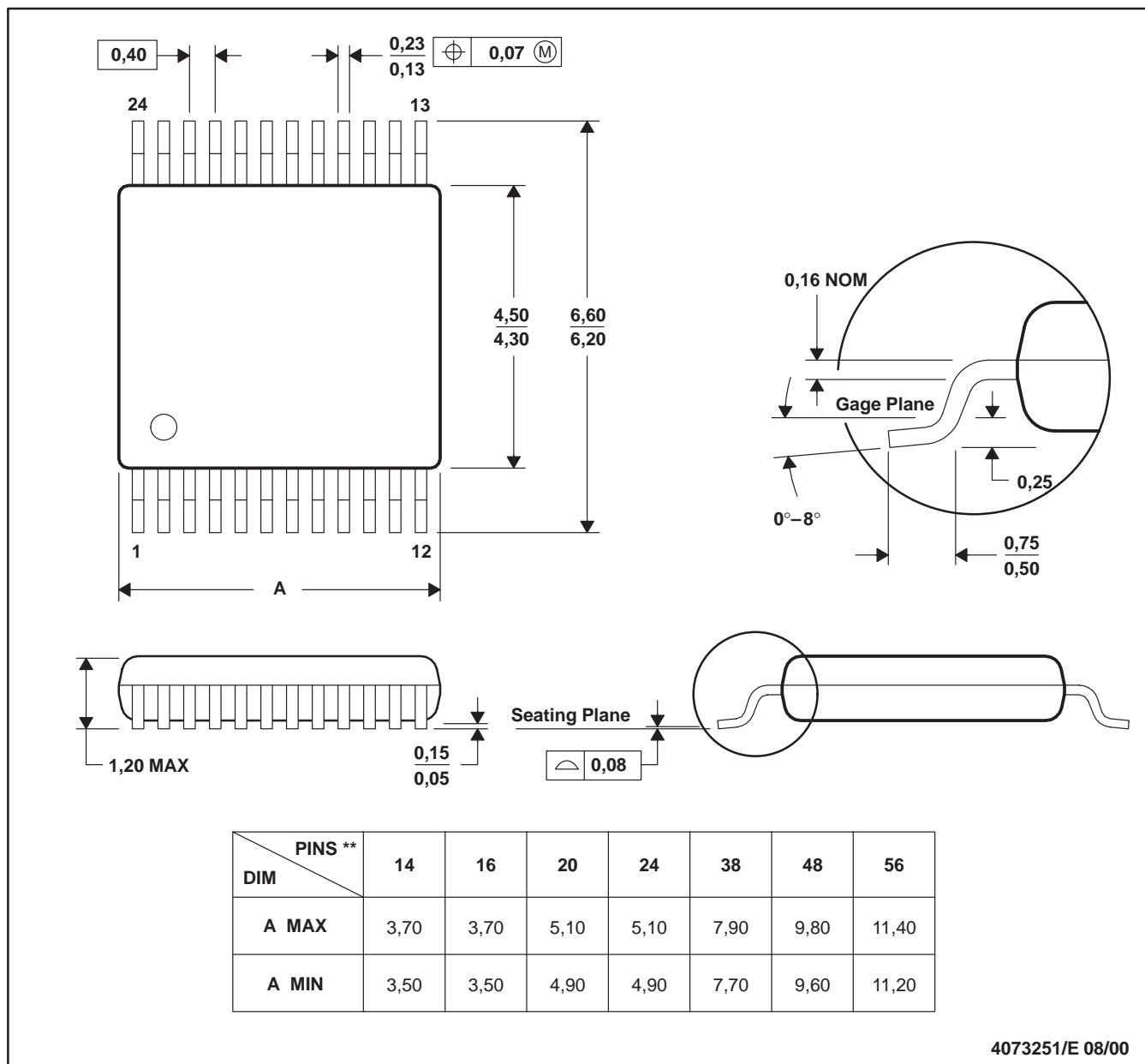
PLASTIC BALL GRID ARRAY



DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

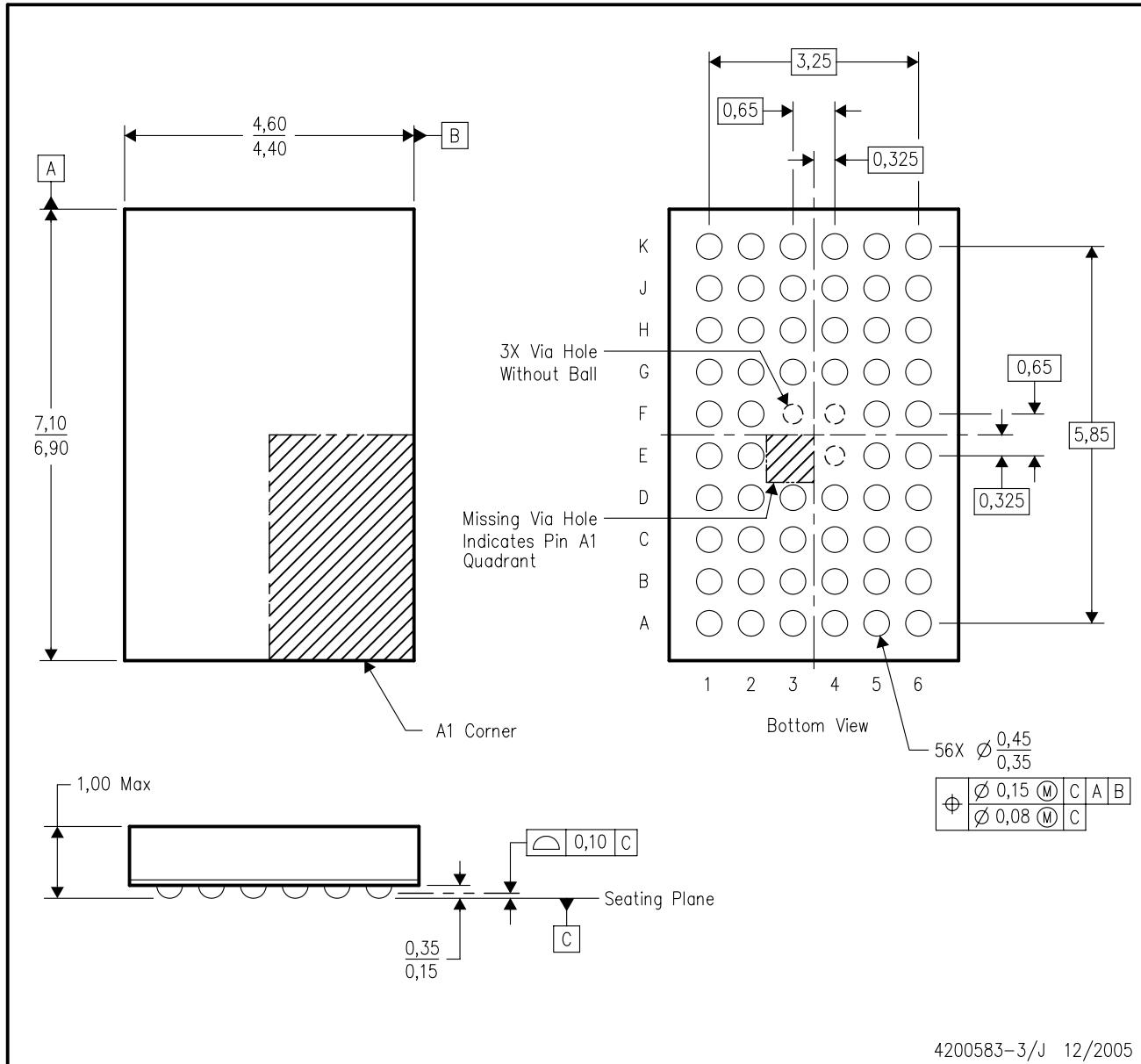
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



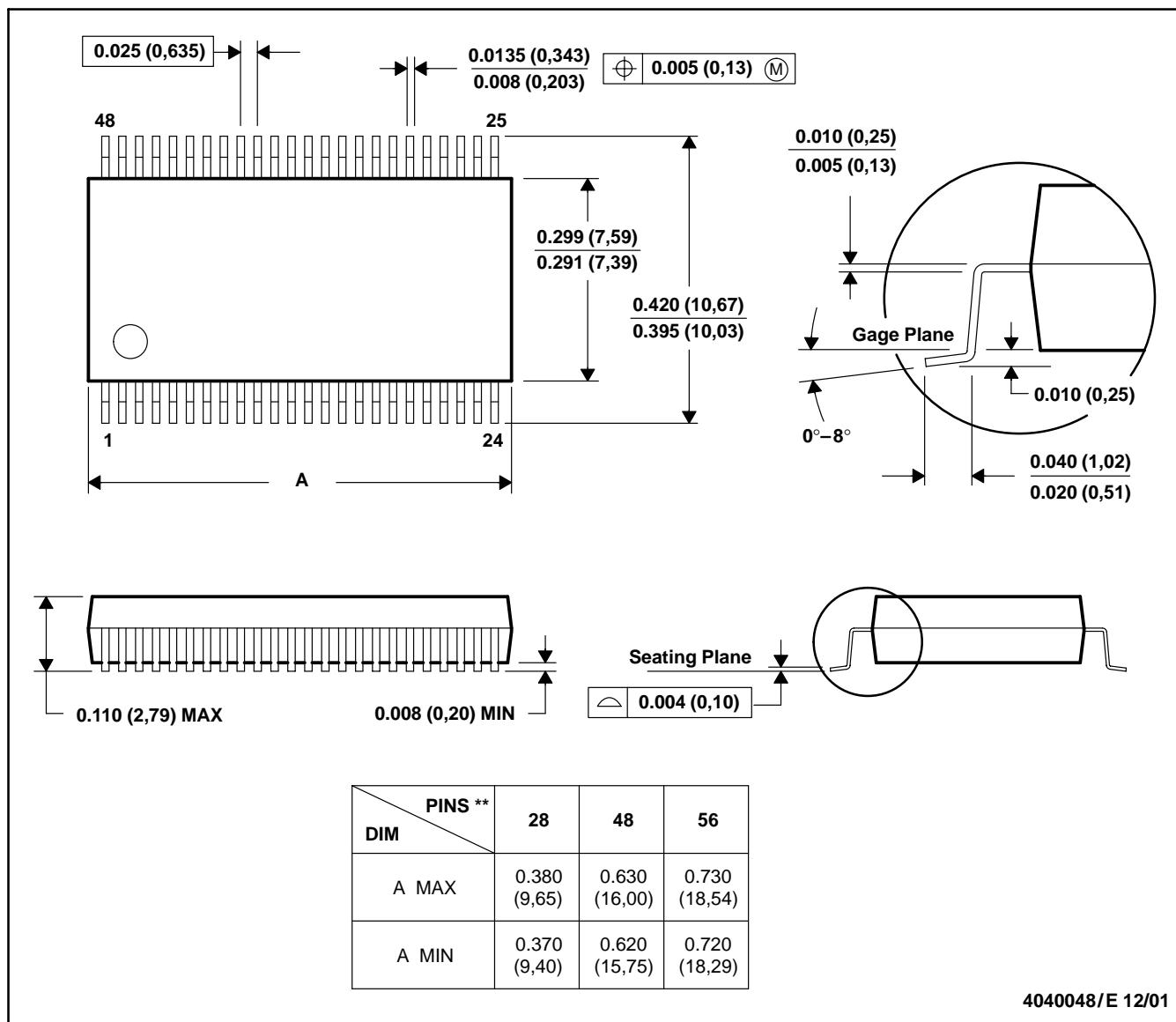
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC M0-225 variation BA.
D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

4200583-3/J 12/2005

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

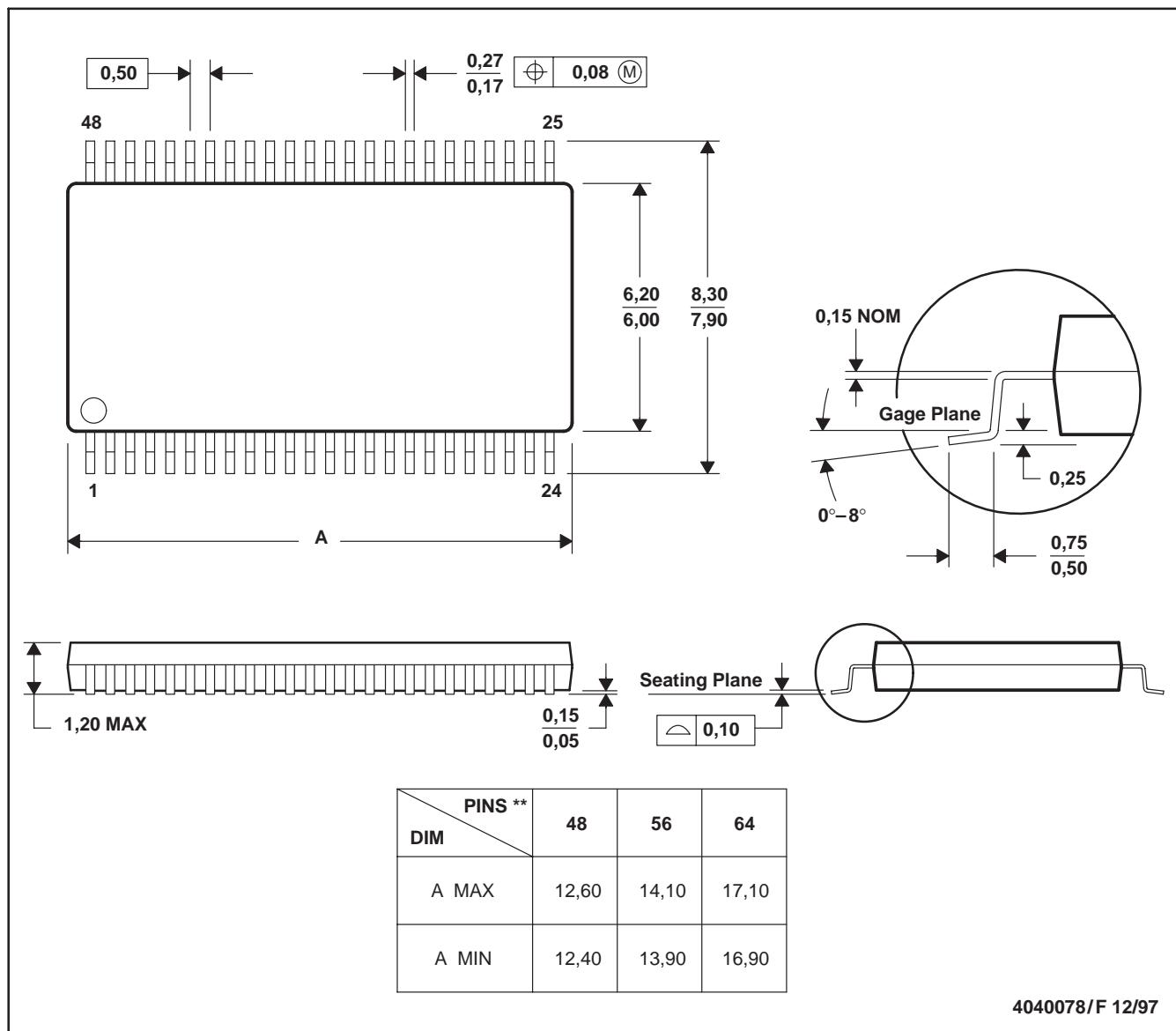


NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| Products | | Applications | |
|------------------|------------------------|---------------------|--|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Interface | interface.ti.com | Digital Control | www.ti.com/digitalcontrol |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| | | Telephony | www.ti.com/telephony |
| | | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2006, Texas Instruments Incorporated