DS33Z41DK
Ethernet Transport Design Kit

www.maxim-ic.com

GENERAL DESCRIPTION

The DS33Z41 design kit is an easy-to-use evaluation board for the DS33Z41 Ethernet transport-over-serial link device. The DS33Z41DK is intended to be used with a resource card for the serial link. The serial link resource cards are complete with transceivers, transformers, and network connections. Dallas' ChipView software is provided with the design kit, giving point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal, queue overflow, Ethernet link, Tx/Rx, and interrupt status.

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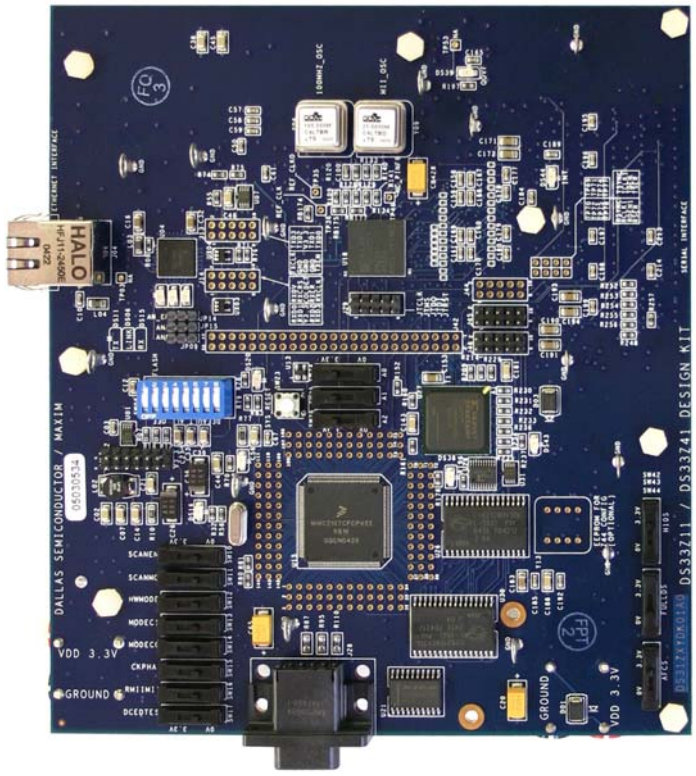
ORDERING INFORMATION

PART	DESCRIPTION
DS33Z41DK	DS33Z41 demo card, T1/E1 transceiver resource card included

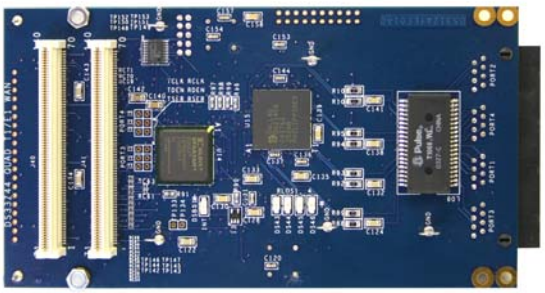


FEATURES

- **Demonstrates Key Functions of DS33Z41 Ethernet Transport Chipset**
- **Includes Resource Card for DS21458 T1/E1 quad Transceiver with Transformers, RJ48 Network Connectors, and Termination**
- **Provides Support for Hardware and Software Modes**
- **On-Board MMC2107 Processor and ChipView Software Provide Point-and-Click Access to the DS33Z41 Register Set**
- **All DS33Z41 Interface Pins are Easily Accessible for External Data Source/Sink**
- **LEDs for Loss-of-Signal, Queue Overflow, Ethernet Link, Tx/Rx, and Interrupt Status**
- **Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs**

DESIGN KIT CONTENTS

- DS33Z41DK Main Board
- Quad-Port Serial Card with DS21458 T1/E1
- CD_ROM
  - ChipView Software and Manual
  - DS33Z41DK Data Sheet
  - Configuration Files



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COMPONENT LIST

Table 1 shows the component list for the DS33Z44 and DS33Z11/DS33Z41 design kits and resource cards. This BOM contains the part listing for five boards. These boards are the DS33Z41DK, DS33Z44DK, DS21458RC, DS3174RC, and DS2155-DS21348-DS3170RC. Each reference designator is only used once. For example, U18 only appears on the DS33Z41DK and is not used on any of the other boards. See Table 2.

Table 1. Component List (Decoupling Caps Not Shown)

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
U18	1	ELITE 10/100 ETHERNET TRANSPORT OVER SERIAL LINK 14X14 CSBGA 169 PIN	Dallas Semiconductor	DS33Z41
U20	1	3.3V T1.E1.J1 QUAD TRANSCEIVER 0-70C 256P BGA	Dallas Semiconductor	DS21458
U22	1	QUAD 10/100 ETHERNET EXTENSION TO WAN 17X17 PBGA 256 PIN	Dallas Semiconductor	DS33Z44
U23	1	DS3/E3 SCT, 11X11 CSBGA, 100 PIN	Dallas Semiconductor	DS3170
U24	1	T1/E1/J1 XCVR 100P QFP 0-70C	Dallas Semiconductor	DS2156L
U25	1	3.3V LIU	Dallas Semiconductor	DS21348
UB08	1	QUAD TRIPLE DUAL SINGLE ATM PACKET PHYS FOR DS3 E3 STS1 0-70C 400P BGA	Dallas Semiconductor	DS3184
U01, U09	2	SOIC 8PIN STEP-UP DC-DC CONVERTER 0.5A LIMIT	Maxim	MAX1675EUA
U07, U11	2	8-Pin µMAX/SOIC 1.8V or Adj	Maxim	MAX1792EUA18
U13, UB01	2	MICROPROCESSOR VOLTAGE MONITOR, 2.93V RESET, 4PIN SOT143	Maxim	MAX811SEUS-T
U21, UB07	2	Dual RS-232 transceivers with 3.3V/5V internal capacitors	MAXIM	NA
U31, UB06, UB11	3	8-Pin µMAX/SOIC 2.5V or Adj	Maxim	MAX1792EUA25
C11, C13, C16, C25, C27, C31–C35, C37, C41, C47, CB10, CB63, CB114, CB128, CB164, CB496	19	1206 CERAM 10uF 10V 20%	Panasonic	ECJ-3YB1A106M
CB390, CB391, CB395, CB396	4	1206 CERAM 0.1uF 25V 10%	Panasonic	ECJ-3VB1E104K
D01–D03, D05, DB03–DB05	7	SCHOTTKY DIODE, 1 AMP 40 VOLT	International Rectifier	10BQ040
DS01, DS07, DS10–DS12, DS17, DS20	7	LED, AMBER, SMD	Panasonic	LN1451C
DS02, DS03, DS09, DS14, DS15	5	L_LED, GREEN, SMD	Panasonic	LN1351C
DS04–DS06, DS08, DS13, DS16, DS18, DS27, DS28, DS35, DS37, DS38, DS40	13	LED, RED, SMD	Panasonic	LN1251C
DS19, DS43	2	LED, GREEN, SMD	Panasonic	LN1351C
DS21–DS26, DS30, DS32–DS34, DS36, DS39, DS41, DS42, DS44–DS48	19	L_LED, RED, SMD	Panasonic	LN1251C
GND_TP01–GND_TP07, GND_TP09-–GND_TP44, GND_TP46–GND_TP68, GND_TPB01–GND_TPB10	76	STANDARD GROUND CLIP	KEYSTONE	4954
H1–H8, H17–H19	8	KIT, 4-40 HARDWARE, .50 NYLON STANDOFF AND NYLON HEX-NUT	NA	Lab Stock

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
H9–H16	16	KIT, 4-40 HARDWARE, 1.12 NYLON STANDOFF AND NYLON HEX-NUT (1.12 STANDOFF PN = 4807K-ND)	NA	Lab Stock
J01–J05	5	CONNECTOR, FASTJACK SINGLE, 8 PIN	Halo Electronics	HFJ11-2450E
J06, J41	2	100 MIL 2*7 POS JUMPER	NA	Lab Stock
J07–J12	6	RECEPTACLE, SMD, 140 PIN, .8MM, 2 ROW VERTICAL	AMP	5-179010-6
J13–J22	10	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT DO NOT POPLUATE	NA	Lab Stock
J23, J29, J32, J38, J39, J43, J44, J47, JB07	9	L_TERMINAL STRIP, SHROUDED, 10 PIN, DUAL ROW, VERT	3M Electronics	2510-6002UB
J24, J30, J31, J33	4	100 MIL 2 POS JUMPER	NA	Lab Stock
J25, J26, J45, J46	4	TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	NA	Lab Stock
J27, J42	2	CONN 50 PIN, 2 ROW, POSTS VERT, MOTHERBOARD FOOTPRINT	SAMTEC	TSW-125-07-T-D
J28, J36	2	L_CONN, DB9 RA, LONG CASE	AMP	747459-1
J48, J54, JB01	3	SOCKET, BANANA PLUG, HORIZONTAL, BLACK	Mouser Electronics	164-6218
J49–J52	4	CONNECTOR BNC 75 OHM VERTICAL 5PIN	Cambridge	CP-BNCPC-004
J53, JB02, JB08	3	SOCKET, BANANA PLUG, HORIZONTAL, RED	Mouser Electronics	164-6219
J55, JB11	2	L_RJ48 8 PIN SINGLE PORT CONNECTOR	MOLEX	15-43-8588
J56–J59, J61, J63	6	CONNECTOR BNC 75 OHM RA 5PIN	Trompetor	UCBJR220
J60, J62, J64, J65	4	CONNECTOR BNC RA 5PIN	Trompetor	UCBJR220
JB05, JB06, JB09, JB10, JB13, JB14	6	PLUG, SMD, 140 PIN, .8MM, 2 ROW VERTICAL	AMP	179031-6
JB12	1	RA RJ45 8PIN 4PORT JACK	MOL	43223-8140
JP01–JP19	19	100 MIL 3 POS JUMPER	NA	NA
L01, L03–L08, LB01, LB02	9	FERRITE 3A 100 OHM AT 100 MHZ 1206 SMD	Steward	HI1206N101R-00
L02, L09	2	INDUCTOR 22.0uH 2PIN SMT 20%	Coiltronics	UP1B-220
L10	1	XFMR 1-2CT XMIT, 1-1CT RCV, 40P WIDE SOIC	Pulse	T1068
R01, R02, RB10, RB11, RB18, RB19, RB22, RB23, RB26, RB27	10	RES 0603 54.9 Ohm 1/16W 1%	Panasonic	ERJ-3EKF54R9V
R03, R04, RB12, RB13, RB20, RB21, RB24, RB25, RB28, RB29	10	RES 0603 49.9 Ohm 1/16W 1%	Panasonic	ERJ-3EKF49R9V
R05, R06, R08, R09, R11	5	RES 0603 10.0K Ohm 1/16W 1% - Must be 1% tolerance	Panasonic	ERJ-3EKF1002V
R07, R12, R16, R79, R160, R244, R248, R250, R251, R254, R255, RB126, RB143, RB147, RB150, RB157	16	RES 0603 1.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ102V
R10, R107	2	RES 1206 5.6 Ohm 1/8W 5%	Panasonic	ERJ-8GEYJ5R6V
R132, R137, R142, R144, R156, RB194, RB208, RB227	8	L_RES 0603 0 Ohm 1/16W 1%	AVX	CJ10-000F

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R13–R15, R18–R20, R22, R23, R29, R30, RB01, RB03, RB07, RB09, RB15–RB17, RB30–RB32, RB34–RB38, RB41, RB44, RB47, RB48, RB50–RB52, B55, RB60, RB62, RB72, RB73, RB75, RB80, RB82	40	RES 0603 5.1K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ512V
R17, R21, R25–R28, R31, R55, R57–R59, R71, R74–R76, R83, R96–R102, R105, R106, R109, R111, R112, R115–R117, R120, R122–R126, R128, R133, R134, R140, R141, RB61, RB96, RB97, RB99, RB100, RB102–RB110, RB112, RB114–RB119, RB121, RB123–RB125, RB127, RB128, RB130, RB131, RB133, RB135–RB138, RB145, RB148, RB149, RB160, RB161, RB164, RB165, RB167–RB171, RB173–RB181, RB184, RB187, RB311, RB320, RB335, RB339, RB359	104	RES 0603 30 Ohm 1/16W	Panasonic	ERJ-3GEYJ300V
R171, R172, R174, R175, R190, R191, R240, R241	8	L_RES 0805 0.0 Ohm 1/10W 5%	Panasonic	ERJ-6GEY0R00V
R198–R200, R210–R213, RB306, RB325, RB326	10	RES 0603 332 Ohm 1/16W 1%	Panasonic	ERJ-3EKF3320V
R201–R208, RB321–RB324, RB327–RB330	16	RES 1206 0 Ohm 1/8W 5%	Panasonic	ERJ-8GEYJ0R00V
R239, RB349	2	RES 0805 51.1 Ohm 1/10W 1%	Panasonic	ERJ-6ENF51R1V
R24, R114, R197, RB14, RB33, RB40, RB42, RB43, RB49, RB53, RB54, RB57–RB59, RB71, RB77, RB78, RB152–RB156, RB221, RB234, RB251, RB284, RB304, RB331, RB332, RB342, RB344, RB350, RB354, RB360	34	L_RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V
R242, R243, RB144, RB166, RB355–RB358, RB368–RB371	12	RES 0603 51 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ510V
R32, R70, R78, R161, R176, R194, R195, R237, R238, RB129, RB134, RB146, RB193	13	RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V
R33–R54, R60–R69, R72, R73, R131, R136, R143, R147, R150, R154, R158, R163, R166, R169, R173, R178–R189, R215–R228, RB89–RB95, RB101, RB188–RB191, RB196–RB199, RB202–RB205, RB210–RB213, RB216–RB219, RB223–RB226, RB230–RB233, RB239–RB242, RB244–RB249, RB252–RB260, RB265–RB268, RB270-RB282, RB289–RB297	152	RES 0402 30 Ohm 1/16W 5%	Panasonic	ERJ-2GEJ300X
R56, R90	2	RES 0603 1.0M Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ105V
R77, RB159	2	L_RES 1206 0 Ohm 1/8W 5%	Panasonic	ERJ-8GEYJ0R00V
R80, R81, R84, R87, R89, R91–R93, R95, R108, R110, R118, R127, R152, R153, R196, R209, R214, R229–R236, RB200, RB237, RB238, RB263, RB264, RB286, RB287, RB300, RB301, RB333, RB364	37	RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R85, R88, R94, R104, R113, RB02, RB04–RB06, RB08, RB39, RB45, RB46, RB56, RB63–RB70, RB76, RB83, RB98, RB183, RB185, RB192, RB209, RB228, RB302, RB303, RB305, RB338, RB340, RB341, RB346–RB348, RB351–RB353, RB361–RB363, RB365–RB367	48	RES 0603 2.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ202V
R86, R103, R119, R121, R129, R130, R135, R138, R139, R145, R146, R149, R151, R157, R162, R164, R167, R168, R170, R177, R192, R193, R245-R247, R249, R252, R253, R256, R257, RB74, RB79, RB132, RB139-RB141, RB151, RB162, RB163, RB172, RB182, RB186, RB206, RB207, RB214, RB215, RB220, RB222, RB229, RB235, RB236, RB243, RB250, RB261, RB262, RB269, RB308–RB310, RB343, RB345	61	L_RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V
RB201, RB285	2	RES 0805 330 Ohm 1/10W 5%	Panasonic	ERJ-6GEYJ331V
RB283	1	RES 0603 10K Ohm 1/10W 5% - SEE SPECIAL INSTRUCTIONS	Panasonic	603_ERJ-3GEYJ103V
RB298, RB299, RB312–RB319, RB336, RB337	12	RES 0805 61.9 Ohm 1/10W 1%	Panasonic	ERJ-6ENF61R9V
RB81, RB84–RB88, RB111, RB113, RB120, RB122	10	RES 0603 DO NOT POPULATE	NA	NA
SW01–SW05, SW08–SW21, SW24–SW26, SW29–SW31, SW33–SW44	37	L_SWITCH, SP3T SLIDE, 4PIN TH	Tyco	3-1437575-3
SW06, SW22	2	L_SWITH 8POS 16PIN DIP LOW PROFILE	AMP	435668-7
SW07, SW23	2	SWITCH MOM 4PIN SINGLE POLE	Panasonic	EVQPAE04M
SW27, SW28, SW32	3	L_DIPSWITCH, 10 POS	AMP	435668-9
T01, T03	2	XFMR 16P SMT	Pulse	TX1099
T02, TB01	2	XFMR, OCTAL T3/E3, 1 TO 2, SMT 32 PIN	Pulse	T3049
TP01–TP78, TPB01, TPB02	80	TESTPOINT, 1 PLATED HOLE, DO NOT STUFF	NA	NA
U02–U06	5	IC, DsPHYTER11-SINGLE 10/100 ETHERNET TRANSCEIVER, 65 PIN LLP	National Semiconductor	DP83847ALQA56A
U08, U12, U29	3	1MBit Flash based config mem	Avnet	XCF01SV020C
U10	1	XILINX SPARTAN xc200 2.5V FPGA,256 PIN BGA	Xilinx	XC2S200-5FG256C
U14, U26, U30, UB05	4	CYPRESS SRAM, LAB STOCK	NA	NA
U15, U19	2	mmc2107 processor	Motorola	MMC2107
U16, U27	2	XILINX SPARTAN 2.5V FPGA,256 PIN BGA	Xilinx	XC2S50-5FG256C
U17, U28, U32	3	10 pin res pack, 10K ohm	NA	NA
UB02, UB03, UB04	3	100 PIN CPLD	XILINX	XC95144XL-10TQ100C
UB09, UB10	2	SYNCHRONOUS DRAM, 1MEGX32X4 BANKS, TSOP 86 PIN	Micron	MT48LC4M32B2TG-7

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
UX01–UX12, UXB02–UXB04, UXB06–UXB08	18	HIGH SPEED BUFFER	Fairchild	NC7SZ86
UXB01, UXB05	2	HIGH SPEED INVERTER	Fairchild	NC7SZ86
X01, X02	2	XTAL LOW PROFILE 8.0MHZ	ECL	EC1-8.000M
Y01, Y09	2	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 25.000 MHZ, Low Jitter required for PHY	SaRonix	NTH089AA3-25.000
Y02, Y13	2	SPI SERIAL EEPROM 16K 8 PIN DIP 2.7V NEEDS SOCKET	Atmel	AT25160A-10PI-2.7
Y03	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 2.048 MHZ	SaRonix	NTH039A3-2.0480
Y05, Y06	2	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 100.000 MHZ	SaRonix	NTH089A3-100.0000
Y07	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 44.736 MHZ	SaRonix	NTH089AA3-44.736
Y08	1	OSCILLATOR, CRYSTAL CLOCK, 5.0V - 44.736 MHZ	SaRonix	NTH089AA-44.736
YB02	1	L_OSCILLATOR, CRYSTAL CLOCK, 3.3V - 2.048 MHZ	SaRonix	NTH039A3-2.0480

Figure 1. System Floorplan

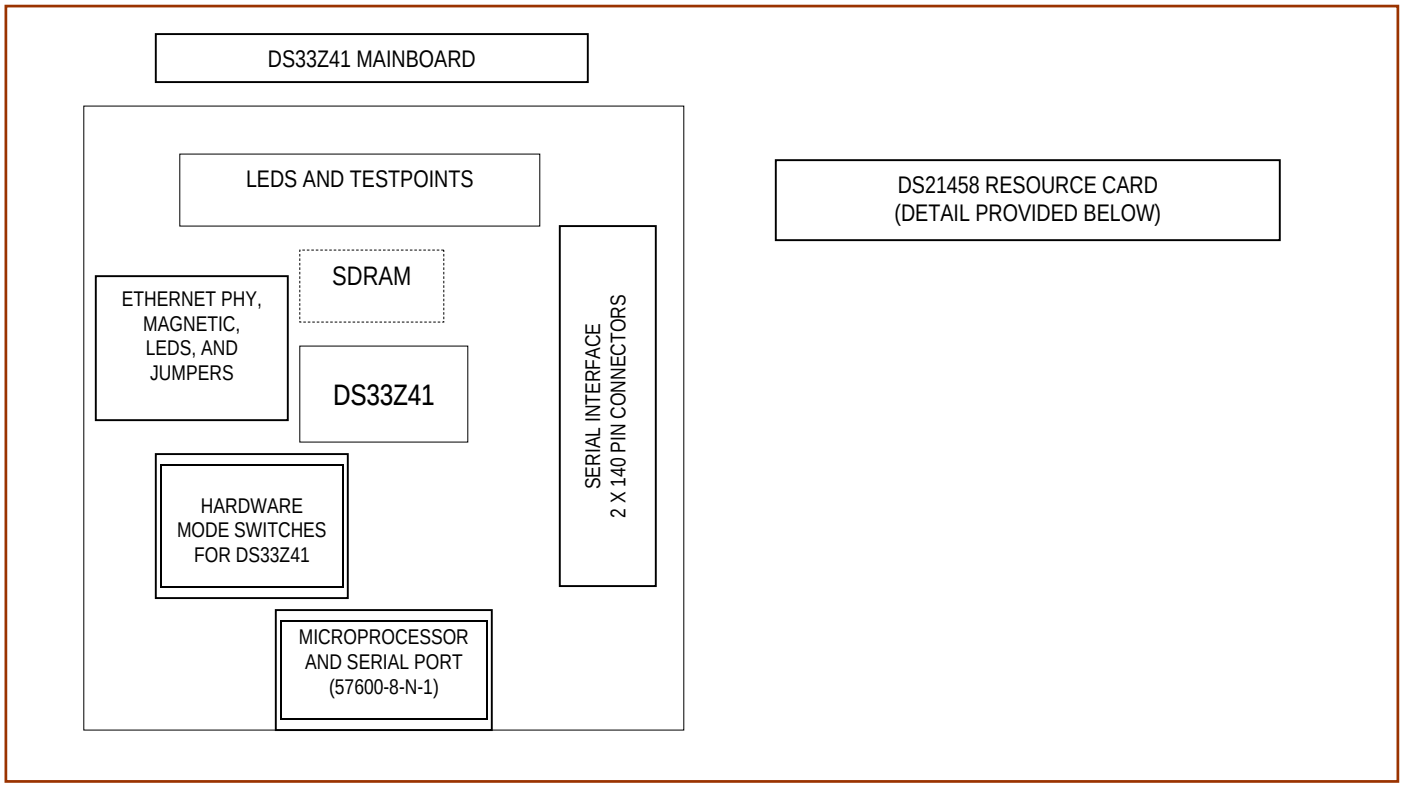
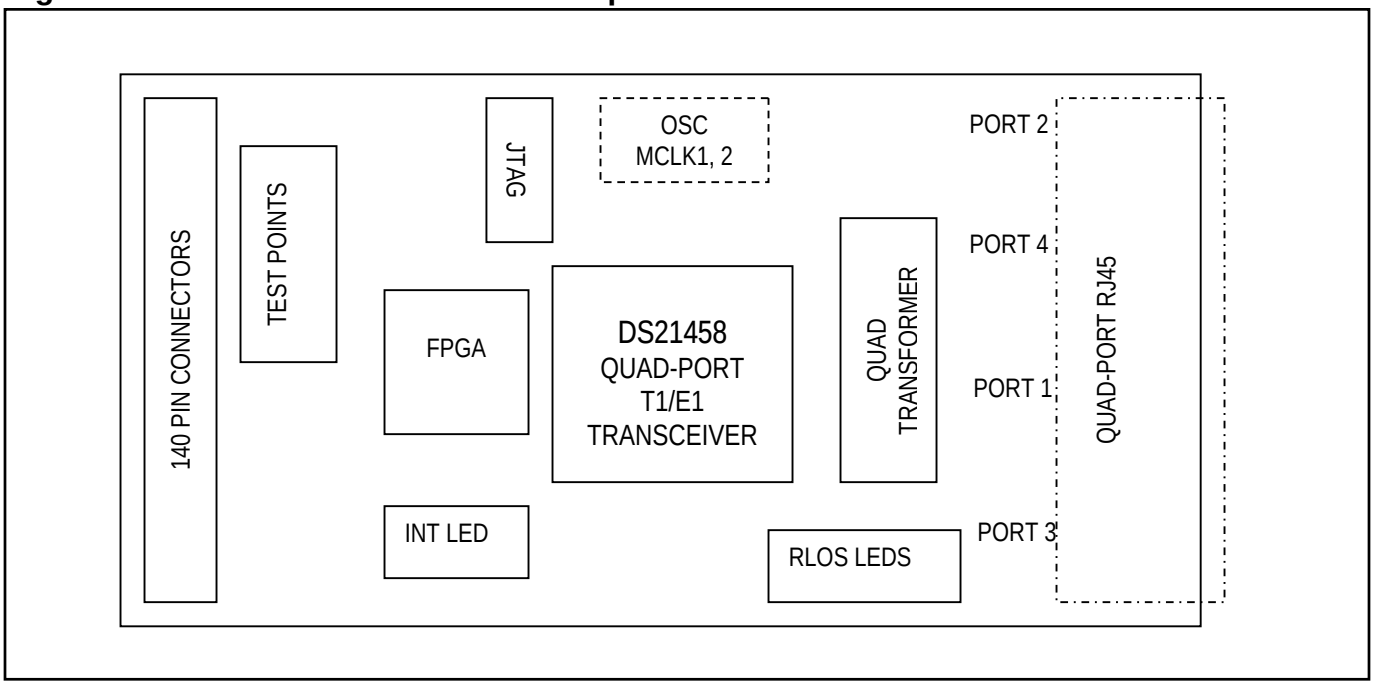


Figure 2 shows the DS21458 quad T1/E1 PC board floorplan. The current configuration is to populate oscillators for MCLK1 with a 8.192MHz oscillator. Testpoints for port 3 and port 4 are provided on the WAN card, and testpoints for ports 1 and 2 are provided on the motherboard.

Figure 2. DS21458 Resource Card Floorplan



PC BOARD ERRATA

- Silkscreen for JTAG connector signal descriptions is incorrect on the quad T1/E1 card. This should be corrected with an adhesive label.

FILE LOCATIONS

This design kit relies upon several supporting files, which are provided on the CD and are available as a zip file from the Maxim website at www.maxim-ic.com/DS33Z41DK.

All locations are given relative to the top directory of the CD/zip file.

- DS33Z41 register definition files and configuration files:
    - .\cfg_demo_gui\DS33Z41_cfg_demo_gui\DS33Z41.def
    - .\DS33Z41_cfg_demo_gui\SU_LI_PORT1.def
    - .\DS33Z41_cfg_demo_gui\z41_basic.mfg

- DS21458 register definition files and configuration files:
    - .\DS33Z41_cfg_demo_gui\Qt1e1_DS21458\DS21458RC_FPGA.def
    - .\DS33Z41_cfg_demo_gui\Qt1e1_DS21458\DS21458RC.def
    - .\DS33Z41_cfg_demo_gui\Qt1e1_DS21458\T1_IBO_ LoopTime.ini
    - .\DS33Z41_cfg_demo_gui\Qt1e1_DS21458\T1_IBO_ SourceTime.ini
    - .\DS33Z41_cfg_demo_gui\Qt1e1_DS21458\E1_CRC_HDB3_IBO_ SourceTime.ini
    - .\DS33Z41_cfg_demo_gui\Qt1e1_DS21458\E1_CRC_HDB3_IBO_ LoopTime.ini

BASIC OPERATION

Powering Up the Design Kit

- Attach DS21458 resource card to main board.
- Connect PCB 3.3V and GND banana plugs to power supply. At power-up the system should draw approximately 1A.
- Set switches for software mode as described in Table 2 (short description follows).
  - Top left bank: All low, except for MODEC0, which is high.
  - Top right bank: A2, A1, A0 in mid position, SCANTRI low
  - Bottom Bank: All high (AFCS, FULLDS, H1OS)

General

- Upon power-up, the processor FPGA Status LEDs (DS43 green) will be lit. Interrupt LEDs (DS44 red) will not be lit. DS33Z11 Queue overflow LEDs (DS39 red) will not be lit. PHY LINK LED (DS06 green) should be lit if the Ethernet is connected.

Following are several basic system initializations. These initializations assume that there are two boards present (DS33Z41 and / or DS33R41). A note is provided below to assist with using a system that only contains one board.

Basic DS33Z41 Initialization (Used for All Quick Setups)

This section covers four basic methods for configuring the DS33Z41. Any one of these initializations can be used with the following Quick Setup examples:

1. Upon power-up, the on-board device driver provides a basic configuration for the DS33Z41 and attached serial cards. This enables traffic to pass from the Ethernet port to the serial port. Consult the device driver documentation for further details. Device driver behavior is dependant upon jumper settings, which are detailed in Table 2.
2. Launch ChipView.exe and select *Register View.* When prompted for a definition file, pick the file named **DS33Z41.def**. Following this load the definition file named **DS21458RC_FPGA.def**
3. Hardware Mode is not available with this DK
4. EEPROM mode is not available with this DK.
5. Ethernet Traffic generation and analysis:
   a. Using a patch cable, connect the Ethernet connector to an ordinary PC, or network test equipment. This should cause the link LED to turn on.
   b. Although ping is mentioned it is *not* recommended. The ping command goes through the computers TCPIP stack, and will sometimes will not be sent out the PCs network connector (i.e. if the PCs ARP cache is out of date). Additionally ping requires two PCs, as a PC can not ping itself (a local ping gets sent to 'localhost' instead of out the connector). With that said – ping is still a valuable test once the prototyping stage is complete.
   c. Generation and capture of arbitrary (raw) packets can be accomplished using CommView. A time-limited demo is available at the website www.tamos.com/products/commview.
   d. Ethereal is an excellent (and free) packet capture utility. Download is available at www.ethereal.com.
   e. Adding additional Ethernet ports to a PC is rather simple when a USB-to-Ethernet adapter is used. This allows for end-to-end testing using a single PC. When using two adapters the PC will have a different IP address for each adapter. Test equipment will allow selection of either adapter. Operating system based network traffic will be sent out the default adapter, usually this is the adapter that has recently had connection to a real network.

Quick Setup #1 (Device Driver + DS21458 T1/E1)

- Select TCLK source for the DS21458 resource card. If this is the only DS33Z41 in the system (i.e. used in loopback) then select TCLK=MCLK. From Table 2, this requires that the J45.3+J45.4 jumper is not installed. If this is the second DS33Z41 in the system select TCLK=RCLK, which requires that J45.3+J45.4 jumper is installed. Note: The TCLK source settings can be changed using the driver interface, which is described below.
- Complete the hardware configuration and one of the basic DS33Z41 configurations as described in the previous section.
- At this point any packets sent to the DS33Z41 are sent out the T1/E1 ports. Incoming Ethernet packets should cause the RX LED to blink, transmitted packets cause the TX LED should also blink.
- Launch ChipView.exe, select Register View
- To interact with the device driver go to ChipView and select from the drop down menu:
  - Tools→Plugins→Load Plugins. When asked if DLLs have already registered select yes
  - Select Tools→Plugins→DS33Z41/11/41 Device Driver Demo
  - A new form called 'Zchip Configuration' appears
  - Preload basic configuration for the GUI by selecting File→Load Settings (in the 'Zchip Configuration' form). Select the file named 'basic_Config.eset'

Quick Setup #2 (DS21458 T1/E1, Register Based)

1. Disable device drivers and callbacks – remove all jumpers from J45 header. Press the reset button, or cycle power on the board to restore the system to its power-on state.
2. Configure the DS33Z41. After the definition files load, go to the File menu and select File→Memory Config File→Load .MFG file. When prompted, select the file named **z41_basic.mfg**.
3. Set the DS2148 serial card for IBO mode. Using the menu marked 'Def File Selection' switch to the DS21458RC_FPGA def file. Set the register MO+CLK to 0x47.
4. Configure the DS21458. Go to the File menu and select File→Register INI File→Load .INI file. When prompted, select either the file named **T1_IBO_ SourceTime.ini** (TCLK=MCLK) or **T1_IBO_ LoopTime.ini** (TCLK=RCLK). Set one board to be the source of network timing (TCLK=MCLK), and one board to follow the timing source (TCLK=RCLK). The RLOS LEDs should go out when this step is complete for both boards.
5. Additional setup (for both boards):
   - Switch to the DS33Z41 def file and set the following:
     - Set the GL.IMUXCN register to 0x0F (both systems)
     - Set GL.IMUXC register to 0x00 then to 0x82 (both systems)
     - Check GL.IMUXSS register. They should be 0xFF on both systems
     - Return to GL.IMUXCN and set the bits RXE and SENDE
     - The system should now be configured to pass Ethernet traffic into one system and out of the other.

Configuration Note: Using a Single System

The DS33Z41 is intended for use in a system with a DS33Z41 at each end. However, the system may be tested with only a single DS33Z41 system. This configuration requires that the DS21458 serial link is in loopback, either internal loopback or hardware loopback may be used. In this configuration any packets sent to the Ethernet side will be echoed back. In this configuration the setting for DS21458 TCLK=MCLK should be used (see Table 2) and steps intended for the "second" system may be ignored.

Configuration Note: A Mixing Device Driver and Register-Based Modes

Quick setup #1 discuses device driver based operation. Quick setup #2 discusses register based operation. To some extent both modes may be used simultaneously to gain insight to device configuration. For example:

- In register view click "Read All" this causes all registers to be read, changed registers turn green.
- Switch to the device driver GUI, select one of the forms, make changes, and click "send configuration"
- Switch back to register view and click "Read All". Newly changed registers will turn green, showing which registers changed as a result of settings selected in the device driver GUI

A second type of device driver/register-based configuration is to power the board with the device drivers enabled, and then remove the jumpers that enable the device drivers. This allows for a fast initial configuration.

CONFIGURATION SWITCHES AND JUMPERS

The DS33Z41DK has several configuration switches, banana plugs, oscillators, and jumpers. Table 2 provides a description of these signals, given in order of appearance on the PC board (going from left to right, top to bottom).

Table 2. Main Board PC Board Configuration

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING		DESCRIPTION
		SW MODE	HW MODE	
J45.9 + J45.10	Reserved	Not installed	—	This jumper is not for use with the DS33Z41 design kit. Pin J25.10 has been removed to prevent accidental installation
J45.7 + J45.8	Enable device driver	User decision	—	When installed the device driver will configure the DS33Z41 and the Transceiver during power-up.
J45.5 + J45.6	Enable callbacks	User decision	—	When installed the driver will respond to interrupts
J45.3 + J45.4	Select TCLK source	User decision	—	When installed the driver will configure DS21458 TCLK to be sourced from DS21458 RCLK. When not installed DS21458 scaled MCLK is used. This setting is only applied at reset. If only one board is used select TCLK = MCLK.
GROUND (banana plug)	Power supply ground	—	—	System Ground. Always connected to power supply.
VDD 3.3V (banana plug)	Power supply VDD	—	—	System VDD. Always connected to power supply.
OnCe	BDM	—	—	Debug connector for processor
DCEDTES (3pos switch)	DS33Z41 mode pin; DTE/DCE selection	LOW	LOW	Low for DTE
RMIIMII (3pos switch)	DS33Z41 mode pin	LOW	LOW	High for RMII, low for MII
CKPHA (3pos switch)	DS33Z41 mode pin	LOW	LOW	SPI EEPROM hardware mode configuration switch
MODEC0 (3pos switch)	DS33Z41 mode pin	HIGH	LOW	Software mode selected
MODEC1 (3pos switch)	DS33Z41 mode pin	LOW	LOW	Software mode selected
HWMODE (3pos switch)	DS33Z41 mode pin	LOW	LOW	Hardware/software mode (software mode selected)
SCANMO (3pos switch)	DS33Z41 mode pin	LOW	LOW	Set low for normal operation
SCANTRI (3pos switch)	DS33Z41 mode pin	LOW	LOW	Set low for normal operation
….testpoints….	DS33Z41 testpoints	—	—	Processor bus, JTAG and LAN side testpoints for Zchip
Z-RESET (button)	DS33Z41 reset	—	—	System reset
A2, A1, A0 (3pos switches)	DS33Z41/SPI pins	Mid position	Mid position	Address pin/EEPROM config switch. Set to mid position to allow connection to processor.
SDRAM CLOCK	DS33Z41 SDRAM clock	Installed	Installed	100MHz oscillator to drive SDRAM clock
MII CLOCK	PHY MII clock	Installed	Installed	25MHz oscillator to drive SDRAM clock

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING		DESCRIPTION
		SW MODE	HW MODE	
spi_cs, spi_ck, spi_miso, spi_mosi	—	—	—	SPI signals (for EEPROM memory)
….testpoints…..	DS33Z41 testpoints	—	—	DS33Z41 serial port testpoints
AFCS (1 per port)	DS33Z41 mode pin	HW mode only	HIGH	Set high to enable auto flow control.
FULLDS (1 per port)	DS33Z41 mode pin	HW mode only	HIGH	Set high to enable full duplex.
H10S (1 per port)	DS33Z41 mode pin	HW mode only	HIGH	Set high to confg for 100Mb.
GROUND/VDD (banana plug)	Power supply ground/3.3V	—	—	Redundant connection to system power. Use plugs at either top or bottom of board.
VDD 3.3V (banana plug)	Power supply VDD	—	—	Redundant connection to system power. Use plugs at either top or bottom of board.

ADDRESS MAP (ALL CARDS)

Motorola resource card address space begins at 0x81000000. All offsets given below are relative to the beginning of the daughter card address space (shown previously).

Table 3. Overview of Daughter Card Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0087	FPGA	Processor board identification
0X1000 to 0X1FFF	DS33Z41	DS33Z41. Uses CS_X1.
0X2000 to 0X2FFF	DS21458	T1/E1 DS21458 resource card. Uses CS_X2.
0X4000 to 0X4010	FPGA	FPGA on DS21458 resource card. Used to facilitate IBO mode. Default configuration of FPGA is compatible with non-IBO mode functionality. The FPGA settings will require modification for use with the DS33Z41 when device drivers are disabled.

Registers in the DS33Z41 and DS21458 can be easily modified using the ChipView host-based user-interface software with the definition files previously mentioned.

Quad T1/E1 Resource Card FPGA Register Map

Table 4. Quad T1/E1 Processor Card FPGA Register Map

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0X4000	Rev	Read only	FPGA Rev
0X4001	delay_line1	Control	Line 1 number of frame delay
0X4002	delay_line2	Control	Line 2 number of frame delay
0X4003	delay_line3	Control	Line 3 number of frame delay
0X4004	delay_line4	Control	Line 4 number of frame delay
0X4005	MO+CLK	Control	Mode and clock ctrl
0X4006	UNUSED	Control	Unused / test
0X4007	UNUSED	Control	Unused / test

ID REGISTERS

REV: FPGA REV (Offset=0X4000)

FPGA Rev is read only, showing the current FPGA revision

CONTROL REGISTERS

Register Name: **delay_line1, delay_line2, delay_line3, delay_line4**
Register Description: **DS33Z41 frame delay**
Register Offset: **0X4001, 0X4002, 0X4003, 0X4004**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	B5	B4	B3	B2	B1	B0
Default	—	—	—	—	0	0	0	0

Bits 5 to 0: B5 to B0. Number of frame delay for a given line.

Register Name: **MO+CLK**
Register Description: **DS33ZXY Mode and Clock Settings**
Register Offset: **0X4005**

Bit #	7	6	5	4	3	2	1	0
Name	LB	MC	IR	tgapclk	rgapclk	comm_tclk	common_rclk	z41_mode
Default	0	—	—	1	1	0	0	0

Bit 7: LB
0 = Normal operation, traffic goes from the Z chip through the FPGA and to the DS21458.
1 = Loopback, Z chip rser is driven by Z chip tser. Clocks, and frame sync for Z41, are still driven by DS21458.

Bit 6: INVERT_RCLKh
0 = Do not invert RCLK.
1 = Invert RCLK.

Bit 5: MclkHiBpclkLow
0 = Use BPCLK for clock signals below.
1 = Use MCLK for clock signals below.
This signal drives the following clocks: TCLK (when bit for common_tclk is set); RCLK (when bit for common_rclk is set); TSYSCLK and RSYSCLK (when bit for Z41_mode is set).

Bit 4: TGAPCLK
0 = Drive internal TGAPCLKx signal with TCLKx.
1 = Drive internal TGAPCLKx signal with TGAPCLK pin.

Bit 3: RGAPCLK
0 = Drive internal RGAPCLKx signal with RCLKx.
1 = Drive internal RGAPCLKx signal with RGAPCLK pin.

Bit 2: Common TCLK
0 = Drive TCLKx with internal TGAPCLKx signal (see bit 4)
1 = Drive Z chip TCLKx with BPCLK

Bit 1: Common RCLK
0 = Drive RCLKx with internal RGAPCLKx signal (see bit 3).
1 = Drive Z chip RCLKx with BPCLK.

Bit 0: Z41 Mode
0 = Not in Z41 mode.
1 = In Z41 mode.

DS33Z41 INFORMATION

For more information about the DS33Z41, consult the DS33Z41 data sheet available on our website at www.maxim-ic.com/DS33Z41.

DS33Z41DK INFORMATION

For more information about the DS33Z41DK, including software downloads, consult the DS33Z41DK data sheet available on the our website at www.maxim-ic.com/DS33Z41DK.

TECHNICAL SUPPORT

For additional technical support, go to www.maxim-ic.com/support.

DOCUMENT REVISION HISTORY

REVISION DATE	DESCRIPTION
051505	Initial DS33Z41DK data sheet release.
080706	Updated Table 2.
110106	Updated schematics.

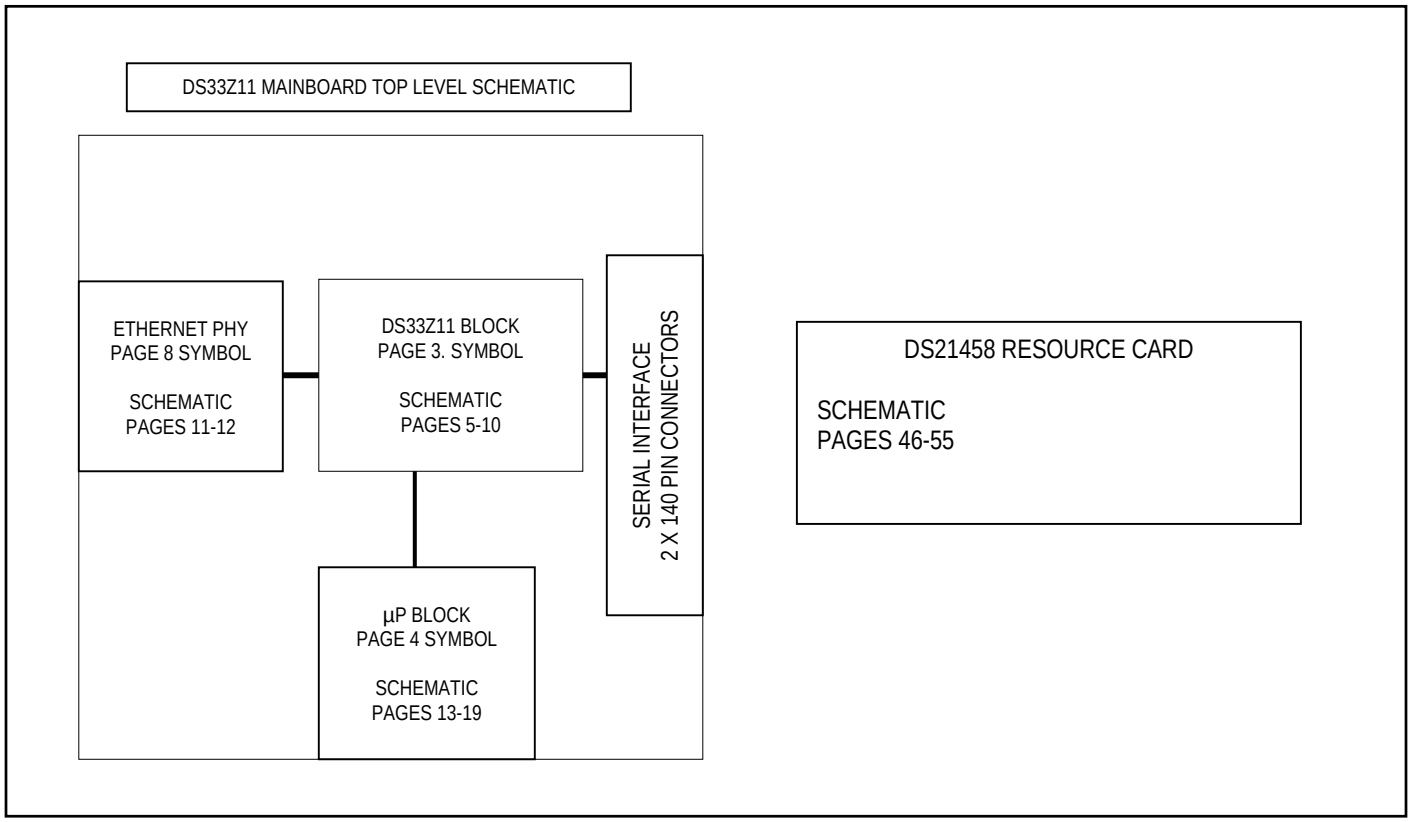
SCHEMATICS

The DS33Z41DK schematics are featured in the following pages. As this is a hierarchal schematic some explanation is in order. The main board is composed of six hierarchal blocks: the processor block, the DS33Z41 block, and four Ethernet blocks inside the DS33Z41 block, which is a nested hierarchy block. The DS21458 consists of a single hierarchy block, which connects to a 140-pin AV bus that snaps into the mainboard.

All signals inside a hierarchy block are local, with exception for V_{CC} and ground. In-port and out-port connectors are used to allow signals inside a hierarchy block to become accessible as pins on the hierarchy blocks symbol. From here, blocks are wired together as if they were ordinary components. The system diagram is shown again below, with schematic page numbers given for each functional block.

This system contained other hierarchy blocks that are not shown (primarily a single-port serial card, T3E3 serial card and the DS33Z44 mainboard). Due to this, page numbers will not be continuous and some gaps in numbering will be seen when referring to the total page count. However, page numbers inside any given hierarchy block will be continuous.

Figure 3. Schematic Hierarchy and Floorplan



DS33Z11/Z41 TOP LEVEL

V3_3

V3_3 3A5<> 3A8<> 3B5<> 3BB<> 3C5<> 3C8<> 4D8> 3D8 4D8

GND

HIERARCHICAL BLOCK

_z11andlan_dn
PAGES 5-10

5C4v 5B1v 5A1v 4C6< A_DUT<9..0>	ADDR<9..0>		
5B4v 4C6< D_DUT<7..0>	DAT<7..0>		
		INT	INT2 3C7<> 3C8<> 4D5< 5A6v
5A6v 4D3> CS_X1	CS		
5A5v 4C5< RD_DUT	RD		
5A5v 4C5< WR_DUT	WR		
5A5v 4C3> 3C7<> RESET_B	RESET_B		
6A6v 3C6<> Z41RSYNC	Z41RSYNC		
6A6v 3C6<> Z41TSYNC	Z41TSYNC		
		HWMODE	BTS_DUT 4B5< 5A5v
		MODEC0	BIS0_DUT 4C5< 5A5v
		MODEC1	BIS1_DUT 4B5< 5A5v

RCLKI TCLKI RSER TSER RDEN TDEN

Z44_RCLK<1> Z44_TCLK<1> Z44_RSER<1> Z44_TSER<1> Z44_RDEN<1> Z44_TDEN<1>

3C6<> 5C5v 3C6<> 5D5v 3C6<> 5C4v 3C8<> 5C5v

PLUG
P2 CONNECTOR (PLUG)

JB13

	V3_3	71	1
	GND	72	2 INT3 4D5<
4C5< INT5		73	3 INT4 4C5<
3D1> 3C7<> INT2 5A6v 4D5<	GND	74	4
	GND	75	5 INT2 3C8<> 3D1> 4D5< 5A6v
		76	6 RESET_B 4C3> 3D3< 5A5v
	GND	77	7
	V3_3	78	8
3C1> 5C5v Z44_RSER<1>		79	9 Z44_TSER<1> 3C1> 5D5v
	GND	80	10
3C1> 5C5v Z44_RDEN<1>	GND	81	11 SIG_RETURN 3A1> 3A3<> 3B7<>
		82	12 Z44_TDEN<1> 3C1> 5C4v
	GND	83	13
3C2> 5C5v Z44_RCLK<1>	GND	84	14
		85	15 Z44_TCLK<1> 3C2> 5C5v
	GND	86	16
	GND	87	17 Z41RSYNC 3D3< 6A6v
		88	18 Z41TSYNC 3D3< 6A6v
4D8 3D8	GND	89	19
3D8> 3B5<> 3A8<> 3A5<> 4D8> 3C8<> 3C5<> 3BB<>	V3_3	90	20
		91	21
	GND	92	22 SIG_RETURN 3A1> 3A3<> 3C7<>
Z44_RSER<2>		93	23 Z44_TSER<2>
	GND	94	24
Z44_RDEN<2>	GND	95	25
		96	26 Z44_TDEN<2>
	GND	97	27
Z44_RCLK<2>	GND	98	28
		99	29 Z44_TCLK<2>
	GND	100	30
4D8 3D8		101	31
3D8> 3B5<> 3A8<> 3A5<> V3_3 4D8> 3C8<> 3C5<> 3BB<>		102	32
		103	33
	GND	104	34
	GND	105	35
		106	36
	GND	107	37
	GND	108	38
		109	39
	GND	110	40
	GND	111	41
		112	42
4D8 3D8	GND	113	43
3D8> 3B5<> 3A8<> 3A5<> V3_3 4D8> 3C8<> 3C5<> 3BB<>		114	44
		115	45
	GND	116	46
	GND	117	47
		118	48
	GND	119	49
	GND	120	50
		121	51
	GND	122	52
	GND	123	53 TDO_NU 4B4>
4B4> TDI_NU 3DB>		124	54 TCK_NU 4B4>
3C5<> 4B4> TMS_NU 3DB>	GND	125	55
3B5<> 3A8<> 3A5<> V3_3 4D8> 3C8<> 3BB<>		126	56
4D8>		127	57
	GND	128	58
	GND	129	59
		130	60
	GND	131	61
XA<15..0>	GND	132	62
		133	63 XA<15..0>
	GND	134	64 3A8 4B2>
	GND	135	65
		136	66
	GND	137	67
3C5<> 3A8<> 3A5<> V3_3 3BB<> 3B5<> OSC2_NU		138	68
4D8 3D8 4D8> 3D8> OSC4_NU		139	69 OSC3_NU
		140	70 GND

PLUG
P1 CONNECTOR (PLUG)

JB09

	GND	71	1
4C3> CS_X5		72	2 ALE
	GND	73	3 CS_X4 4C3>
		74	4
	GND	75	5
		76	6
	GND	77	7
4D8 3D8 4D8> 3D8> 3C8<> 3C5<> 3BB<> 3B5<> 3A8<> 3A5<>	V3_3	78	8
		79	9
	GND	80	10
	GND	81	11
		82	12
	GND	83	13
		84	14
		85	15
	GND	86	16
	GND	87	17
		88	18
	GND	89	19
4D8 3D8 4D8> 3D8> 3C8<> 3C5<> 3BB<> 3B5<> 3A8<> 3A5<>	V3_3	90	20
		91	21
	GND	92	22
	GND	93	23
Z44_RSER<3>		94	24
	GND	95	25
	GND	96	26
Z44_RDEN<3>		97	27 Z44_TSER<3>
		98	28
	GND	99	29
Z44_RCLK<3>		100	30 Z44_TDEN<3>
	GND	101	31
3D8> 3C8<> 3C5<> 3BB<> 3B5<> 3A8<> 3A5<> 4D8 3D8 4D8>	V3_3	102	32
		103	33 Z44_TCLK<3>
	GND	104	34
	GND	105	35
		106	36
	GND	107	37
	GND	108	38
		109	39
	GND	110	40
	GND	111	41
Z44_RSER<4>		112	42 Z44_TSER<4>
	GND	113	43
3D8> 3C8<> 3C5<> 3BB<> 3B5<> 3A8<> 3A5<> 4D8 3D8 4D8>	V3_3	114	44
Z44_RDEN<4>		115	45 Z44_TDEN<4>
	GND	116	46
Z44_RCLK<4>		117	47 SIG_RETURN 3A1> 3B7<> 3C7<>
		118	48 Z44_TCLK<4>
	GND	119	49
	GND	120	50
		121	51
	GND	122	52
	GND	123	53
		124	54
	GND	125	55
4D8 3D8 4D8> 3D8> 3C8<> 3C5<> 3BB<> 3B5<> 3A8<> 3A5<>	V3_3	126	56
		127	57
	GND	128	58
	GND	129	59
OSC1_NU		130	60 0
	GND	131	61
		132	62 1
		133	63 3 XD<7..0>
	GND	134	64
3A4 4B2> XD<7..0>	GND	135	65 5
		136	66 7
	GND	137	67
4D3> CS_X2	V3_3	138	68
4D8 3D8 4D8> 3D8> 3C8<> 3C5<> 3BB<> 3B5<> 3A8<> 3A5<> 4C3> CS_X3		139	69 RW_X 4C3>
4C3> WR_X		140	70 GND

GND SIG_RETURN 3A3<> 3B7<> 3C7<>

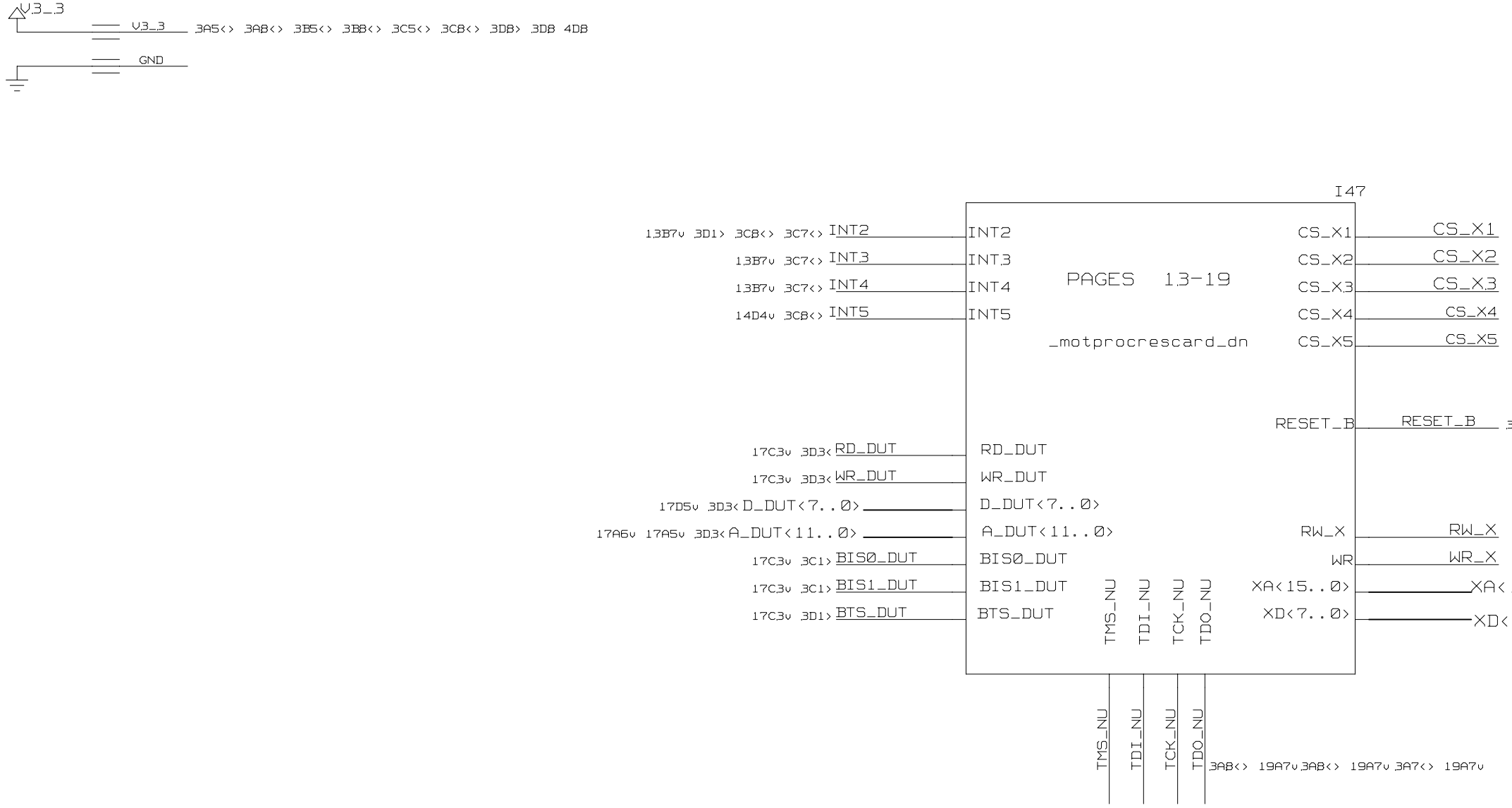
MOTHERBOARD CONNECTORS FOR WAN R.C.

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:1/2(BLOCK) 3/71(TOTAL)

BLOCK NAME: _z11top_dn. PARENT BLOCK: _ztopdn_\

PRINTED Fri Oct 20 10:50:40 2006

CR-4 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_15@_ZTOP_LIB\._Z11TOP_DN\(SCH_1):PAGE2



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:2/2(BLOCK) 4/71(TOTAL)

BLOCK NAME: _z11top_dn. PARENT BLOCK: _ztopdn_\

JMP_3

CR-5 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I5@_ZTOP_LIB\._Z11TOP_DN\(SCH_1):PAGE1_I1@_ZTOP_LIB\._Z11ANDLAN_DN\(SCH_1):PAGE1

DS.33Z11/Z41

JTAG LINE IO

JTMS JTDI JTDO JTCLK JTRST RCLKI TCLKI RSER TSER RDEN/RBSYNC TDEN/TBSYNC QOVF

F7 TIMS 5A3<> | E4 TIDI 5A3<> | E5 TIDO 5A3<> | D4 TICLK 5A3<> | E6 TIRST 5A3<>

G2 YTP72 RCLKI IN 3C2^ | F1 YTP71 TCLKI IN 3C2^ | H1 YTP78 RSER IN 3C2^ | F2 YTP77 TSER OUT 3C2^ | H2 YTP75 TDEN IN 3C2^ | F5 YTP74 TDEN IO 3C2^

RB355 30 | R30 30

C7 LED+TP

NC7SZ86_U BUFFER UXB06 TP53 R197 330 DS39 RED

U18

DS.33Z11_U3

MII/RMII

REF_CLK BA1< YTP36 D13 REF_CLK

REF_CLKO YTP35 RB174 30 E13 REF_CLKO

RX_CRS<1> BC3> C8 RX_CRS/CRS_DV

RX_ERR<1> BC3> B12 RX_ERR

RX_CLK<1> BC3> A10 RX_CLK

RXD0<1> BD3> B11 RXD<0>

RXD1<1> BC3> C11 RXD<1>

RXD2<1> BC3> D11 RXD<2>

RXD3<1> BC3> A11 RXD<3>

RXDV<1> BC3> D10 RXDV

<INPUT>

TX_CLK<1> BC5< A8 TX_CLK

TXD0<1> BD5< RB177 30 B9 TXD<0>

TXD1<1> BC5< RB178 30 C9 TXD<1>

TXD2<1> BC5< R55 VALUE=30 D9 TXD<2>

TXD3<1> BC5< RB175 VALUE=30 E9 TXD<3>

TX_EN<1> BC5< RB176 30 E10 TX_EN

<OUTPUT>

COL_DET<1> BC3> B13 COL_DET

MDC BB4> RB173 30 C12 MDC

MDIO BB4> R74 30 C13 MDIO

MICRO PORT/SPI MASTER PORT

INT* F3 OUT 3D1^ 5A6<> | CS* C1 IN 3D2^ | SPI_CS* B8 ZSPICS 5C2< | RD*/DS* E1 RD IN 3D2^ | WR*/RW* E2 WR IN 3D2^ | RST* B8 RESET_B 8B4< 3D2^ | HWMODE D5 HWMODE OUT 9D4< 3D1^ | MODEC<0> D6 MODEC0 OUT 9D2< 3C1^ | MODEC<1> D7 MODEC1 OUT 9D4< 3C1^ | DCEDTES A13 DCEDTES 9D2< | RMIIMIIS C4 RMIIMIIS 9C4< | FULLDS A9 FULLDS 9C2< | H10S B10 H10S 9C4< | AFCS C10 AFCS 9C2< | SCAN/EN E7 SCANEN 9B4< | SCAN/MODE E8 SCANMOD 9B2< | CKPHA F6 CKPHA 9B4<

A<0> A1 ZADDR0 5B2<>

A<1> B1 ZADDR1 5B2<>

A<2> A2 ZADDR2 5A2<>

A<3> B2 3

A<4> C2 4

A<5> A3 5

A<6> B3 6

A<7> C3 7

A<8> A4 8

A<9> B4 9

ADDR<9..0> IN 3D2^ 5B1<

D<0>/MOSI A5 ZMOSI 0

D<1>/MISO A6 ZMISO 1

D<2>/SPICK A7 ZSPISCK 2

D<3> B5 3

D<4> B6 4

D<5> B7 5

D<6> C5 6

D<7> C6 7

DAT<7..0> IO 3D2^

2.7V

Y13

5B4<> ZMOSI 5 SI | 5B4<> ZMISO 2 SO | 5B4<> ZSPISCK 6 SCK | 5A5> ZSPICS 1 CS* | VCC 8 | WP* 3 | HOLD* 7 | GND 4

V3_3 RB345 10K RB343 10K

AT25160A_U

V3_3

SW24 SP3T 5C3< ZADDR0 0

SW25 SP3T 5C3< ZADDR1 1

SW26 SP3T 5C3< ZADDR2 2

4 common

ADDR<9..0> IN 3D2^ 5B2<

J29

5D5< JTCLK 1 | 5D5< JTMS 3 | 5D5<> JTDO 5 | 5D5< JTDI 7 | 5D5< JTRST 9 | 10

2 TCK_NU | 4 TMS_NU | 6 TDI_NU | 8 TDO_NU

V3_3

CONN_10P

DS44

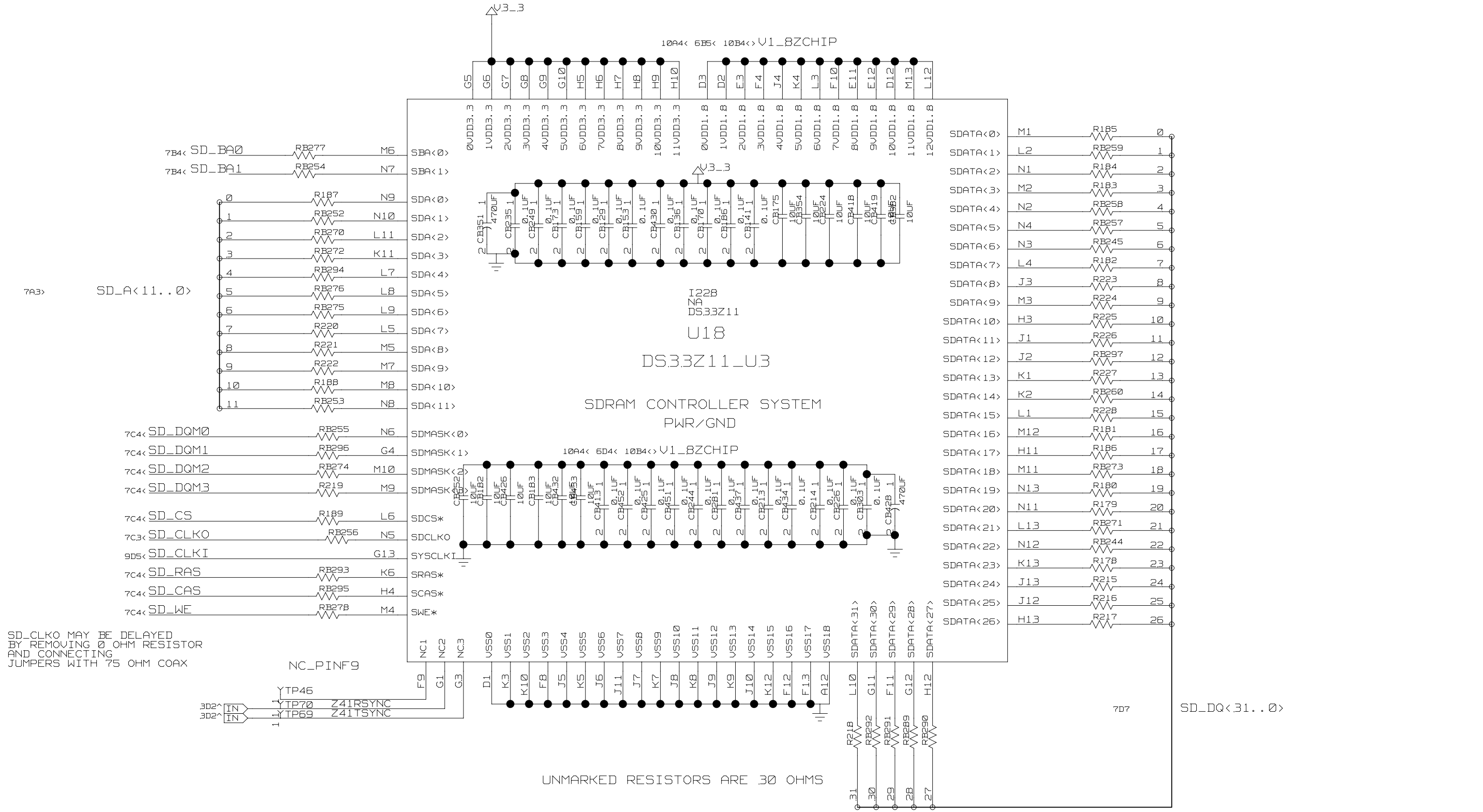
V3_3 RB342 330 RED NC7SZ86_U BUFFER UXB08 INT 5A6> 3D1^

HW MODE PINS ARE OUTPUTS FROM Z MODULE TO PROC
PROC (FPGA) AUTOMATICALY IMPLEMENTS BUS MODE

TITLE: DS.33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:1/6(BLOCK) 5/71(TOTAL)

BLOCK NAME: _z11andlan_dn. PARENT BLOCK: _z11top_dn\

CR-6 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I5@_ZTOP_LIB\._Z11TOP_DN\(SCH_1):PAGE1_I1@_ZTOP_LIB\._Z11ANDLAN_DN\(SCH_1):PAGE2



TITLE: DS.33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/6 (BLOCK) 6/71 (TOTAL)

BLOCK NAME: _z11andlan_dn. PARENT BLOCK: _z11top_dn\

CR-7 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_15@_ZTOP_LIB\._Z11TOP_DN\(SCH_1):PAGE1_11@_ZTOP_LIB\._Z11ANDLAN_DN\(SCH_1):PAGE3

6A2

SD_DQ<31..0>

V3_3

FROM Z11 SYSCLKO

UB10

MT48LC4M32B2_TSOP_U

SYNCHRONOUS DRAM

MT48LC4M32B2 - 1 MEG X 32 X 4 BANKS

DQ<2>	5		CLK	68	SD_CLKO 6BB<
DQ<3>	7		CKE	67	
DQ<4>	8		CS*	20	SD_CS 6BB<
DQ<5>	10		WE*	17	SD_WE 6A8<
DQ<6>	11		CAS*	18	SD_CAS 6BB<
DQ<7>	13		RAS*	19	SD_RAS 6BB<
DQ<8>	74		DQM<0>	16	SD_DQM0 6BB<
DQ<9>	76		DQM<1>	71	SD_DQM1 6BB<
DQ<10>	77		DQM<2>	28	SD_DQM2 6BB<
DQ<11>	79		DQM<3>	59	SD_DQM3 6BB<
DQ<12>	80		BA<0>	22	SD_BA0 6D7<
DQ<13>	82		BA<1>	23	SD_BA1 6C7<
DQ<14>	83		A<0>	25	0
DQ<15>	85		A<1>	26	1
DQ<16>	31		A<2>	27	2
DQ<17>	33		A<3>	60	3
DQ<18>	34		A<4>	61	4
DQ<19>	36		A<5>	62	5
DQ<20>	37		A<6>	63	6
DQ<21>	39		A<7>	64	7
DQ<22>	40		A<8>	65	8
DQ<23>	42		A<9>	66	9
DQ<24>	45		A<10>	24	10
DQ<25>	47		A<11>	21	11
DQ<26>	48				
DQ<27>	50				
DQ<28>	51				
DQ<29>	53				

SD_A<11..0> 6C8

DQ<1> 4, DQ<0> 2, DQ<30> 54, DQ<31> 56

VDD4 43, VDD3 29, VDD2 15, VDD1 1

VDDQ8 81, VDDQ7 75, VDDQ6 55, VDDQ5 49, VDDQ4 41, VDDQ3 35, VDDQ2 9, VDDQ1 3

VSS4 86, VSS3 72, VSS2 58, VSS1 44

VSSQ8 84, VSSQ7 78, VSSQ6 52, VSSQ5 46, VSSQ4 38, VSSQ3 32, VSSQ2 12, VSSQ1 6

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:3/6(BLOCK) 7/71(TOTAL)

BLOCK NAME: _z11andlan_dn. PARENT BLOCK: _z11top_dn\

CR-B : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I5@_ZTOP_LIB\._Z11TOP_DN\(SCH_1):PAGE1_I1@_ZTOP_LIB\._Z11ANDLAN_DN\(SCH_1):PAGE4

HIERARCHICAL BLOCK
_mii_wan_dn
PAGES 11-12

11A5v 5B7< TXD0<1> — TXD0
11A5v 5B7< TXD1<1> — TXD1
11A5v 5B7< TXD2<1> — TXD2
11A5v 5B7< TXD3<1> — TXD3
11A5v 5B7<> TX_CLK<1> — TX_CLK
11A5v 5BB< TX_EN<1> — TX_EN
11C5v BBB< LED_DPLX_A0<1> — LED_DPLX_ADD0
11C5v BBB< LED_COL_A1<1> — LED_COL_ADD1
11C5v BAB<> LED_GDLINK_A2<1> — LED_GDLINK_ADD2
11C5v BAB<> LED_TX_A3<1> — LED_TX_ADD3
11C5v BAB<> LED_RX_A4<1> — LED_RX_ADD4

RXD0 — RXD0<1> 5C7< 11A7v
RXD1 — RXD1<1> 5C7< 11A7v
RXD2 — RXD2<1> 5B7< 11A7v
RXD3 — RXD3<1> 5B7< 11A7v
RX_CLK — RX_CLK<1> 5C7<> 11A7v
RX_CRS — RX_CRS<1> 5C7< 11A7v
RX_ERR — RX_ERR<1> 5C7< 11A7v
RXDV — RXDV<1> 5B7< 11A7v
COL_DET — COL_DET<1> 5B7< 11A7v

RESET_B — RESET_B
MDIO — MDIO
MDC — MDC
MII_CLK — MII_CLK

RESET_B: 11C7v 5A5< 3D2>
MDIO: 11C5v 5B7<5B7< BA1< 11C7v 11C5v
MDC: 11C5v 5B7<5B7< BA1< 11C7v 11C5v
MII_CLK: 11C5v 5B7<5B7< BA1< 11C7v 11C5v

11C5v BC6< LED_DPLX_A0<1> — RB44 5.1K — V3_3
11C5v BC6< LED_COL_A1<1> — RB48 5.1K

LED_GDLINK_A2<1> — RB72 5.1K — DS15 — RB78 330 — GREEN

LED_TX_A3<1> — RB60 5.1K — DS11 — RB57 330 — AMBER

LED_RX_A4<1> — RB47 5.1K — DS06 — RB54 330 — RED

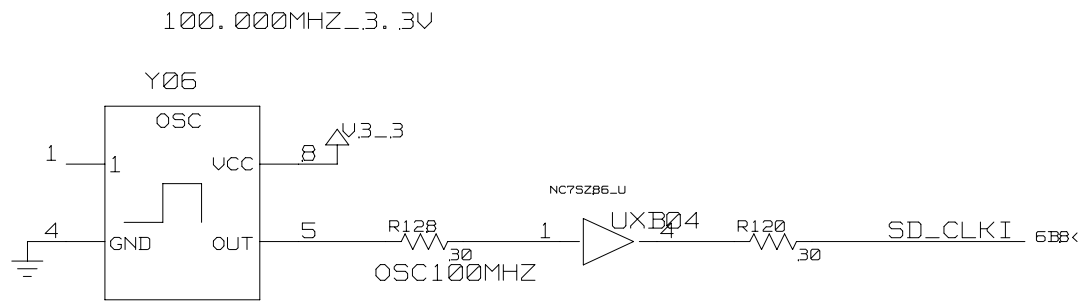
I69
1000100MZH
V3_3 — L04 — 1000100MZH — LB01
CR53 10UF
CR54 10UF
C10 0.1UF
CHASSIS GND FOR PHY
CHASSIS

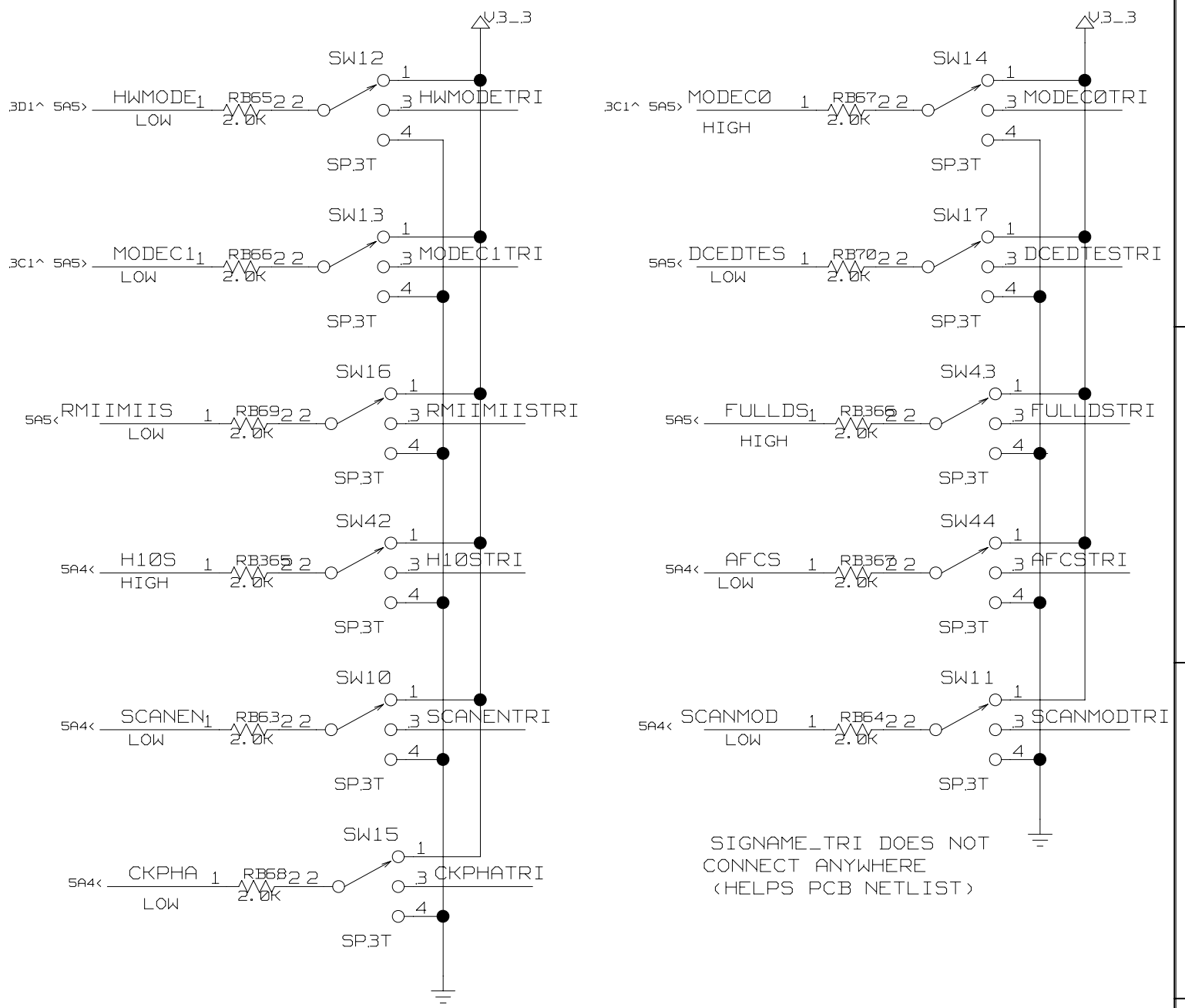
25.000MHZ_3.3V
Y09
OSC
V3_3
1 — VCC — 8
4 — GND
5 — OUT
R140 30 — MII_CLK BB3> 11C7v
R133 30 — REF_CLK 5C7<>

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:4/6(BLOCK) 8/71(TOTAL)

BLOCK NAME: _z11andlan_dn PARENT BLOCK: _z11top_dn\

CR-9 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_15@_ZTOP_LIB\._Z11TOP_DN\(SCH_1):PAGE1_11@_ZTOP_LIB\._Z11ANDLAN_DN\(SCH_1):PAGE5





SIGNAME_TRI DOES NOT
CONNECT ANYWHERE
(HELPS PCB NETLIST)

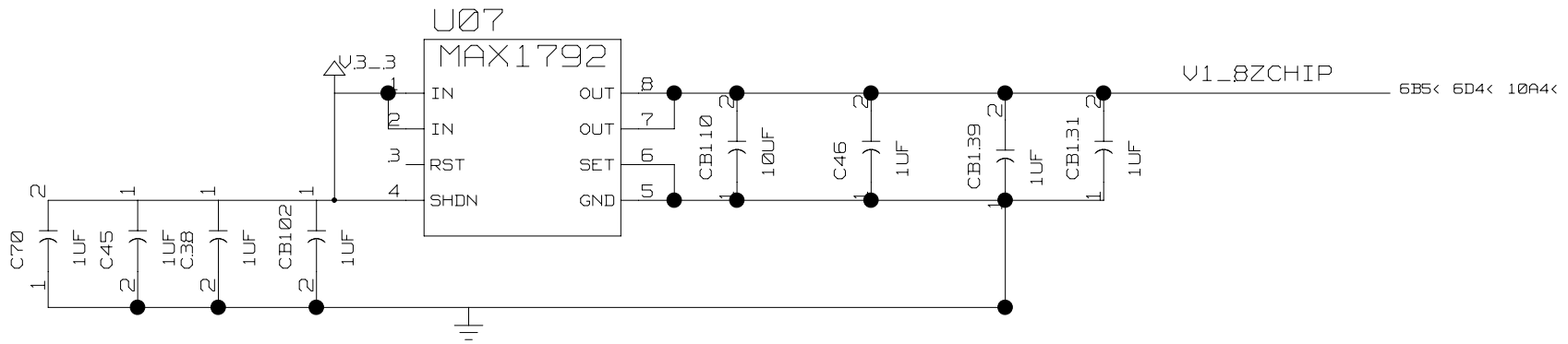
MODE (SHOWN BELOW SIGNAL) RESULTS IN:
MOTOROLA NON-MUX, MII, FULL DUPLEX, 100 MBIT, AUTO-FLOW CONTROL

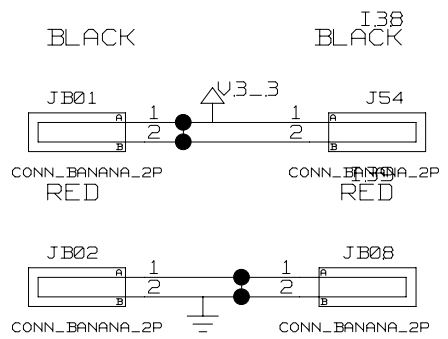
CONFIG SWITCHES FOR Z11

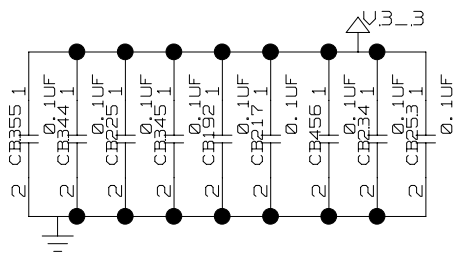
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 5/6 (BLOCK) 9/71 (TOTAL)

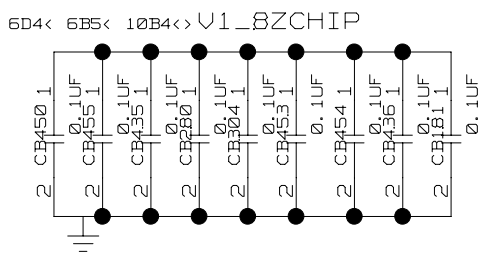
BLOCK NAME: _z11andlan_dn, PARENT BLOCK: _z11top_dn\

CR-10 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I5@_ZTOP_LIB\._Z11TOP_DN\(SCH_1):PAGE1_I1@_ZTOP_LIB\._Z11ANDLAN_DN\(SCH_1):PAGE6









TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:6/6(BLOCK) 10/71(TOTAL)

BLOCK NAME: _z11andlan_dn, PARENT BLOCK: _z11top_dn\

CR-11 : @_ztop_lib\:_ztopdn_\(sch_1):page1_15@_ztop_lib\:_z11top_dn\(sch_1):page1_11@_ztop_lib\:_z11andlan_dn\(sch_1):page4_132@_ztop_lib\:_mii_wan_dn\(sch_1):Page1

COMPONETS FOR
C1 AND RBIAS MUST
BE PLACED CLOSE TO PIN

C1PIN

C32 10UF
C30 0.1UF

R08 10.0K RBIAS

U04
DP83847_U1
CONTROL

LEDS NEED TO BE ATTACHED
OUTSIDE OF MODULE DUE TO
STRAP ADAPTING OPTION OF DP83847

R109 30

RESERVED2
RESERVED1
C1
RBIAS
X1
RESET*
X2
RESERVED10
RESERVED11
RESERVED12
RESERVED13
RESERVED14
RESERVED15
RESERVED16
RESERVED17
RESERVED18
RESERVED3
RESERVED4
RESERVED5
RESERVED6
RESERVED7
RESERVED8
RESERVED9
VDD/IO_VDD1
VDD/IO_VDD2
VDD/ANA_VDD
VDD1
VDD2
VDD3
GND1
GND2
GND3
GND4
GND5
MDC
MDIO
LED_DPLX/PHYAD0
LED_COL/PHYAD1
LED_GDLNK/PHYAD2
LED_TX/PHYAD3
LED_RX/PHYAD4
LED_SPEED
AN_EN
AN_1
AN_0

MII_CLK
RESET_B
MDC
MDIO
LED_DPLX_ADD0
LED_COL_ADD1
LED_GDLINK_ADD2
LED_TX_ADD3
LED_RX_ADD4
TP03
RB55 5.1K
RB52 5.1K
RB07 5.1K
AN_EN
AN1
AN0

V3_3
AN_V3_3

JP09 JP15 JP14

J14

RXD0
RXD1
RXD2
RXD3
RXDV
RX_CRS
COL_DET
RX_ERR
RX_CLK

CONN_10P

J13

TX_CLK
TX_EN
TXD3
TXD2
TXD1
TXD0

CONN_10P

1000100MZH

L03

PLACEMENT NOTE:
TESTPOINTS (SHOWN ABOVE) MUST BE PLACED THE SAME FOR EACH PORT TO
ALLOW USE OF A DIFFERENT PHY CARD IF DESIRED. PLACEMENT SHOULD ALLOW
0.2 BETWEEN CONNECTORS.

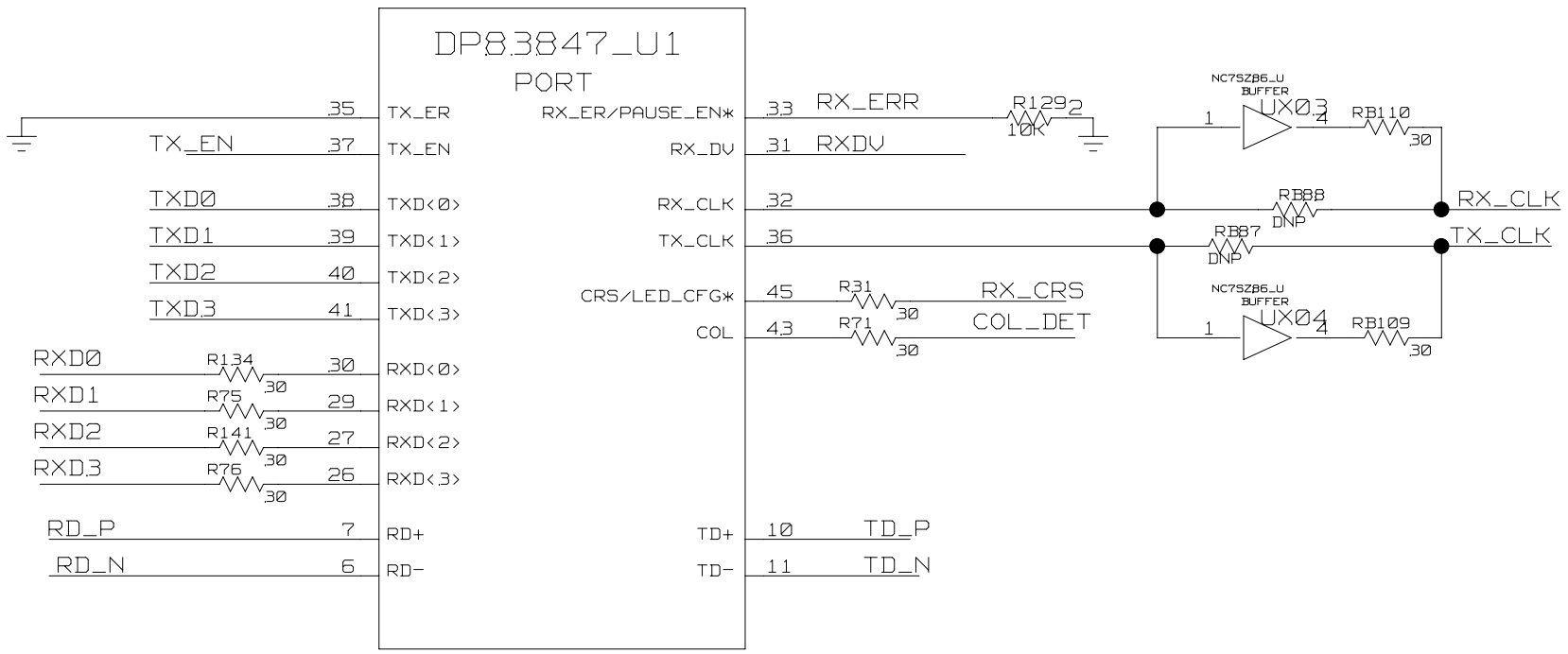
ON Z44 CARD ALL 4 PORTS MUST BE PLACED WITH EQUAL SPACING AND A COMMON CENTER LINE

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 11/71(TOTAL)

BLOCK NAME: _mii_wan_dn. PARENT BLOCK: _z11andlan_dn\

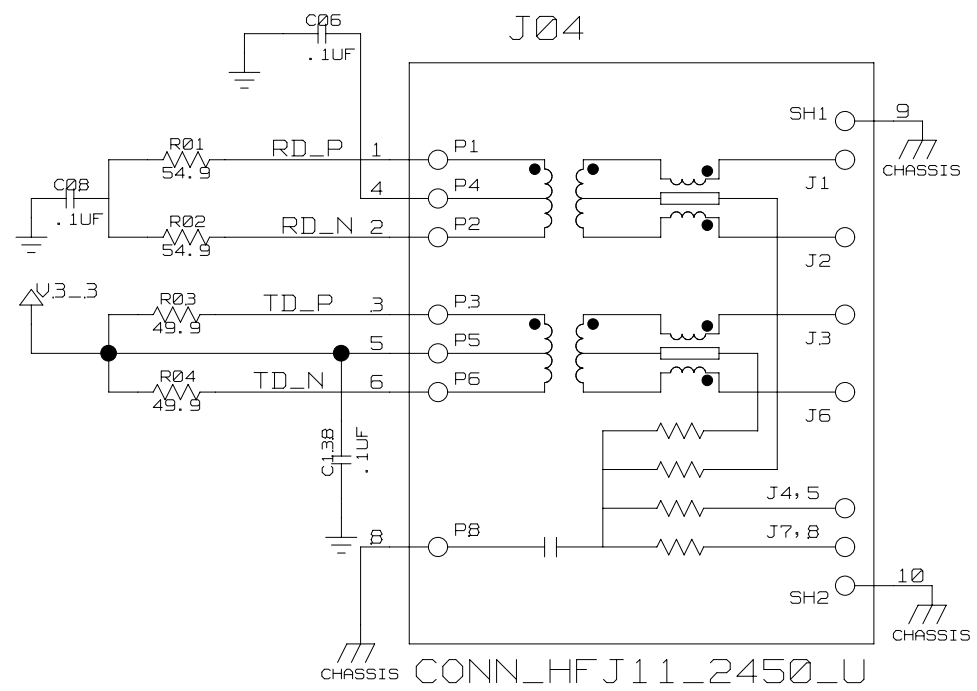
PRINTED Fri Oct 20 10:50:42 2006

U04



SYM_1

J04



CAPS FOR XFRM CENTER TAP
SHOULD BE PLACED CLOSE TO XFRM

RESISTORS FOR TD+-/RD+-
SHOULD BE PLACED CLOSE TO PHY

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/2 (BLOCK) 12/71 (TOTAL)

TQFP
NZA
MMC2107
I69

U15

MMC2107
CONTROL

INT7*	89	USER_LED1	
INT5*	84	USER_LED2	
INT4	82	INT3	
INT3*	79	INT4	
INT2*	75	RUN_KIT_USR	
INT1*	72	TIM_STATUS	
INT0*	71	INT2	
YC0	80	YC0	
MOSI	90	MOSI	
MISO	91	MISO	
XTAL	124	XTAL	
EXTAL	125	OSC_MCU	
TCLK	130	ONCE_TCLK	
TRST*	142	ONCE_TRST_B	
TMS	138	ONCE_TMS	
INT8*	88	TIM_16H_8L	
EB3*	96	EB3	
EB2*	98	EB2	
EB1*	100	EB1	
EB0*	101	EB0	
PQB3	104	PQB3	
PQB2	105	PQB2	
PQB1	106	PQB1	
PQB0	107	PQB0	
PQA4	108	PQA4	
PQA3	109	PQA3	
PQA1	110	PQA1	
PQA0	111	PQA0	
TDI	133	ONCE_TDI	
TDO	135	2107_TDO	
ICOC23	52	ICOC23	
ICOC22	53	ICOC22	
ICOC21	54	ICOC21	
ICOC20	55	ICOC20	
ICOC13	56	ICOC13	
ICOC12	57	ICOC12	
ICOC11	58	ICOC11	
ICOC10	61	ICOC10	
GND	I68	TEST	63
SCI2_OUT	66	TXD2	
SCI2_IN	68	RXD2	
SCI1_OUT	69	TXD1	
SCI1_IN	70	RXD1	
CSE1	60	CSE1	
CSE0	62	CSE0	
TC2	67	TC2	
TC1	78	TC1	
CS3*	81	CS3	
CS2*	83	CS2	
CS1*	85	CS1	
CS0*	86	CS0	
RESET*	118	RESET_B	
CLKOUT	128	CPUCLK_OUT	
RSTOUT*	120	PROC_RESET_OUT	
SCK	93	SCK	
DE*	143	ONCE_DE_B	
SS*	94	SS	

SOT143
2.93V
MAX811SEUS-T
I70
U13

MAX811_U

MR*	3	I64 SW23	
GND	1	RESET*	2
VCC	4	V3_3	

TQFP
NZA
MMC2107
I51
U15

RW	59	RW	
OE*	95	OE	
SHS*	97	RCON	
TA*	99	TA	
TEA*	102	TEA	
VSTBY	92		
VRH	113	VRH	
VRL	112		
VPP	87	FLASH_VPP	
VDDA	115		
VDDF	74		
VDDH	103		
VDDSYN	123	VDDSYN	
VDD8	141		
VDD7	129		
VDD6	77		
VDD5	65		
VDD4	45		
VDD3	33		
VDD2	19		
VDD1	9	V3_3	

R77 2 0.0
C67 2 1 .1UF

MMC2107
PORT

D31	31	144	
D30	30	1	
D29	29	2	
D28	28	3	
D27	27	4	
D26	26	5	
D25	25	7	
D24	24	10	
D23	23	12	
D22	22	15	
D21	21	16	
D20	20	17	
D19	19	20	
D18	18	21	
D17	17	22	
D16	16	25	
D15	15	27	
D14	14	30	
D13	13	31	
D12	12	34	
D11	11	35	
D10	10	36	
D9	9	37	
D8	8	38	
D7	7	39	
D6	6	40	
D5	5	41	
D4	4	42	
D3	3	43	
D2	2	45	
D1	1	48	
D0	0	51	
PD<31..0>			
VSSA	114		
VSSF	73		
VSSSYN	126		
VSS8	140		
VSS7	127		
VSS6	76		
VSS5	64		
VSS4	44		
VSS3	32		
VSS2	18		
VSS1	8		
A22	116	22	
A21	117	21	
A20	119	20	
A19	121	19	
A18	122	18	
A17	131	17	
A16	132	16	
A15	134	15	
A14	136	14	
A13	137	13	
A12	139	12	
A11	6	11	
A10	11	10	
A9	13	9	
A8	14	8	
A7	23	7	
A6	24	6	
A5	26	5	
A4	28	4	
A3	29	3	
A2	47	2	
A1	49	1	
A0	50	0	
PA<22..0>			

MMC2107
PROCESSOR RESOURCE CARD

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 1/7 (BLOCK) 13/71 (TOTAL)

CR-14 : @_ztop_lib\._ztopdn_\(sch_1):page1_15@_ztop_lib\._z11top_dn\(sch_1):page2_147@_ztop_lib\._motprocrescard_dn\(sch_1):Page2

RESET CONFIGURATION

MASTER MODE

FULL DRIVE

XTAL W/ PLL

INTERNAL
FLASH ENABLE

BOOT
INTERN/EXTERN

PD<26> R230 10K
PD<17> R236 10K
PD<16> R235 10K
PD<21> R233 10K
PD<23> R232 10K
PD<22> R231 10K
PD<28> R234 10K
V3_3

RCON R152 10K

PD<19> R196 10K
PD<18> R229 10K

WHEN SET FOR
BOOT INTERNAL
D18 HAS A 10K LOAD TO GND
BOOT EXT
D18 HAS A 10.5K LOAD TO V3V

V3_3
R255 1.0K
R248 1.0K
R07 1.0K
R1502 1.0K
R254 1.0K
R12 1.0K
R16 1.0K
R79 1.0K
V5_0
I69
SW06
SWITCH
8 POS
BTS_0BSXI
BIS10BSXI
BIS00BSXI
INT3
INT4
USERFPGA2
INT5
FLASH_VPP
R83 30
DS20
I65
AMBER
V3_3
0L_SMT0805_10PCT
ECJ-2VB1C104K
C12 .1UF

U30
I54
CY62128V
CY62128V
VCC N_C WE* OE* CE2 CE1* GND
EB0 OE CS0
A16 A15 A14 A13 A12 A11 A10 A9 A8
A7 A6 A5 A4 A3 A2 A1 A0
IO7 IO6 IO5 IO4 IO3 IO2 IO1 IO0
PD<31..24>
PA<17..1>

U26
I18
CY62128V
CY62128V
VCC N_C WE* OE* CE2 CE1* GND
FB1 OE CS0
A16 A15 A14 A13 A12 A11 A10 A9 A8
A7 A6 A5 A4 A3 A2 A1 A0
IO7 IO6 IO5 IO4 IO3 IO2 IO1 IO0
PD<23..16>
PA<17..1>

RESET AND CHIP CONFIGURATION

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/7 (BLOCK) 14/71 (TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _z11top_dn\

X01
I47
8.0MHZ
OSC_MCU
R56
1.0M
PLACE PADS FOR CAP
BUT DO NOT POPULATE
XTAL

V3_3
R81 10K
R80 10K
J06
CON14P
CON14P
NA
I1
CON14P
ONCE_TDI
2107_TDO
ONCE_TCLK
RESET_B
ALIGN KEY
ONCE_TMS
ONCE_DE_B
ONCE_TRST_B
R209
10K
I11

V5_0
C44 1UF
C33 10UF
C27 10UF
CB113 1UF
RB134 330
C52 68UF
U01
MAX1675
OUT
LX
GND
SHDN
FB
LBI
LBO*
REF
I10
L02
22.0UH
C25 68UF
C03 .1UF

MAX3233E
MAX3233E
NA
I31
U21
MAX3233E
R2OUT
INVALID*
T2IN
T1IN
FORCEON
R1OUT
T1OUT
R1IN
VCC
FORCEOFF*
R2IN
T2OUT
GND
V-
C2-
C2+
C1-
C1+
V+2
V+1
SCI1_OUT
SCI1_IN
PRT1_OUT
PRT1_IN

SMT1206_5PCT
ERJ-8GEYJ5R6V
R10
5.6
C02 1UF
C07 1UF
C21 1UF
C14 1UF
C40 1UF
CB28 1UF
CB490 1UF
CB488 1UF
C55 1UF
VDDSYN

R110 10K
R95 10K
R87 10K
I35
J28
PRT1_OUT
PRT1_IN
CONN_DB9P

JTAG CONFIGURATION
ONCETDI PIN
MMC2107
ONCETDO PIN
TDI
...FPGA+FLASH...

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:3/7(BLOCK) 15/71(TOTAL)

CR-16 : @_ztop_lib\._ztopdn_\(sch_1):page1_15@_ztop_lib\._z11top_dn\(sch_1):page2_147@_ztop_lib\._motprocrescard_dn\(sch_1):Page4

J45

CONN_10P

SPARE_B<5..0>

BANK 1

U27

XC2S50_BGA

BANK 0

BANK 2

BANK 3

PD<31..16>

PA<16..0>

X_INIT

TIM_INTERUPT_IND

TIM_INTERUPT

USER_LED1

USER_LED2

PROC_RESET_OUT

CFG_DIN

R176 330

R32 330

R70 330

R237 330

DS38 RED

DS16 RED

DS18 RED

DS43 GREEN

V3_3

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 4/7 (BLOCK) 16/71 (TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _z11top_dn\

CR-17 : @_ztop_lib\._ztopdn_\(sch_1):page1_15@_ztop_lib\._z11top_dn\(sch_1):page2_147@_ztop_lib\._motprocrescard_dn\(sch_1):Page5

I34
ZZCONN_THRU-HOLE
NA

J46

CONN_10P

SPARE_A<10..1>

D_DUT<7..0>

CPUCLK_OUT

BANK 5

I46
U27

XC2S50_BGA

BANK 4

BANK 6

BANK 7

XA<11..0>

XD<7..0>

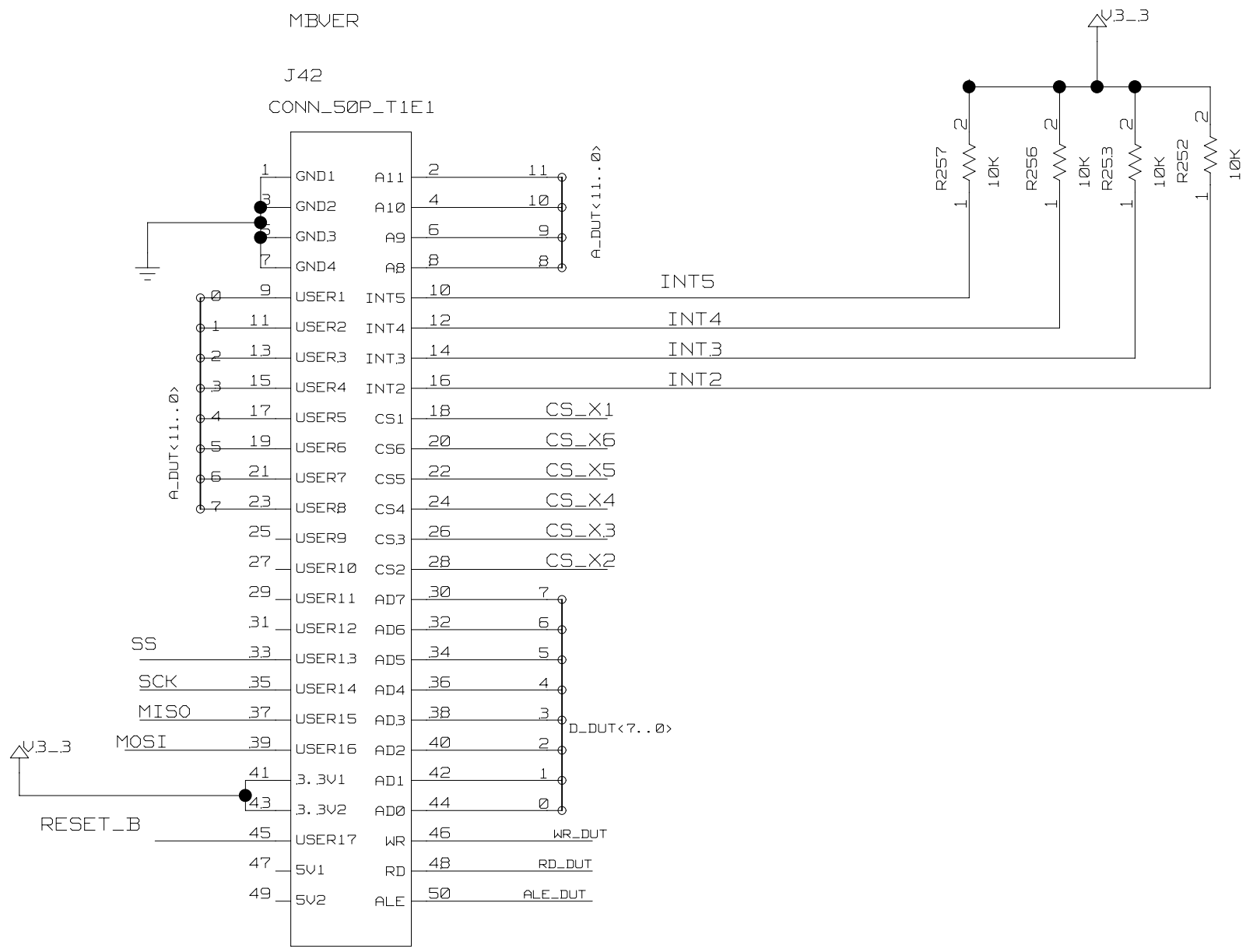
A_DUT<11..0>

BUS MODE
DETECTION (DUT AT CS_X2)

WE ALSO FUNCTIONS AS ALT_WR_RW
RW ALSO FUNCTIONS AS ALT_RD_DS

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 5/7 (BLOCK) 17/71 (TOTAL)

BLOCK NAME: _motprocrescard_dn, PARENT BLOCK: _z11top_dn\



IN INT5 14C3<> 17A6<> 18C6<> 4C5^
IN INT4 13A7<> 14C3<> 18C6<> 4C5^
IN INT3 13A7<> 14D3<> 18C6<> 4D5^
IN INT2 13A7<> 18C6<> 4D5^

RESET_B OUT 13A4> 13B5<> 15C3<> 4C3^ 18A7< 19B1<

IN BTS_DUT 17C3<> 4B5^
IN BIS0_DUT 17C3<> 4C5^
IN BIS1_DUT 17C3<> 4B5^

TDO_NU OUT 19A6<> 4B4^
IN TCK_NU 19A6<> 4B4^
IN TDI_NU 19A6<> 4B4^
IN TMS_NU 19A6<> 4B4^

CS_X4 OUT 17A4<> 18B6<> 4C3^
CS_X5 OUT 17A4<> 18B6<> 4C3^
CS_X1 OUT 17B3<> 18B6<> 4D3^
CS_X2 OUT 17B3<> 18B6<> 4D3^
CS_X3 OUT 17A4<> 18B6<> 4C3^
WR OUT 17B3<> 4C3^
RW_X OUT 17B3<> 4C3^
WR_DUT OUT 17C3<> 18A6<> 4C3^
RD_DUT OUT 17C3<> 18A6<> 4C5^
A_DUT<11..0> OUT 4C5^ 17A6 18B7 18C6
17B7 4B3^XA<15..0> OUT
D_DUT<7..0> IO
XD<7..0> IO

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 5/7 (BLOCK) 18/71 (TOTAL)

U29

XILINX_XCF01S

U27

XC2S50_BGA

CONTROL

U31

MAX1792

J44

CONN_10P

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 7/7 (BLOCK) 19/71 (TOTAL)

DS21458 WAN INTERFACE BLOCK

I73
2.048MHZ_3.3V

YB02
OSC
1 — 1 VCC — 8 — V3_3
4 GND OUT — 5 — RB160 30 — MCLK — 46C7<
RB184 30 — MCLK2FPGA — 53B6<>

V3_3 — P4 P5 P6 C11 C12 C13 D3 E3 F3 L14 M14 N14 H1 J16 A9 T8 R6 T6 A11 B11 F1 F2 L15 L16
DVDD11 DVDD12 DVDD13 DVDD21 DVDD22 DVDD23 DVDD31 DVDD32 DVDD33 DVDD41 DVDD42 DVDD43 RVDD1 RVDD2 RVDD3 RVDD4 TVDD11 TVDD12 TVDD21 TVDD22 TVDD31 TVDD32 TVDD41 TVDD42

V3_3 — C42 10UF, C48 10UF, CR236 10UF, CR126 10UF, CR154 10UF, C103 10UF, C151 10UF, CR340 10UF, CR112 10UF

V3_3 — CR179 1 0.1UF 2, CR144 1 0.1UF 2, CR161 1 0.1UF 2, CR160 1 0.1UF 2, CR156 1 0.1UF 2, CR120 2 0.1UF 1, CR204 1 0.1UF 2, CR138 1 0.1UF 2, CR152 2 0.1UF 1

V3_3 — CR155 2 0.1UF 1, CR127 2 0.1UF 1, CR201 1 0.1UF 2, CR210 1 0.1UF 2

U20
DS21458_U

CONTROL

K14	JTRST	
52C1< 52C8<> 52A7<> XI_TMS	J15	JTMS
52C1< 52C8<> 52A7<> ONCE_TCK	K16	JTCLK
52C6<> JTD_FLASH_TDO	C10	JTDI
52A7<> JTD0458	K13	JTDO
55D5> 46A4<> OUT WAN_INT	H5	INT*
51D7< LIUC	D9	LIUC
46D7< MCLK	H4	MCLK1
	J12	MCLK2
	H9	RCLKI
	H10	RNEGI
	G8	RPOSI
	J14	TEST1
	J13	TEST2
46A1<> IN RESET_AH	K15	TSTRST
55A4< IN CS	M8	CS*
55A2<> 54C7<> IN RD	A10	RD*
55A3<> 54C7<> IN WR	C9	WR*
	N4	DVSS11
	N5	DVSS12
	N6	DVSS13
	D11	DVSS21
	D12	DVSS22
	D13	DVSS23

ADDR<9..0> IN 54C7 55A5 55A7

A<0>	H2	0
A<1>	E10	1
A<2>	H3	2
A<3>	G4	3
A<4>	N7	4
A<5>	B9	5
A<6>	T7	6
A<7>/ALE_A5	G2	7
A<8>	H6	8
A<9>	J11	9

DAT<7..0> IO 54C3 55A2 55A4

AD<0>	P8	0
AD<1>	D10	1
AD<2>	N8	2
AD<3>	P7	3
AD<4>	M7	4
AD<5>	R7	5
AD<6>	G1	6
AD<7>	G3	7

BTS	B10	BTS 51C7<
MUX	R8	MUX 51B7<
ESIBRD	H8	ESIBRD 51C7<
ESIBS<0>	J8	ESIBR0 51C7<
ESIBS<1>	J9	ESIBR1 51C7<

DVSS31 DVSS32 DVSS33 DVSS41 DVSS42 DVSS43 RVSS11 RVSS12 RVSS13 RVSS21 RVSS22 RVSS23 RVSS31 RVSS32 RVSS33 RVSS41 RVSS42 RVSS43 TVSS11 TVSS12 TVSS21 TVSS22 TVSS31 TVSS32 TVSS41 TVSS42 NC1 NC2 NC3
D4 E4 F4 L13 M13 N13 N1 J1 M1 E16 H16 D16 A5 A8 A4 T12 T13 T9 R5 T5 A12 B12 E1 E2 M15 M16 K9 P3 E9

I37
NA
NC7SZ86

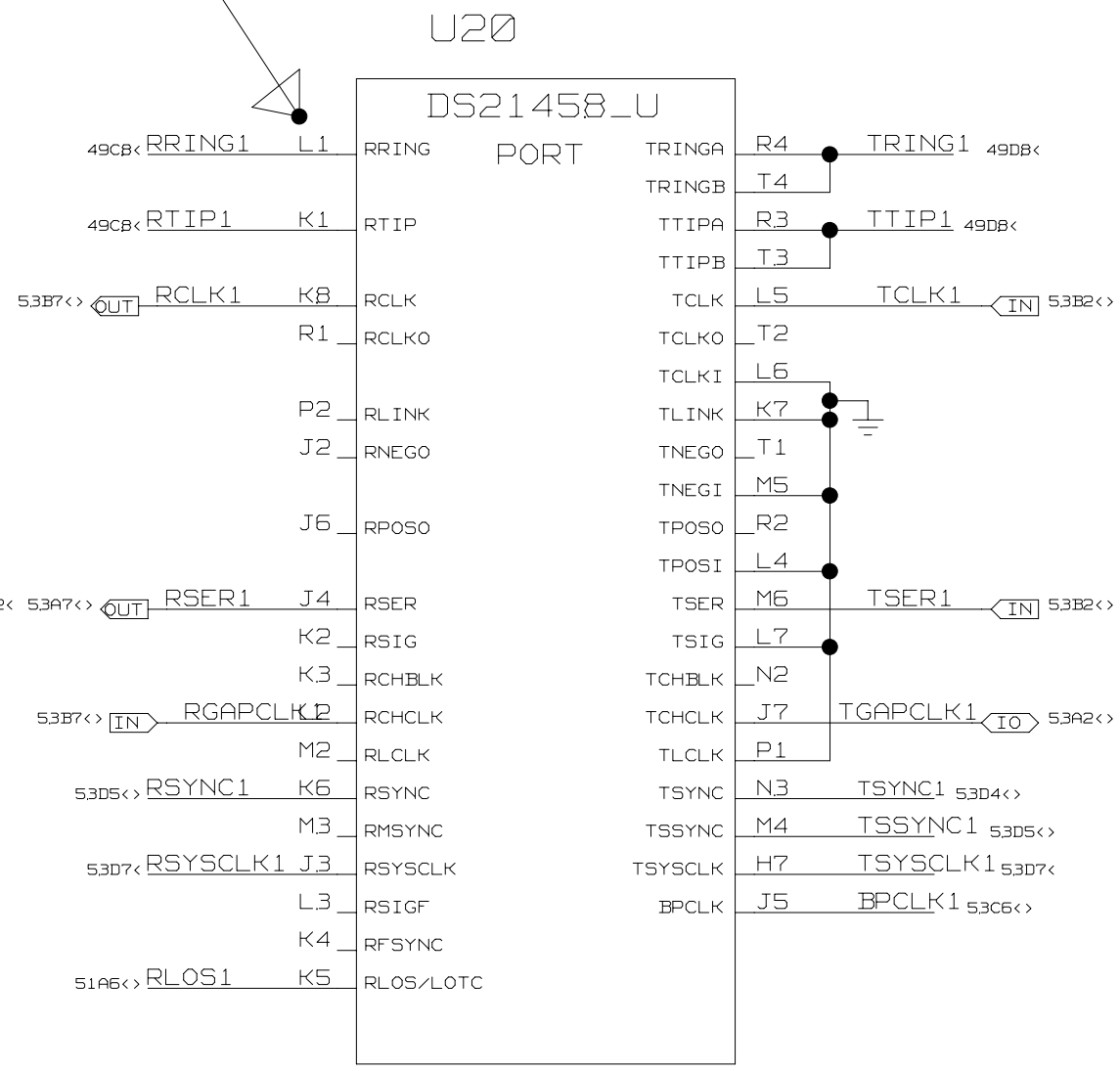
I41
NA
NC7SZ86
NC7SZB5_U
52B1< 55D6<> RESET_B — 1 UXB05 4 — RESET_AH 46B7<
INVERTER

V3_3 — RED DS25 — R1142 330 — 1 — 2 — NC7SZB6_U BUFFER WX11 — 4 — 1 — WAN_INT 46C7> 55D5>

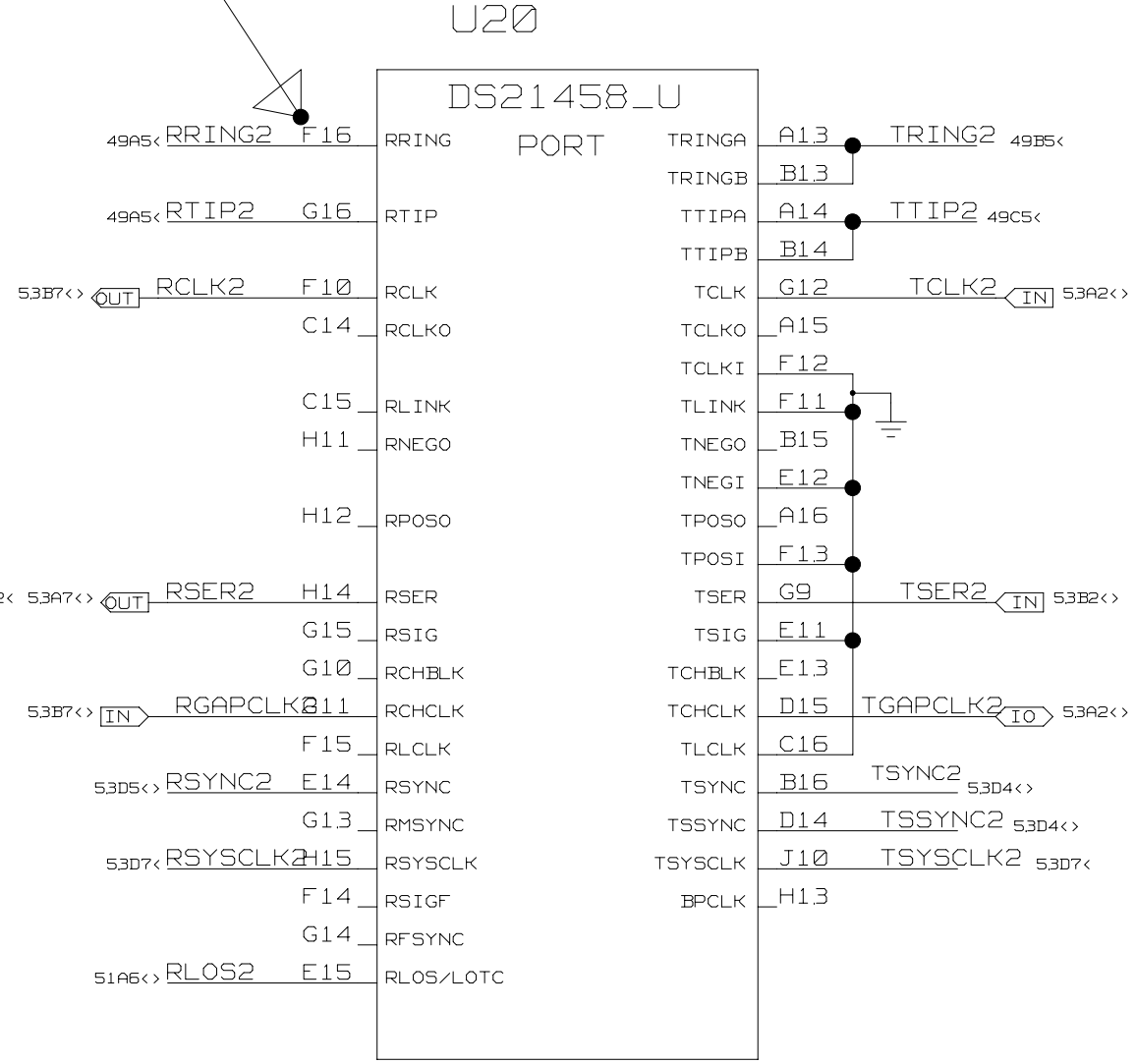
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 46/71<TOTAL>

CR-47 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_T11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_T1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE2

PORT1_RRING = PIN L1



PORT2_RRING = PIN F16



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/10 (BLOCK) 47/71 (TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-4B : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_T11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_T1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE3

PORT3_RRING = PIN A6

U20

DS21458_U

PORT

50C8<	RRING3	A6	RRING	TRINGA	D1	TRING3	50D8<
				TRINGB	D2		
50C8<	RTIP3	A7	RTIP	TTIPA	C1	TTIP3	50D8<
				TTIPB	C2		
53B7<> OUT	RCLK3	G5	RCLK	TCLK	F6	TCLK3 IN	53A2<>
		A2	RCLKO	TCLKO	B2		
				TCLKI	F7		
		C3	RLINK	TLINK	G7		
		F8	RNEGO	TNEGO	A1		
				TNEGI	E5		
		F9	RPOSO	TPOSO	B1		
				TPOSI	D5		
53C2< 53A7<> OUT	RSER3	C8	RSER	TSER	G6	TSER3 IN	53B2<>
		B7	RSIG	TSIG	F5		
		C7	RCHBLK	TCHBLK	C5		
53B7<> IN	RGAPCLK3	D7	RCHCLK	TCHCLK	B4	TGAPCLK3 IO	53A2<>
		B6	RLCLK	TLCLK	C4		
53D4<>	RSYNC3	B5	RSYNC	TSYNC	B3	TSYNC3	53D4<>
		E6	RMSYNC	TSSYNC	A3	TSSYNC3	53D4<>
53D7<	RSYSCLK3	B8	RSYSCLK	TSYSCLK	D8	TSYSCLK3	53C7<
		E7	RSIGF	BPCLK	E8		
		C6	RFSYNC				
51A6<>	RLOS3	D6	RLOS/LOTC				

PORT4_RRING = PIN T11

U20

DS21458_U

PORT

50A5<	RRING4	T11	RRING	TRINGA	N15	TRING4	50B5<
				TRINGB	N16		
50A5<	RTIP4	T10	RTIP	TTIPA	P15	TTIP4	50C5<
				TTIPB	P16		
53B7<> OUT	RCLK4	K12	RCLK	TCLK	L9	TCLK4 IN	53A2<>
		P14	RCLKO	TCLKO	R16		
				TCLKI	L11		
		T15	RLINK	TLINK	L12		
		P10	RNEGO	TNEGO	T16		
				TNEGI	M12		
		N10	RPOSO	TPOSO	R15		
				TPOSI	L10		
53C2< 53A7<> OUT	RSER4	P9	RSER	TSER	K10	TSER4 IN	53B2<>
		R10	RSIG	TSIG	K11		
		R11	RCHBLK	TCHBLK	R13		
53B7<> IN	RGAPCLK4	M9	RCHCLK	TCHCLK	P13	TGAPCLK4 IO	53A2<>
		R12	RLCLK	TLCLK	T14		
53D4<>	RSYNC4	N12	RSYNC	TSYNC	R14	TSYNC4	53D4<>
		M10	RMSYNC	TSSYNC	M11	TSSYNC4	53D4<>
53D7<	RSYSCLK4	R9	RSYSCLK	TSYSCLK	L8	TSYSCLK4	53C7<
		N11	RSIGF	BPCLK	N9		
		P11	RFSYNC				
51A6<>	RLOS4	P12	RLOS/LOTC				

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:3/10(BLOCK) 48/71(TOTAL)

BLOCK NAME: _quadte1wan_dn, PARENT BLOCK: _wan4z44_dn\

CR-49 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_I1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE4

TTIP1 R2082 C176 1UF XMIT L10 I11

TRING1 R2072

I13 RJ45_4PORT JB12 RJ45

RTIP1 RB3282 RCV I14

RRING1 RB3272

RB313 2.61R RB315 2.61R

CB395 0.1UF

47C2 TTIP2 R2042 C173 1UF XMIT L10 I2

47C2 TRING2 R2032

I25 RJ45_4PORT JB12 RJ45

47C4 RTIP2 RB3222 RCV I26

47C4 RRING2 RB3212

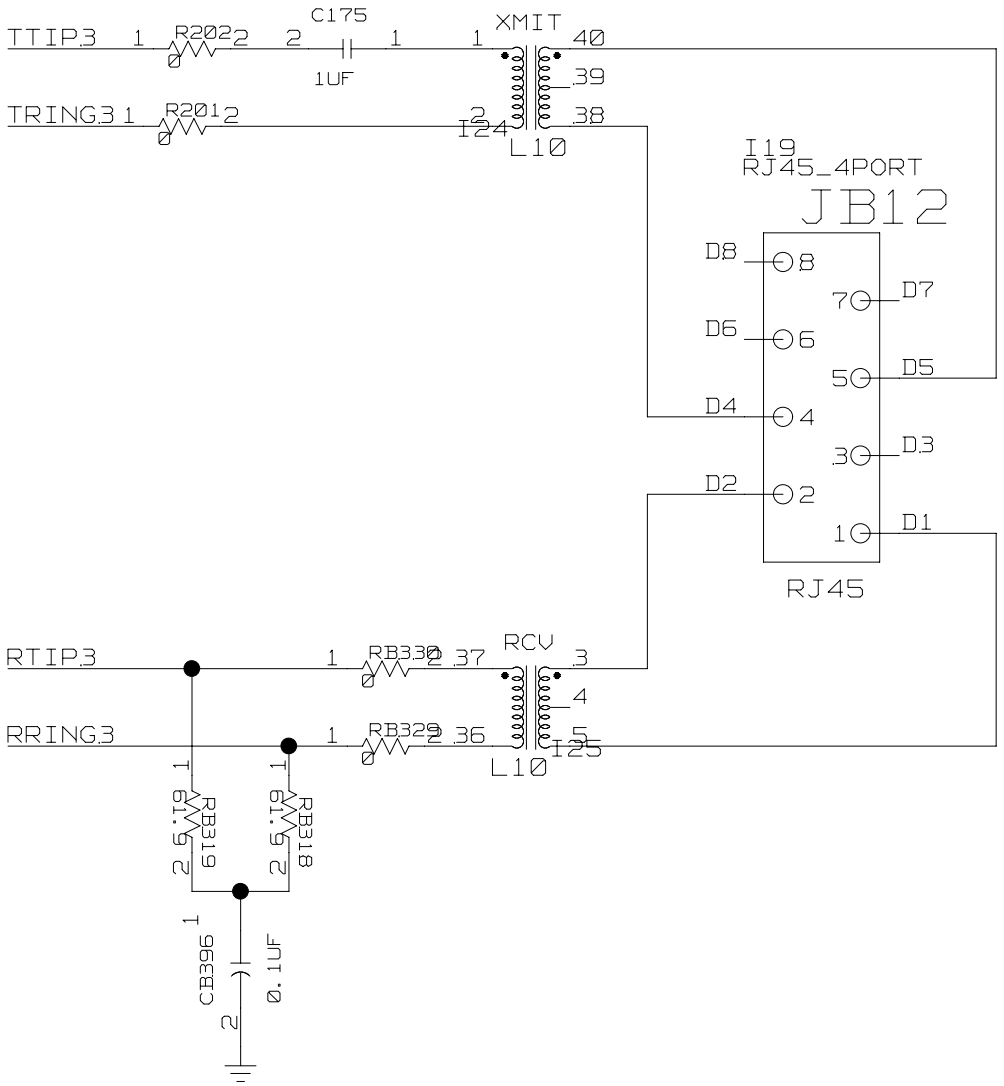
RB313 2.61R RB312 2.61R

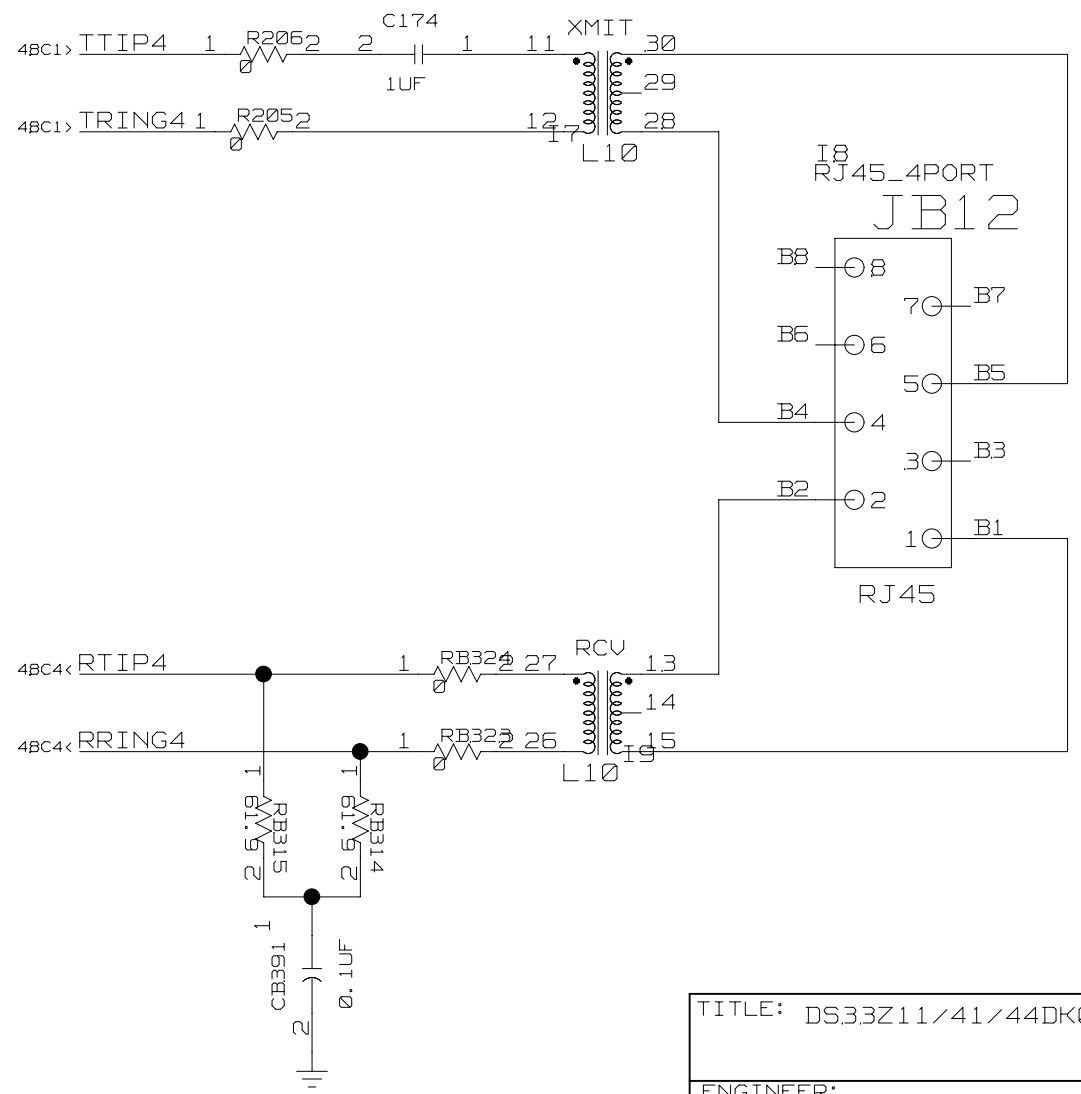
CB390 0.1UF

THE PCB LAYOUT INCORRECTLY USES PINS 38-40, 33-35, 28-30 AND 23-25
AS THE TX PRIMARY. THIS HAS BEEN CORRECTED IN THE SCHEMATIC,
THE PCB / ASSEMBLY HAS BEEN MODIFIED TO ACCOMMODATE THIS.

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:4/10(BLOCK) 49/71(TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\



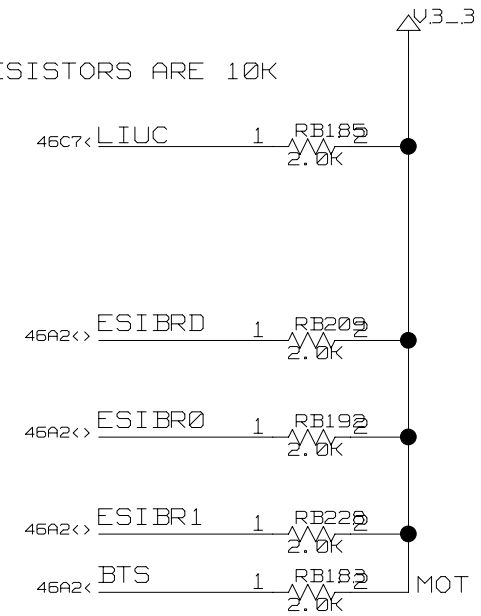


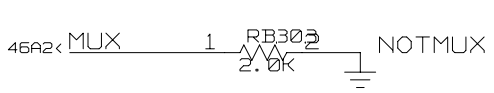
THE PCB LAYOUT INCORRECTLY USES PINS 38-40, 33-35, 28-30 AND 23-25 AS THE TX PRIMARY. THIS HAS BEEN CORRECTED IN THE SCHEMATIC, THE PCB / ASSEMBLY HAS BEEN MODIFIED TO ACCOMMODATE THIS.

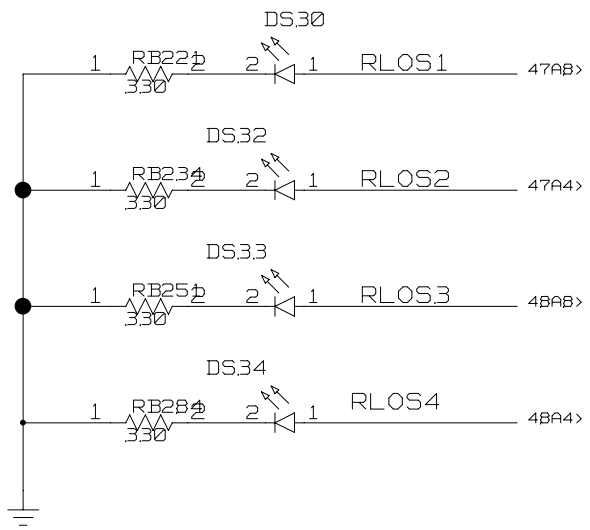
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 5/10(BLOCK) 50/71(TOTAL)

CR-51 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_T11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_T1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE5

ALL UNMARKED BIAS RESISTORS ARE 10K



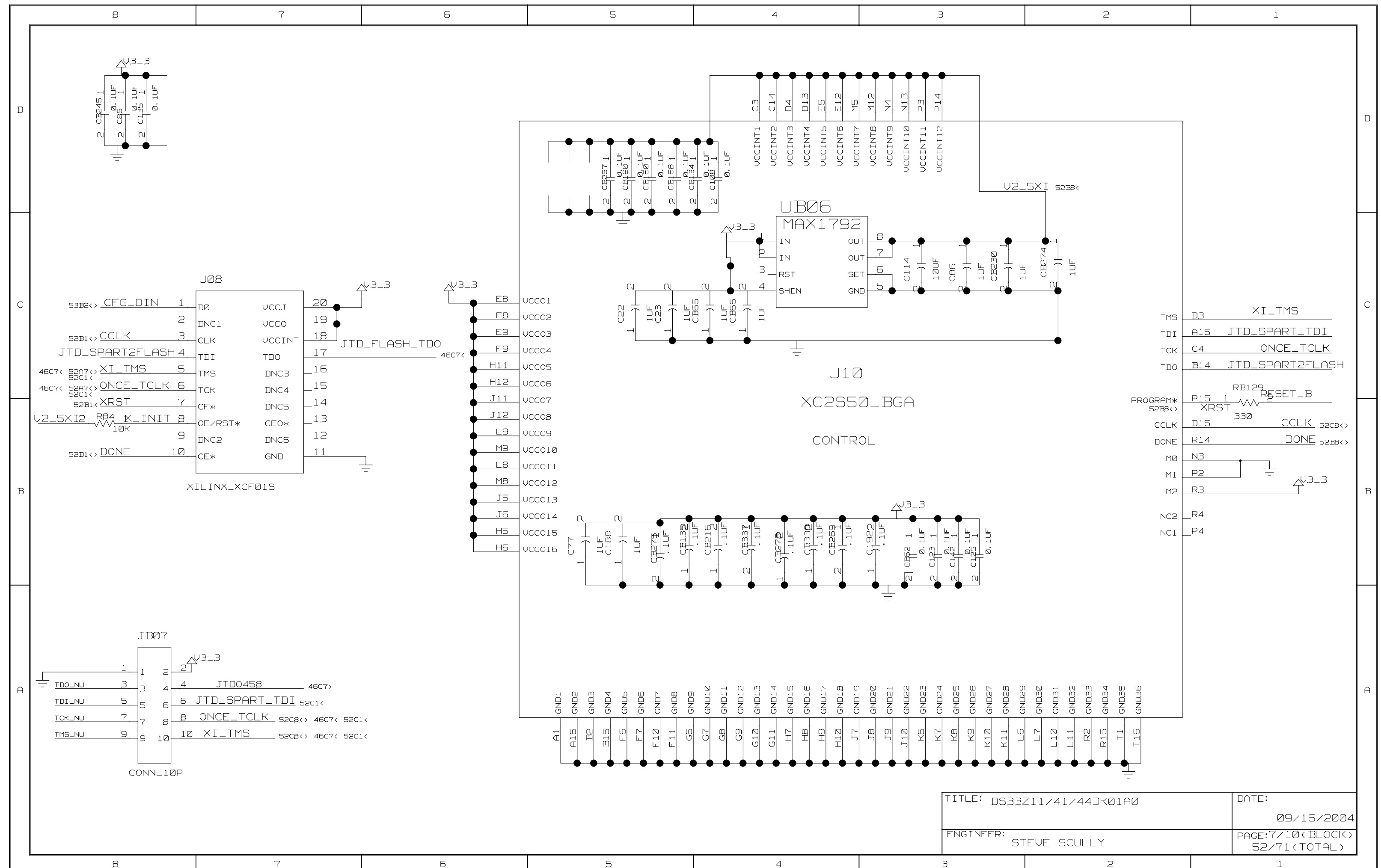




TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:6/10(BLOCK) 51/71(TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-52 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_T11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_T1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE7



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 7/10 (BLOCK) 52/71 (TOTAL)

BLOCK NAME: _quadte1wan_dn, PARENT BLOCK: _wan4z44_dn\

47B8< RSYSCLK1
47B4< RSYSCLK2
4BB8< RSYSCLK3
4BB4< RSYSCLK4
RSYSCLK

47B6< TSYSCLK1
47B2< TSYSCLK2
4BB5< TSYSCLK3
4BB1< TSYSCLK4
TSYSCLK

BANK 1

	C9	GCK2	
	B13	IO1_1\CS*	
	C13	IO2_1\WRITE*	
	A14	IO3_1	
	C11	IO4_1\VREF	
	E11	IO5_1	
	B11	IO6_1	RSYNC1 47B8<>
	A11	IO7_1	TSYNC1 47B6<
	C10	IO8_1	
	B9	IO9_1\VREF	
	D9	IO10_1	RSYNC2 47B4<>
	A8	IO11_1	TSYNC2 47B2<
	C12	IO12_1	RSYNC3 4BB8<>
	D12	IO13_1	TSYNC3 4BB5<
	B12	IO14_1	RSYNC4 4BB4<>
	A13	IO15_1	TSYNC4 4BB1<
	D11	IO16_1	
	A12	IO17_1	TSYNC1 47B6<>
	B10	IO18_1	TSYNC2 47B2<>
	D10	IO19_1	TSYNC3 4BB5<>
	A10	IO20_1	TSYNC4 4BB1<>
	E10	IO21_1	
	A9	IO22_1	

47B6> BPCLK1

B8	GCK3	
A7	IO1_0	
B7	IO2_0\VREF	
C7	IO3_0	
B6	IO4_0	
A5	IO5_0	46D7< MCLK2FPGA
C6	IO6_0	
B4	IO7_0\VREF	
A3	IO8_0	47B8< RGAPCLK1
B3	IO9_0	47B4< RGAPCLK2
D8	IO10_0	4BB8< RGAPCLK3
A6	IO11_0	4BB4< RGAPCLK4
C8	IO12_0	47C8> RCLK1
D7	IO13_0	47C4> RCLK2
E7	IO14_0	4BC8> RCLK3
B5	IO15_0	4BC4> RCLK4
D6	IO16_0	53C2< 47B8> RSER1
A4	IO17_0	53C2< 47B4> RSER2
E6	IO18_0	53C2< 4BB8> RSER3
D5	IO19_0	53C2< 4BB4> RSER4
C5	IO20_0	

U10

XC2S50_BGA

BANK 0

BANK 2

IO2_1\IRDY	H16	
IO2_2\VREF	H15	
IO3_2\D3	G16	
IO4_2	H13	
IO5_2	G13	
IO6_2\D2	F15	
IO7_2\D1	E16	SPARE_TP1 TP32
IO8_2	F14	SPARE_TP2 TP30
IO9_2	D16	
IO10_2\VREF	F13	
IO11_2	E13	TSER1 47B5<
IO12_2\<DIN,D0>	D14	CFG_DIN 52C8<>
IO13_2\<DOUT,BUSY>	C15	
IO14_2	H14	TSER2 47B1<
IO15_2	J13	TSER3 4BB5<
IO16_2	G14	TSER4 4BB1<
IO17_2	G15	TCLK1 47C5<
IO18_2	G12	TCLK2 47C1<
IO19_2	F16	TCLK3 4BC5<
IO20_2	F12	TCLK4 4BC1<
IO21_2	E15	TGAPCLK1 47B5<>
IO22_2	E14	TGAPCLK2 47B1<>
IO23_2	C16	TGAPCLK3 4BB5<>
IO24_2	B16	TGAPCLK4 4BB1<>

BANK 3

N15	IO1_3\INIT*	
N14	IO2_3\D7	
M13	IO3_3	
L14	IO4_3\VREF	
P16	IO5_3	
L13	IO6_3	
N16	IO7_3\D6	
M16	IO8_3\D5	
K14	IO9_3	
K16	IO10_3\VREF	
J16	IO11_3\D4	
K15	IO12_3	
J15	IO13_3\TRDY	
T15	IO14_3	
R16	IO15_3	
M14	IO16_3	
M15	IO17_3	
L12	IO18_3	
L16	IO19_3	
K13	IO20_3	
L15	IO21_3	
K12	IO22_3	
J14	IO23_3	

X_INIT
52B8<>

TSER PULLDNS USED IN IBO MODE
(IMPLEMENTS IMUX)

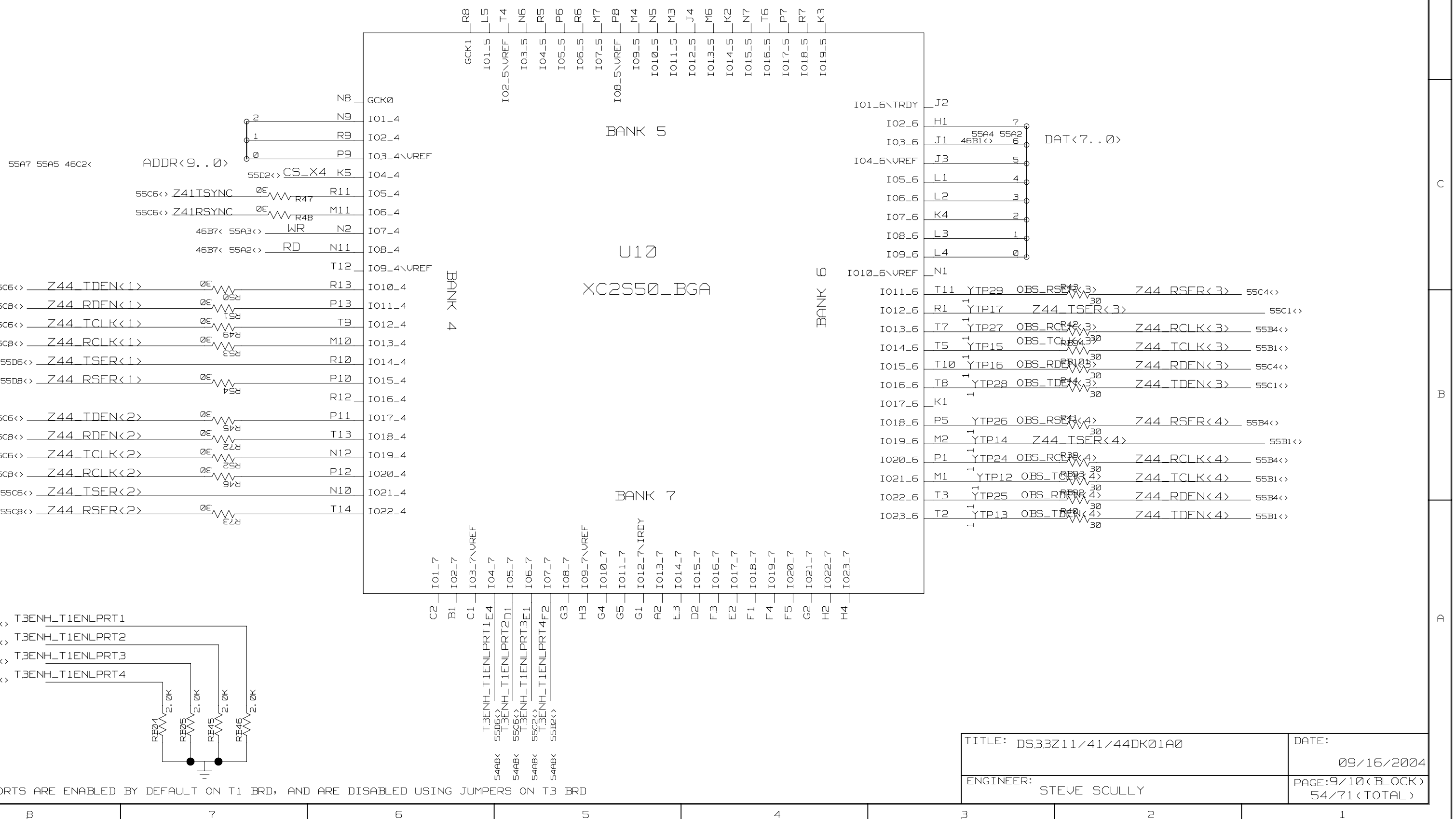
53A7<> 47B8> RSER1
53A7<> 47B4> RSER2
53A7<> 4BB8> RSER3
53A7<> 4BB4> RSER4

R88 2.0K
R113 2.0K
R104 2.0K
R94 2.0K

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:8/10(BLOCK) 53/71(TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-54 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_T11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_T1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE9



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:9/10(BLOCK) 54/71(TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-55 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_I1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE10

V3_3
V3_3
GND

RECEPTACLE
P2 CONNECTOR (RECEPTICAL)

J12

VDD

I28
INT3 — WAN_INT 46A4<> 46C7>

INT5
55D6<> INT2
RESET_B 46A2<> 52B1<
INT2 55D7<>

54B8< Z44_RSER<1> — T3ENH_T1ENLPRT1 54A6<> 54AB<
Z44_TSER<1> 54B8<>
54B8< Z44_RDEN<1> — SIG_RETURN 55A1> 55B2<> 55C6<>
Z44_TDEN<1> 54B8<
54B8< Z44_RCLK<1> — Z44_TCLK<1> 54B8<
Z41RSYNC 54C7<
Z41TSYNC 54C7<
T3ENH_T1ENLPRT2 54A5<> 54AB<
54AB< Z44_RSER<2> — SIG_RETURN 55A1> 55B2<> 55C6<>
Z44_TSER<2> 54B8<>
54B8< Z44_RDEN<2> — Z44_TDEN<2> 54B8<
54B8< Z44_RCLK<2> — Z44_TCLK<2> 54B8<

TDO_NU 52AB<>
TCK_NU 52AB<>
52AB<> TDI_NU
52AB<> TMS_NU

ADDR<9..0> — ADDR<9..0> 46C2< 54C7 55A7
55A2 54C3 46B1<>

55A5
46C2< 54C7

OSC2_NU
OSC4_NU
OSC3_NU

P1 CONNECTOR (RECEPTICAL)
RECEPTACLE

J09

ALE
CS_X4 54C7<>
CS_X5

54B1< Z44_RSER<3> — T3ENH_T1ENLPRT3 54A5<> 54AB<
Z44_TSER<3> 54B1<>
54B1< Z44_RDEN<3> — Z44_TDEN<3> 54B1<
54B1< Z44_RCLK<3> — Z44_TCLK<3> 54B1<
T3ENH_T1ENLPRT4 54A5<> 54AB<
54B1< Z44_RSER<4> — Z44_TSER<4> 54B1<>
54B1< Z44_RDEN<4> — Z44_TDEN<4> 54A1<
54B1< Z44_RCLK<4> — SIG_RETURN 55A1> 55C6<>
Z44_TCLK<4> 54B1<

DAT<7..0> — DAT<7..0>
55A4
54C3 46B1<>

46B7< CS — CS_X2
CS_X3
46B7< 54C7<> WR
RD 54C7<> 46B7<

NOTE 3184 IS ON CS3 WHILE 21455 IS ON CS2/CS4

WAN R.C. CONNECTOR TO MOTHERBOARD

I27
GND — SIG_RETURN

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 10/10 (BLOCK) 55/71 (TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\