

## LM5104 High Voltage Half-Bridge Gate Driver with Adaptive Delay

Check for Samples: [LM5104](#)

### FEATURES

- Drives Both a High Side and Low Side N-Channel MOSFET
- Adaptive Rising and Falling Edges with Programmable Additional Delay
- Single Input Control
- Bootstrap Supply Voltage Range up to 118V DC
- Fast Turn-Off Propagation Delay (25 ns Typical)
- Drives 1000 pF Loads with 15 ns Rise and Fall Times
- Supply Rail Under-Voltage Lockout

### TYPICAL APPLICATIONS

- Current Fed Push-Pull Power Converters
- High Voltage Buck Regulators
- Active Clamp Forward Power Converters
- Half and Full Bridge Converters

### DESCRIPTION

The LM5104 High Voltage Gate Driver is designed to drive both the high side and the low side N-Channel MOSFETs in a synchronous buck configuration. The floating high-side driver is capable of working with supply voltages up to 100V. The high side and low side gate drivers are controlled from a single input. Each change in state is controlled in an adaptive manner to prevent shoot-through issues. In addition to the adaptive transition timing, an additional delay time can be added, proportional to an external setting resistor. An integrated high voltage diode is provided to charge high side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high side gate driver. Under-voltage lockout is provided on both the low side and the high side power rails. This device is available in the standard SOIC and the WSON packages.

### PACKAGE

- SOIC
- WSON-10 (4 mm x 4 mm)



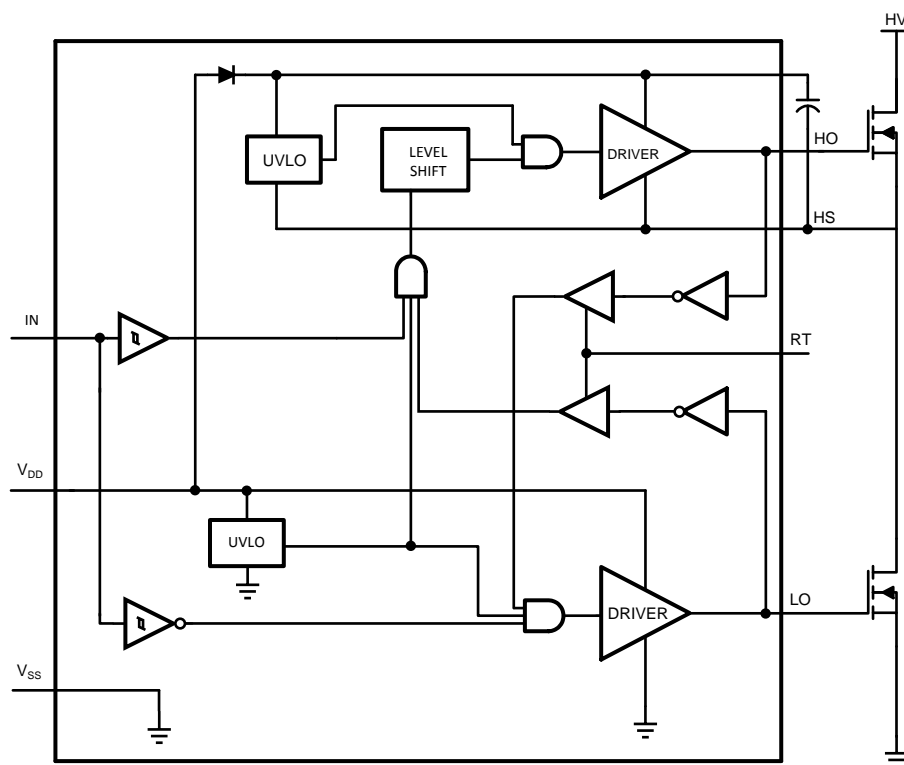
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

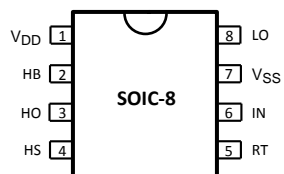
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2004–2013, Texas Instruments Incorporated

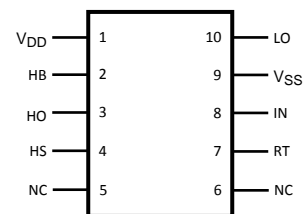
### SIMPLIFIED BLOCK DIAGRAM



## Connection Diagram



**Figure 1. 8-Lead SOIC  
See D Package**



**Figure 2. 10-Lead WSON  
See DPR0010A Package**

### PIN DESCRIPTIONS

Pin		Name	Description	Application Information
SOIC	WSON			
1	1	V <sub>DD</sub>	Positive gate drive supply	Locally decouple to V <sub>SS</sub> using ESR/ESL capacitor, located as close to IC as possible.
2	2	HB	High side gate driver bootstrap rail	Connect the positive terminal to bootstrap capacitor to the HB pin and connect negative terminal to HS. The Bootstrap capacitor should be placed as close to IC as possible
3	3	HO	High side gate driver output	Connect to gate of high side MOSFET with short low inductance path.
4	4	HS	Highside MOSFET source connection	Connect to bootstrap capacitor negative terminal and source of high side MOSFET.
5	7	RT	Deadtime programming pin	Resistor from RT to ground programs the deadtime between high and low side transitions. The resistor should be located close to the IC to minimize noise coupling from adjacent traces.
6	8	IN	Control input	Logic 1 equals High Side ON and Low Side OFF. Logic 0 equals High Side OFF and Low Side ON.
7	9	V <sub>SS</sub>	Ground return	All signals are referenced to this ground.
8	10	LO	Low side gate driver output	Connect to the gate of the low side MOSFET with a short low inductance path.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)</sup>

V <sub>DD</sub> to V <sub>SS</sub>	–0.3V to +18V
V <sub>HB</sub> to V <sub>HS</sub>	–0.3V to +18V
IN to V <sub>SS</sub>	–0.3V to V <sub>DD</sub> + 0.3V
LO Output	–0.3V to V <sub>DD</sub> + 0.3V
HO Output	V <sub>HS</sub> – 0.3V to V <sub>HB</sub> + 0.3V
V <sub>HS</sub> to V <sub>SS</sub>	–1V to +100V
V <sub>HB</sub> to V <sub>SS</sub>	118V
RT to V <sub>SS</sub>	–0.3V to 5V
Junction Temperature	+150°C
Storage Temperature Range	–55°C to +150°C
ESD Rating HBM <sup>(3)</sup>	2 kV

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see [Electrical Characteristics](#).
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. 2 kV for all pins except Pin 2, Pin 3 and Pin 4 which are rated at 500V.

### Recommended Operating Conditions

V <sub>DD</sub>	+9V to +14V
HS	–1V to 100V
HB	V <sub>HS</sub> + 8V to V <sub>HS</sub> + 14V
HS Slew Rate	< 50V/ns
Junction Temperature	–40°C to +125°C

## Electrical Characteristics

Specifications in standard typeface are for  $T_J = +25^\circ\text{C}$ , and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified,  $V_{DD} = V_{HB} = 12\text{V}$ ,  $V_{SS} = V_{HS} = 0\text{V}$ ,  $R_T = 100\text{k}\Omega$ . No Load on LO or HO.

Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Typ	Max <sup>(1)</sup>	Units
<b>SUPPLY CURRENTS</b>						
$I_{DD}$	$V_{DD}$ Quiescent Current	$LI = HI = 0\text{V}$		0.4	<b>0.6</b>	mA
$I_{DDO}$	$V_{DD}$ Operating Current	$f = 500\text{ kHz}$		1.9	<b>3</b>	mA
$I_{HB}$	Total HB Quiescent Current	$LI = HI = 0\text{V}$		0.06	<b>0.2</b>	mA
$I_{HBO}$	Total HB Operating Current	$f = 500\text{ kHz}$		1.3	<b>3</b>	mA
$I_{HBS}$	HB to $V_{SS}$ Current, Quiescent	$V_{HS} = V_{HB} = 100\text{V}$		0.05	<b>10</b>	$\mu\text{A}$
$I_{HBSO}$	HB to $V_{SS}$ Current, Operating	$f = 500\text{ kHz}$		0.08		mA
<b>INPUT PINS</b>						
$V_{IL}$	Low Level Input Voltage Threshold		<b>0.8</b>	1.8		V
$V_{IH}$	High Level Input Voltage Threshold			1.8	<b>2.2</b>	V
$R_I$	Input Pulldown Resistance		<b>100</b>	200	<b>500</b>	k $\Omega$
<b>TIME DELAY CONTROLS</b>						
$V_{RT}$	Nominal Voltage at RT		<b>2.7</b>	3	<b>3.3</b>	V
$I_{RT}$	RT Pin Current Limit	$RT = 0\text{V}$	<b>0.75</b>	1.5	<b>2.25</b>	mA
$T_{D1}$	Delay Timer, $RT = 10\text{ k}\Omega$		<b>58</b>	90	<b>130</b>	ns
$T_{D2}$	Delay Timer, $RT = 100\text{ k}\Omega$		<b>140</b>	200	<b>270</b>	ns
<b>UNDER VOLTAGE PROTECTION</b>						
$V_{DDR}$	$V_{DD}$ Rising Threshold		<b>6.0</b>	6.9	<b>7.4</b>	V
$V_{DDH}$	$V_{DD}$ Threshold Hysteresis			0.5		V
$V_{HBR}$	HB Rising Threshold		<b>5.7</b>	6.6	<b>7.1</b>	V
$V_{HBH}$	HB Threshold Hysteresis			0.4		V
<b>BOOT STRAP DIODE</b>						
$V_{DL}$	Low-Current Forward Voltage	$I_{VDD-HB} = 100\text{ }\mu\text{A}$		0.60	<b>0.9</b>	V
$V_{DH}$	High-Current Forward Voltage	$I_{VDD-HB} = 100\text{ mA}$		0.85	<b>1.1</b>	V
$R_D$	Dynamic Resistance	$I_{VDD-HB} = 100\text{ mA}$		0.8	<b>1.5</b>	$\Omega$
<b>LO GATE DRIVER</b>						
$V_{OLL}$	Low-Level Output Voltage	$I_{LO} = 100\text{ mA}$		0.25	<b>0.4</b>	V
$V_{OHL}$	High-Level Output Voltage	$I_{LO} = -100\text{ mA}$ $V_{OHL} = V_{DD} - V_{LO}$		0.35	<b>0.55</b>	V
$I_{OHL}$	Peak Pullup Current	$V_{LO} = 0\text{V}$		1.6		A
$I_{OLL}$	Peak Pulldown Current	$V_{LO} = 12\text{V}$		1.8		A
<b>HO GATE DRIVER</b>						
$V_{OLH}$	Low-Level Output Voltage	$I_{HO} = 100\text{ mA}$		0.25	<b>0.4</b>	V
$V_{OHH}$	High-Level Output Voltage	$I_{HO} = -100\text{ mA}$ , $V_{OHH} = V_{HB} - V_{HO}$		0.35	<b>0.55</b>	V
$I_{OHH}$	Peak Pullup Current	$V_{HO} = 0\text{V}$		1.6		A
$I_{OLH}$	Peak Pulldown Current	$V_{HO} = 12\text{V}$		1.8		A
<b>THERMAL RESISTANCE</b>						
$\theta_{JA}^{(2)}$	Junction to Ambient	SOIC		170		$^\circ\text{C/W}$
		WSN <sup>(3)</sup>		40		

- (1) Min and Max limits are 100% production tested at  $25^\circ\text{C}$ . Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
- (2) The  $\theta_{JA}$  is not a given constant for the package and depends on the printed circuit board design and the operating environment.
- (3) 4 layer board with Cu finished thickness 1.5/1/1/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50mm ground and power planes embedded in PCB. See Application Note AN-1187.

## Switching Characteristics

Specifications in standard typeface are for  $T_J = +25^\circ\text{C}$ , and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified,  $V_{DD} = V_{HB} = 12\text{V}$ ,  $V_{SS} = V_{HS} = 0\text{V}$ , No Load on LO or HO.

Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Typ	Max <sup>(1)</sup>	Units
$t_{LPHL}$	Lower Turn-Off Propagation Delay (IN Rising to LO Falling)			25	<b>56</b>	ns
$t_{HPLH}$	Upper Turn-Off Propagation Delay (IN Falling to HO Falling)			25	<b>56</b>	ns
$t_{RC}, t_{FC}$	Either Output Rise/Fall Time	$C_L = 1000\text{ pF}$		15		ns
$t_R, t_F$	Either Output Rise/Fall Time (3V to 9V)	$C_L = 0.1\text{ }\mu\text{F}$		0.6		$\mu\text{s}$
$t_{BS}$	Bootstrap Diode Turn-Off Time	$I_F = 20\text{ mA}, I_R = 200\text{ mA}$		50		ns

- (1) Min and Max limits are 100% production tested at  $25^\circ\text{C}$ . Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

## Typical Performance Characteristics

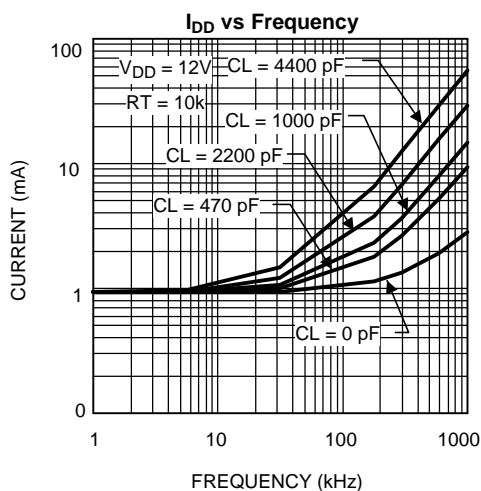


Figure 3.

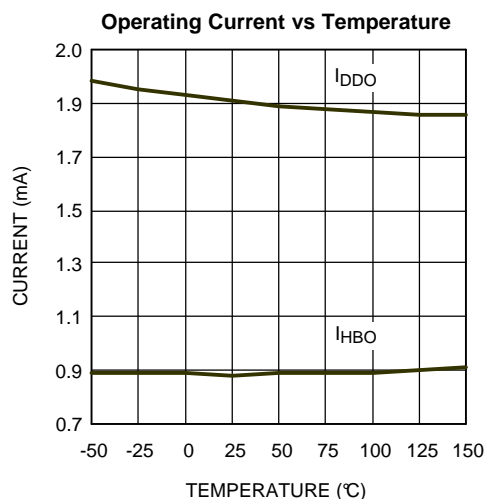


Figure 4.

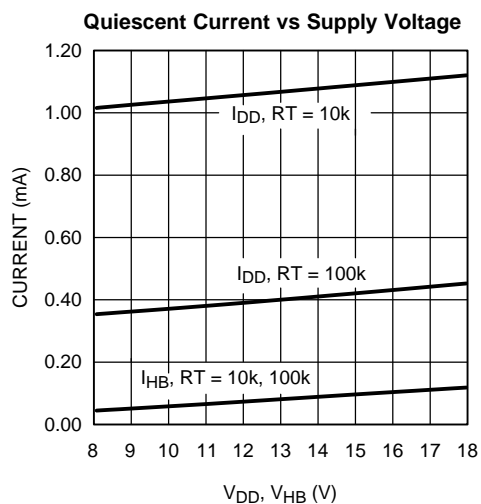


Figure 5.

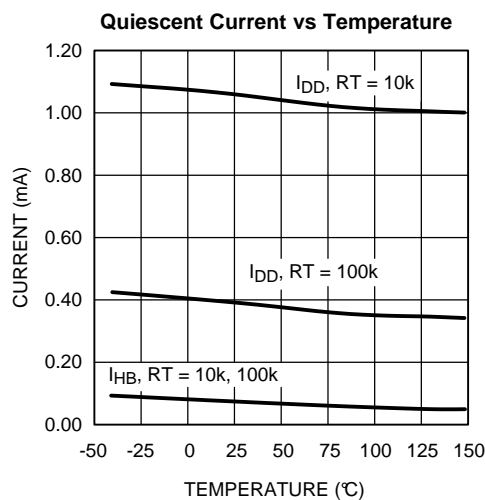


Figure 6.

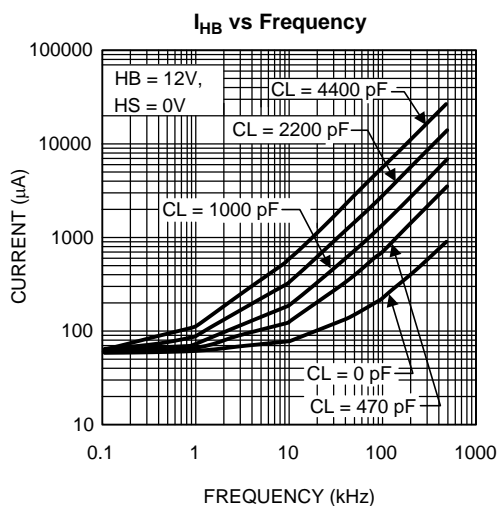


Figure 7.

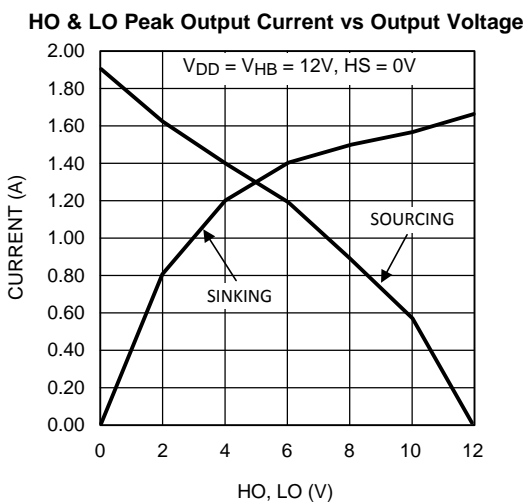


Figure 8.

## Typical Performance Characteristics (continued)

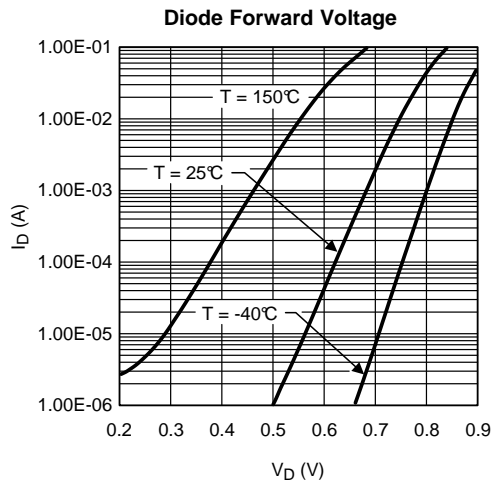


Figure 9.

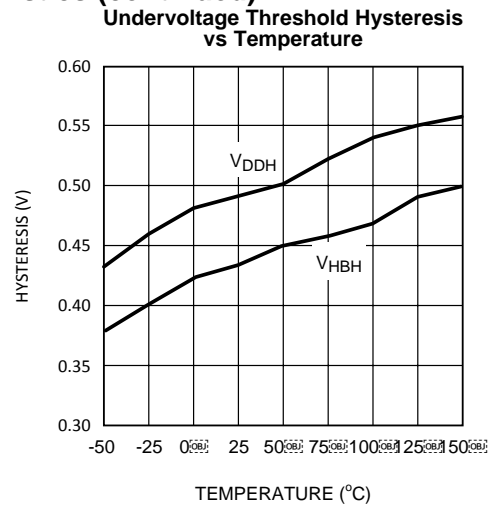


Figure 10.

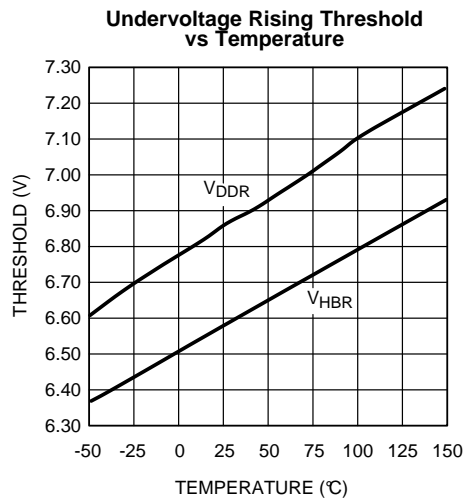


Figure 11.

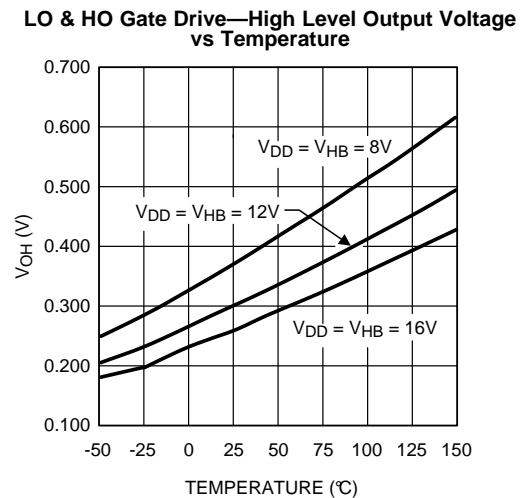


Figure 12.

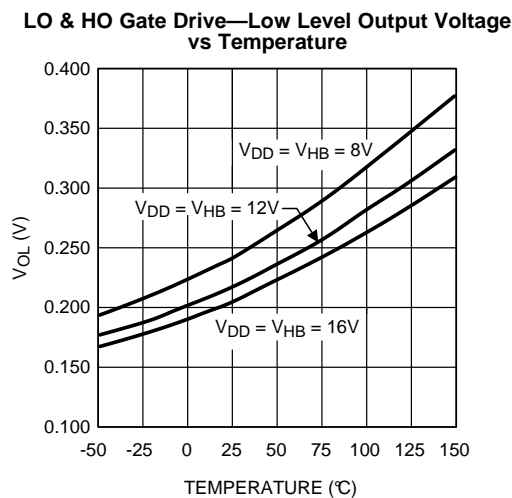


Figure 13.

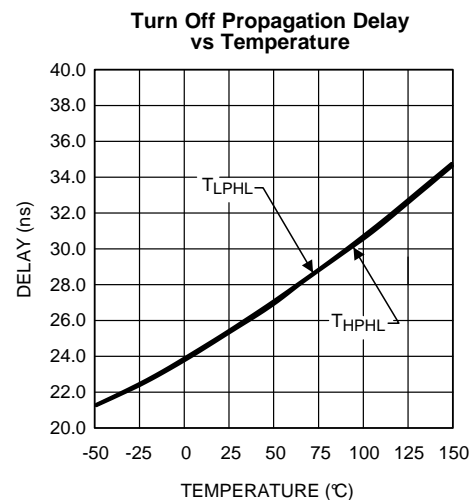


Figure 14.

## Typical Performance Characteristics (continued)

Timing vs Temperature RT = 10K

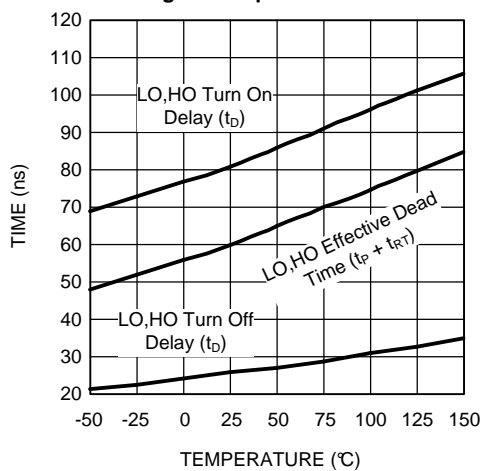


Figure 15.

Timing vs Temperature RT = 100K

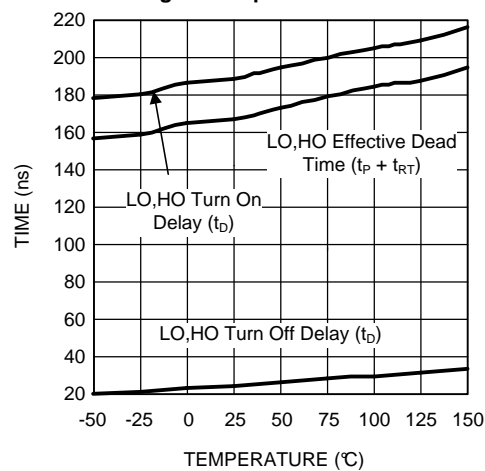


Figure 16.

Turn On Delay vs RT Resistor Value

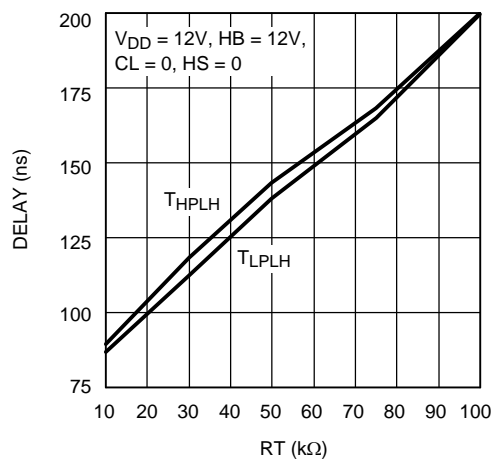


Figure 17.



## LM5104 Waveforms

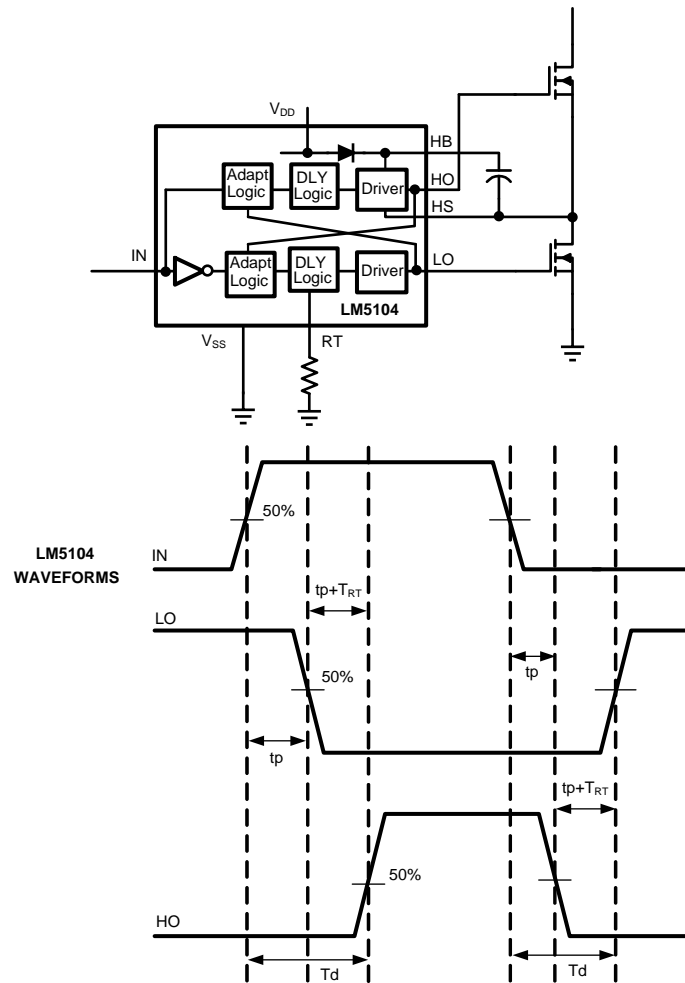


Figure 18. Application Timing Waveforms

## OPERATIONAL DESCRIPTION

### ADAPTIVE SHOOT-THROUGH PROTECTION

LM5104 is a high voltage, high speed dual output driver designed to drive top and bottom MOSFET's connected in synchronous buck or half-bridge configuration, from one externally provided PWM signal. LM5104 features adaptive delay to prevent shoot-through current through top and bottom MOSFETs during switching transitions. Referring to the timing diagram [Figure 18](#), the rising edge of the PWM input (IN) turns off the bottom MOSFET (LO) after a short propagation delay ( $t_p$ ). An adaptive circuit in the LM5104 monitors the bottom gate voltage (LO) and triggers a programmable delay generator when the LO pin falls below an internally set threshold ( $\approx V_{dd}/2$ ). The gate drive of the upper MOSFET (HO) is disabled until the deadtime expires. The upper gate is enabled after the TIMER delay ( $t_p + T_{RT}$ ), and the upper MOSFET turns-on. The additional delay of the timer prevents lower and upper MOSFETs from conducting simultaneously, thereby preventing shoot-through.

A falling transition on the PWM signal (IN) initiates the turn-off of the upper MOSFET and turn-on of the lower MOSFET. A short propagation delay ( $t_p$ ) is encountered before the upper gate voltage begins to fall. Again, the adaptive shoot-through circuitry and the programmable deadtime TIMER delays the lower gate turn-on time. The upper MOSFET gate voltage is monitored and the deadtime delay generator is triggered when the upper MOSFET gate voltage with respect to ground drops below an internally set threshold ( $\approx V_{dd}/2$ ). The lower gate drive is momentarily disabled by the timer and turns on the lower MOSFET after the deadtime delay expires ( $t_p + T_{RT}$ ).

The RT pin is biased at 3V and current limited to 1mA. It is designed to accommodate a resistor between 5K and 100K, resulting in an effective dead-time proportional to RT and ranging from 90ns to 200ns. RT values below 5K will saturate the timer and are not recommended.

### Startup and UVLO

Both top and bottom drivers include under-voltage lockout (UVLO) protection circuitry which monitors the supply voltage ( $V_{DD}$ ) and bootstrap capacitor voltage ( $V_{HB} - V_{HS}$ ) independently. The UVLO circuit inhibits each driver until sufficient supply voltage is available to turn-on the external MOSFETs, and the built-in hysteresis prevents chattering during supply voltage transitions. When the supply voltage is applied to  $V_{DD}$  pin of LM5104, the top and bottom gates are held low until  $V_{DD}$  exceeds UVLO threshold, typically about 6.9V. Any UVLO condition on the bootstrap capacitor will disable only the high side output (HO).

### LAYOUT CONSIDERATIONS

The optimum performance of high and low side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

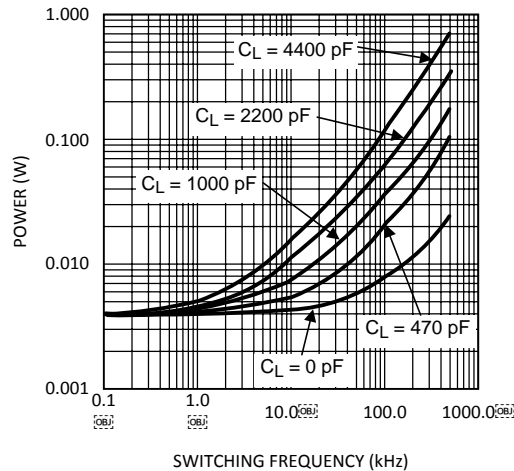
1. A low ESR/ESL capacitor must be connected close to the IC, and between  $V_{DD}$  and  $V_{SS}$  pins and between HB and HS pins to support high peak currents being drawn from  $V_{DD}$  during turn-on of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground ( $V_{SS}$ ).
3. In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding considerations:
  - a) The first priority in designing grounding connections is to confine the high peak currents from charging and discharging the MOSFET gate in a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
  - b) The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low side MOSFET body diode. The bootstrap capacitor is recharged on the cycle-by-cycle basis through the bootstrap diode from the ground referenced  $V_{DD}$  bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.
5. The resistor on the RT pin must be placed very close to the IC and separated from high current paths to avoid noise coupling to the time delay generator which could disrupt timer operation.

## POWER DISSIPATION CONSIDERATIONS

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO ( $C_L$ ), and supply voltage ( $V_{DD}$ ) and can be roughly calculated as:

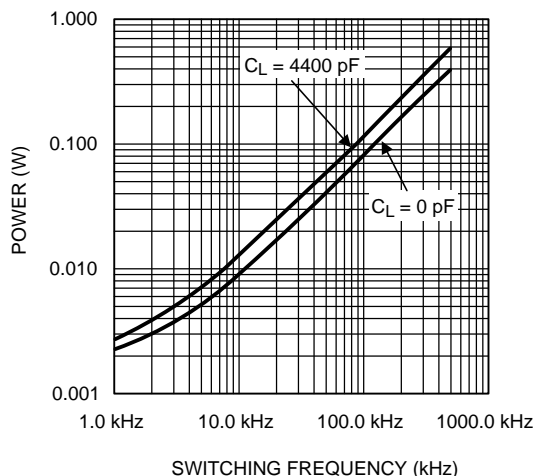
$$P_{DGATES} = 2 \cdot f \cdot C_L \cdot V_{DD}^2 \quad (1)$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. The following plot shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the above equation. This plot can be used to approximate the power losses due to the gate drivers.

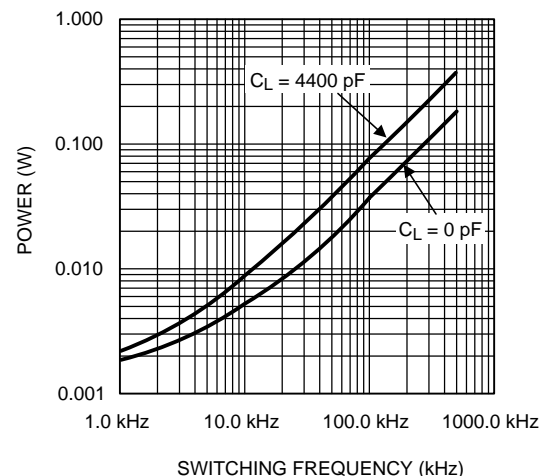


**Figure 19. Gate Driver Power Dissipation (LO + HO)**  
 **$V_{CC} = 12V$ , Neglecting Diode Losses**

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to frequency. Larger capacitive loads require more current to recharge the bootstrap capacitor resulting in more losses. Higher input voltages ( $V_{IN}$ ) to the half bridge result in higher reverse recovery losses. The following plot was generated based on calculations and lab measurements of the diode recovery time and current under several operating conditions. This can be useful for approximating the diode power dissipation.

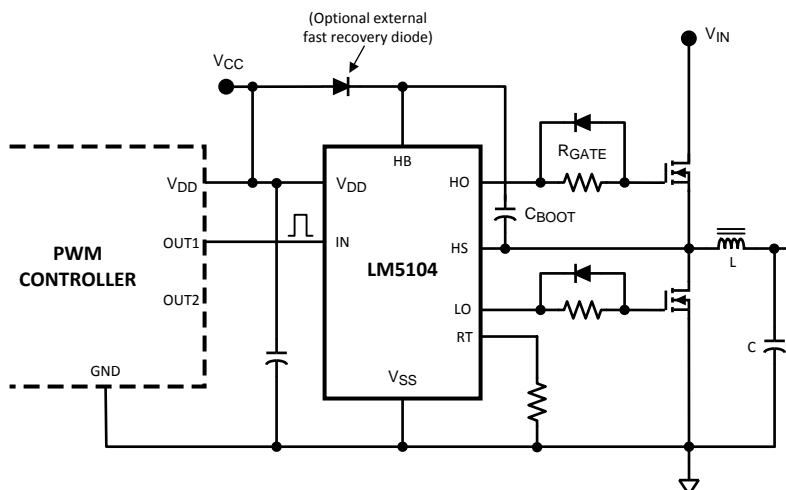


**Figure 20. Diode Power Dissipation  $V_{IN} = 80V$**



**Figure 21. Diode Power Dissipation  $V_{IN} = 40V$**

The total IC power dissipation can be estimated from the above plots by summing the gate drive losses with the bootstrap diode losses for the intended application. Because the diode losses can be significant, an external diode placed in parallel with the internal bootstrap diode (refer to [Figure 22](#)) can be helpful in removing power from the IC. For this to be effective, the external diode must be placed close to the IC to minimize series inductance and have a significantly lower forward voltage drop than the internal diode.



**Figure 22. LM5104 Driving MOSFETs Connected in Synchronous Buck Configuration**

## REVISION HISTORY

### Changes from Revision B (March 2013) to Revision C

### Page

- Changed layout of National Data Sheet to TI format ..... [12](#)

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5104M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	5104 M	
LM5104M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5104 M	<a href="#">Samples</a>
LM5104MX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125	5104 M	
LM5104MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5104 M	<a href="#">Samples</a>
LM5104SD/NOPB	ACTIVE	WSO	DPR	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5104SD	<a href="#">Samples</a>
LM5104SDX/NOPB	ACTIVE	WSO	DPR	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5104SD	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

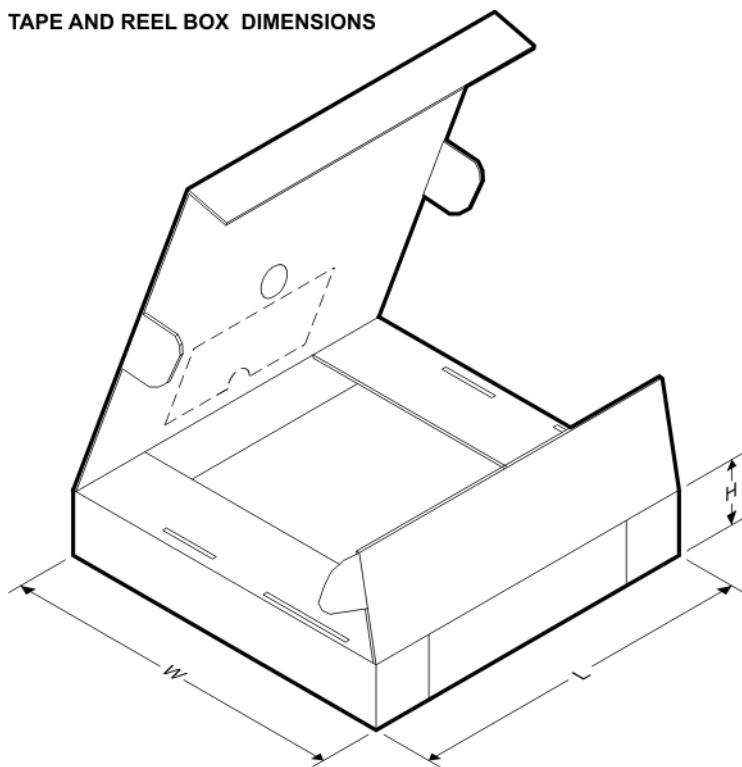
**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5104MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5104MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5104SD/NOPB	WSO	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5104SDX/NOPB	WSO	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1



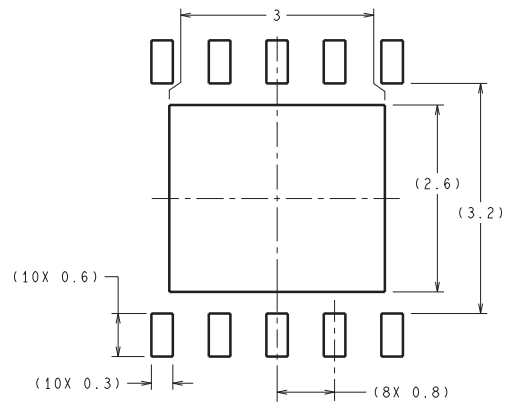
## TAPE AND REEL BOX DIMENSIONS



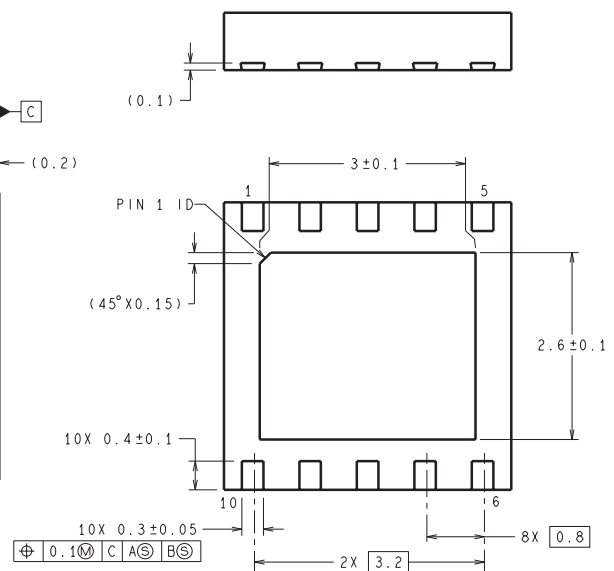
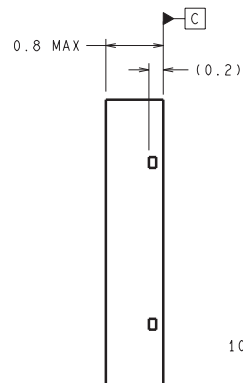
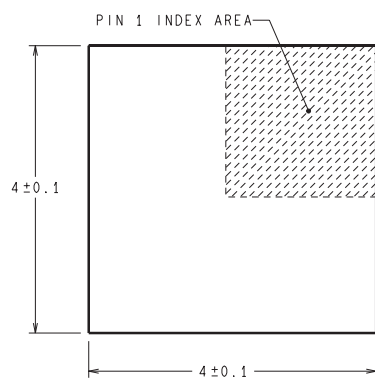
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5104MX	SOIC	D	8	2500	367.0	367.0	35.0
LM5104MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5104SD/NOPB	WSO	DPR	10	1000	210.0	185.0	35.0
LM5104SDX/NOPB	WSO	DPR	10	4500	367.0	367.0	35.0

DPR0010A



## RECOMMENDED LAND PATTERN

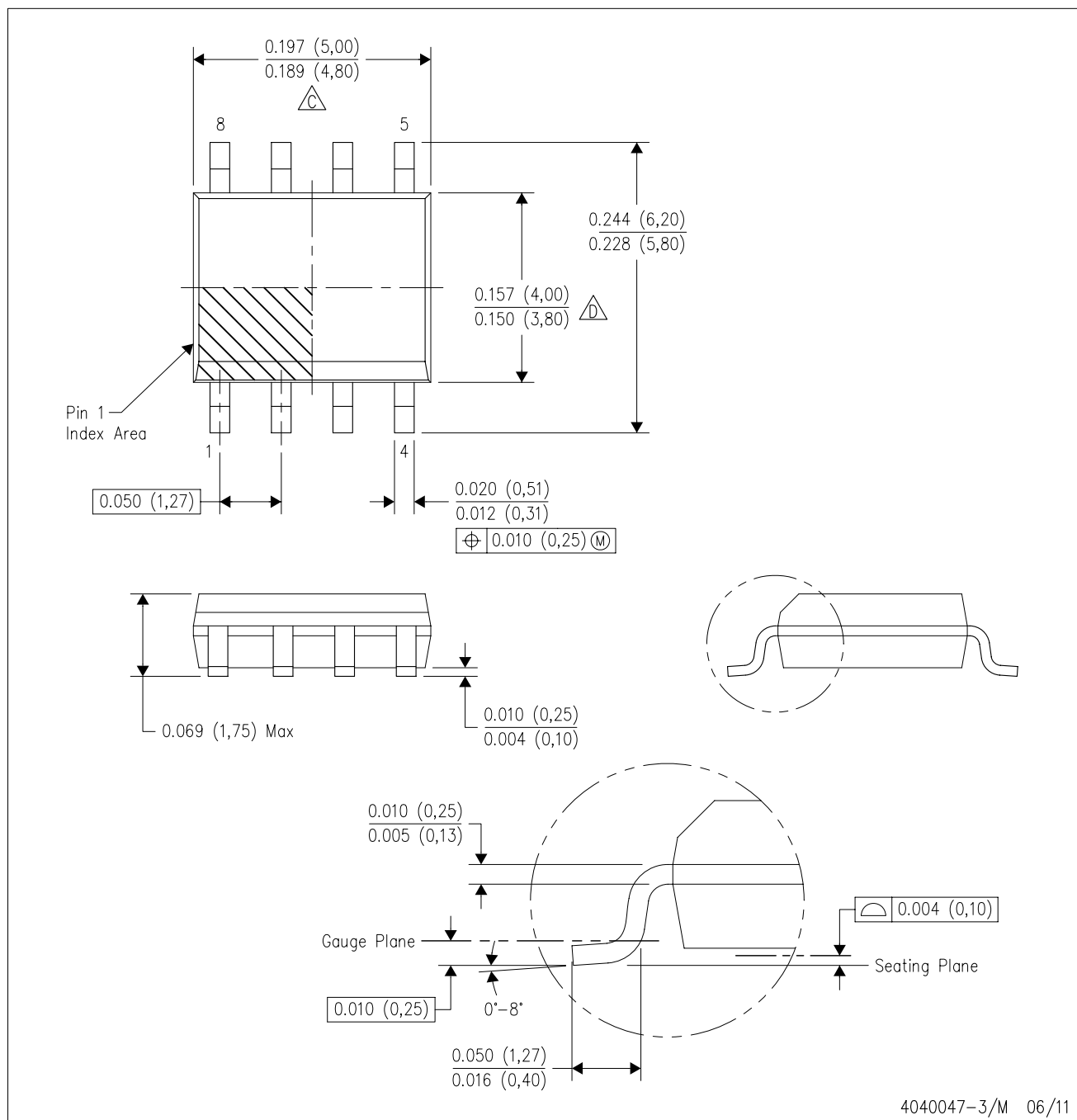


**DIMENSIONS ARE IN MILLIMETERS**

SDC10A (Rev A)

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)