

General Description

The 843751 is a low jitter, high performance clock generator. The 843751 is designed for use in the SAS-2 interconnect and the three transport protocols that use the SAS-2 interconnect: Serial SCSI Protocol (SSP), Serial ATA Tunneled Protocol (STP), and Serial Management Protocol (SMP). The 843751 has excellent (<1ps) RMS phase jitter, over the SAS defined integration range. The 843751 uses an external, 25MHz, parallel resonant crystal to generate 75MHz. This silicon based approach provides excellent frequency stability and reliability. The 843751 features up, down, and center spread spectrum (SSC) clocking techniques. The up, down and center SSC will be required in the SAS-2 applications that have three clock trees in the HBA and expander ASICs.

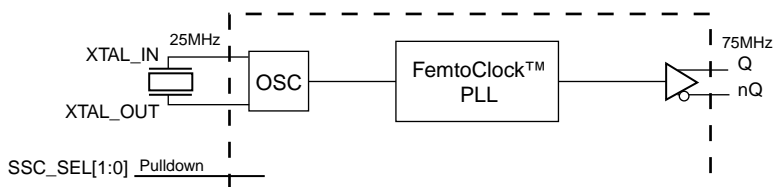
Applications

- SAS/SATA Host Bus Adapters
- SATA Port Multipliers
- SAS I/O Controllers
- TapeDrive and HDD Array Controllers
- SAS Edge and Fanout Expanders
- HDDs and TapeDrives
- Disk Storage Enterprise

Features

- Designed for use in SAS, SAS-2 systems
- Up, down and center Spread Spectrum Clocking (SSC)
- One differential 3.3V or 2.5V LVPECL output pair
- Output frequency: 75MHz
- RMS phase jitter @ 75MHz, (900kHz – 7.5MHz): 0.734ps (typical) @ 3.3V
- 3.3V or 2.5V operating supply modes
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- **Functional replacement part: 843002AYLF**

Block Diagram



Pin Assignment



843751

8-Lead SOIC, 150 Mil

3.90mm x 4.90mm x 1.375mm package body

M Package

Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
3, 4	SSC_SEL0, SSC_SEL1	Input	Pulldown	SSC select pins. See Table 3A. LVCMOS/LVTTL interface levels.
5	V _{CC}	Power		Power supply pin.
6, 7	Q, nQ	Output		Differential clock outputs. LVPECL interface levels.
8	V _{EE}	Power		Negative supply pin.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3. SSC_SEL[1:0] Function Table

Inputs		Mode
SSC_SEL1	SSC_SEL0	
0 (default)	0 (default)	SSC Off
0	1	0.5% Down-spread
1	0	0.5% Up-spread
1	1	0.5% Center-spread

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to $V_{CC} + 0.5V$
Outputs, I_O Continuous Current Surge Current	50mA 100mA
Package Thermal Impedance, θ_{JA}	96°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				77	mA

Table 4B. Power Supply DC Characteristics, $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				75	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		$V_{CC} = 3.3V$	2		$V_{CC} + 0.3$	V
			$V_{CC} = 2.5V$	1.7		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage		$V_{CC} = 3.3V$	-0.3		0.8	V
			$V_{CC} = 2.5V$	-0.3		0.7	V
I_{IH}	Input High Current	SSC_SEL[0:1]	$V_{CC} = V_{IN} = 3.465V$ or $2.5V$			150	μA
I_{IL}	Input Low Current	SSC_SEL[0:1]	$V_{CC} = 3.465V$ or $2.5V$, $V_{IN} = 0V$	-5			μA

Table 4D. LVPECL DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		0.9	V

NOTE 1: Output termination with 50Ω to $V_{CC} - 2V$.

Table 4E. LVPECL DC Characteristics, $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.5$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		0.9	V

NOTE 1: Output termination with 50Ω to $V_{CC} - 2V$.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency; NOTE 1			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

AC Electrical Characteristics

Table 6A. AC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			75		MHz
$\text{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 1	75MHz, Integration Range: 900kHz – 7.5MHz		0.734		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	325		575	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Refer to the Phase Noise plot.

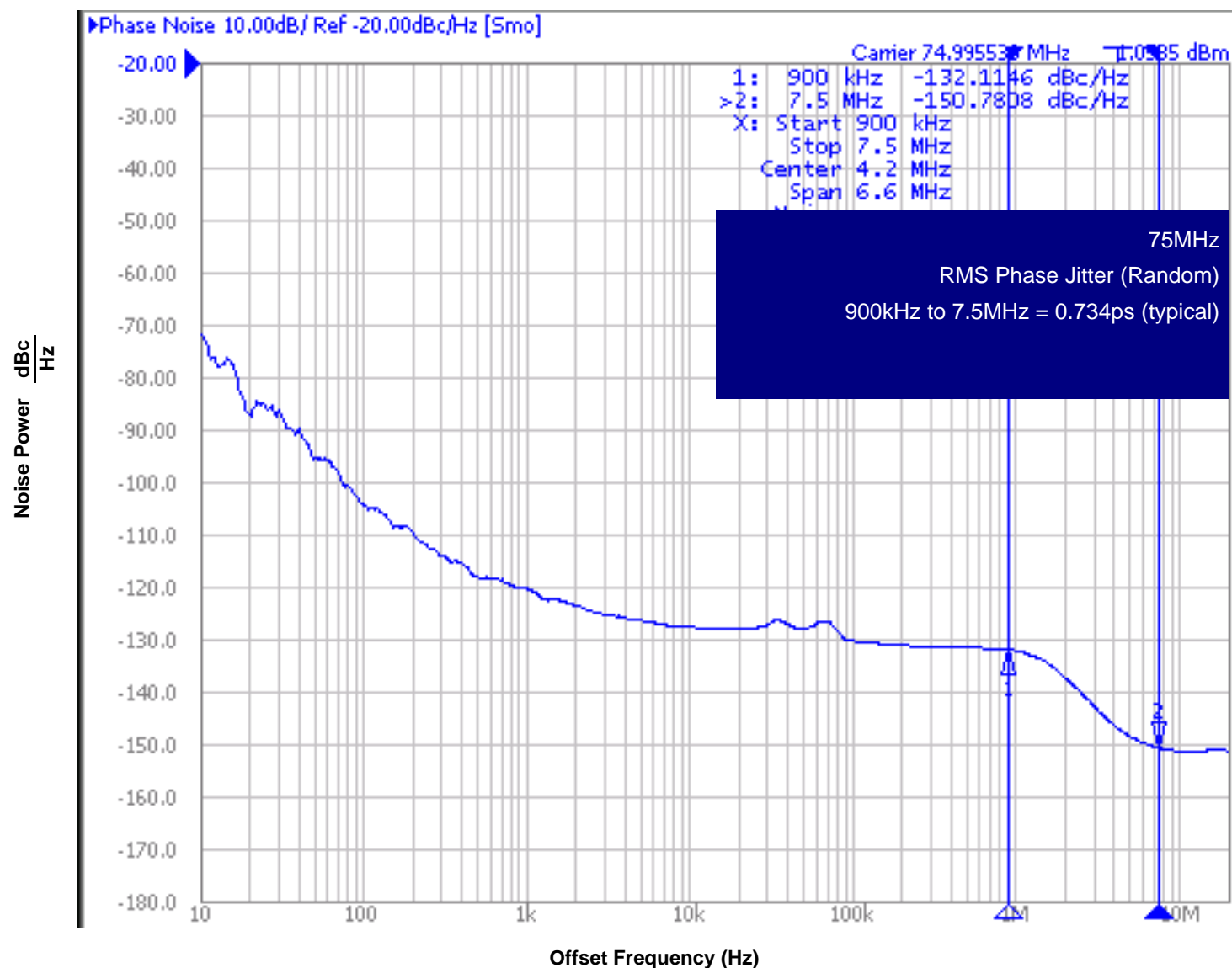
Table 6B. AC Characteristics, $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			75		MHz
$\text{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 1	75MHz, Integration Range: 900kHz – 7.5MHz		0.755		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	325		575	ps
odc	Output Duty Cycle		48		52	%

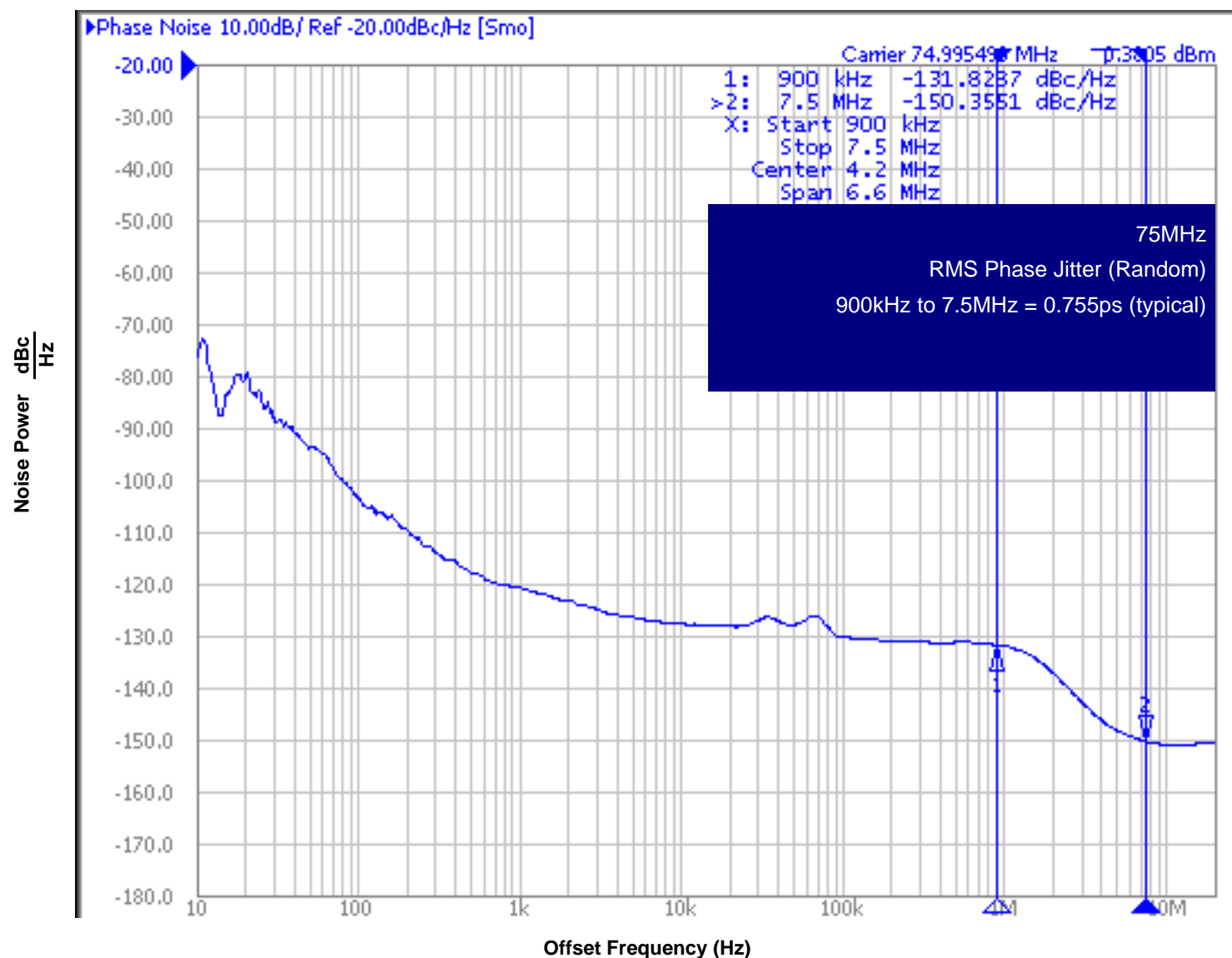
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NOTE 1: Refer to the Phase Noise plot.

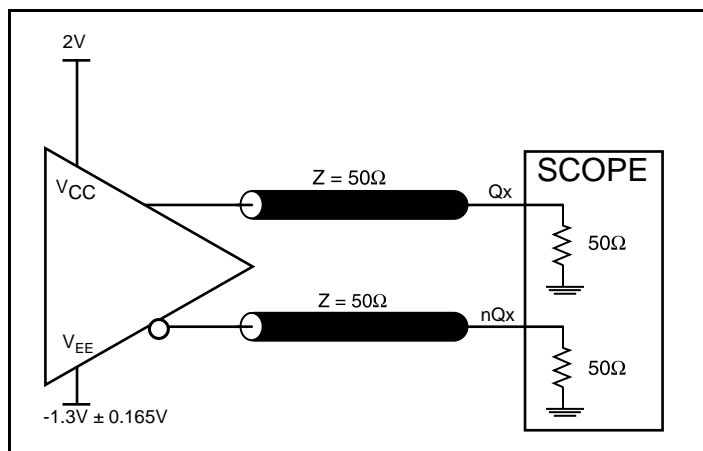
Typical Phase Noise at 75MHz at 3.3V



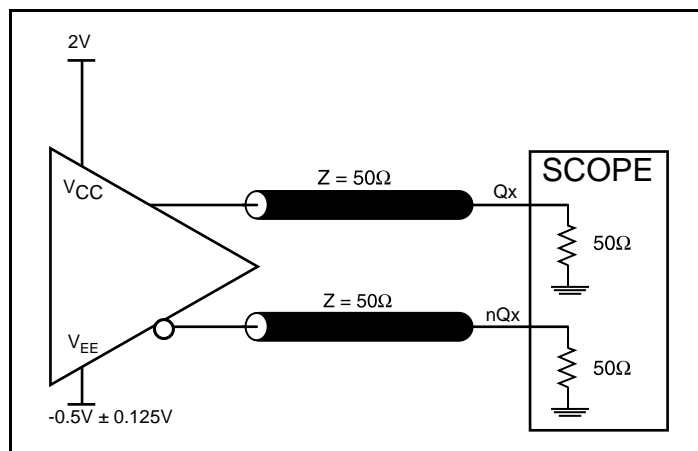
Typical Phase Noise at 75MHz at 2.5V



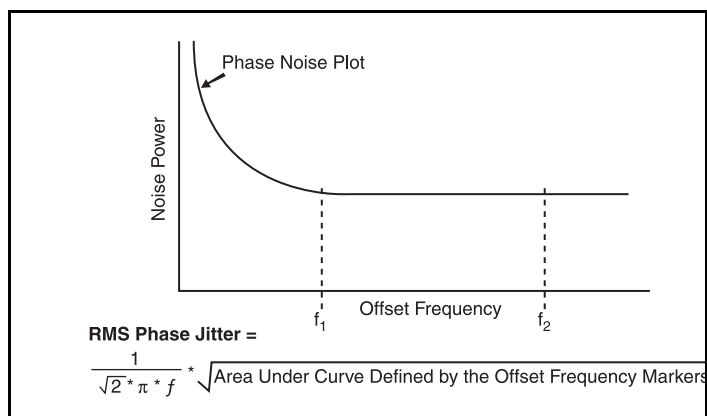
Parameter Measurement Information



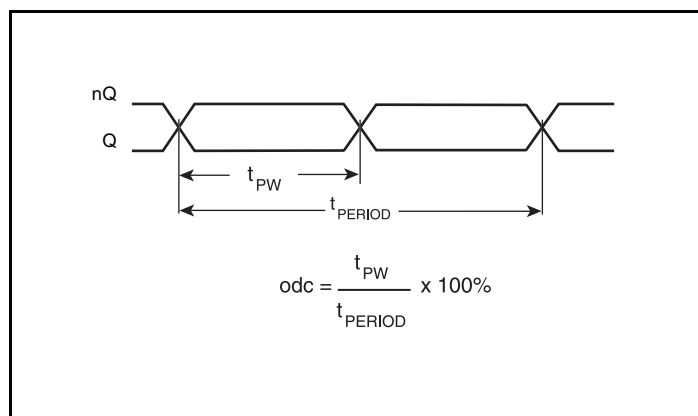
3.3V LVPECL Output Load AC Test Circuit



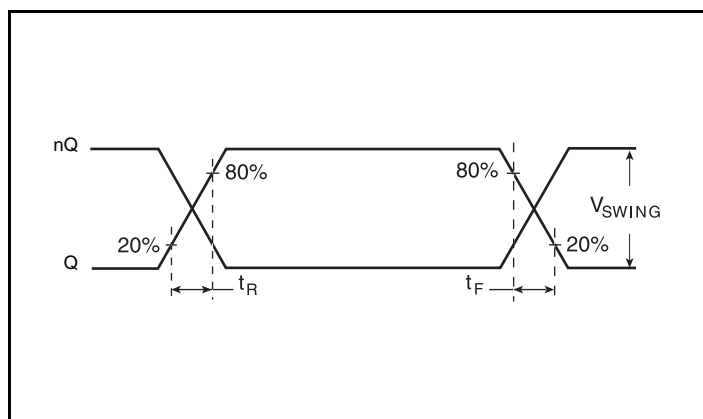
2.5V LVPECL Output Load AC Test Circuit



RMS Phase Jitter



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Crystal Input Interface

The 843751 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using a 25MHz, 18pF parallel resonant crystal and

were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

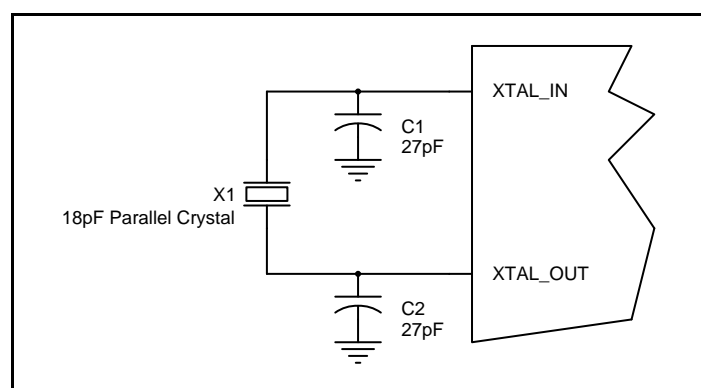


Figure 1. Crystal Input Interface

LVC MOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 2*. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (R_o) plus the series resistance (R_s) equals

the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50Ω applications, R_1 and R_2 can be 100Ω. This can also be accomplished by removing R_1 and making R_2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

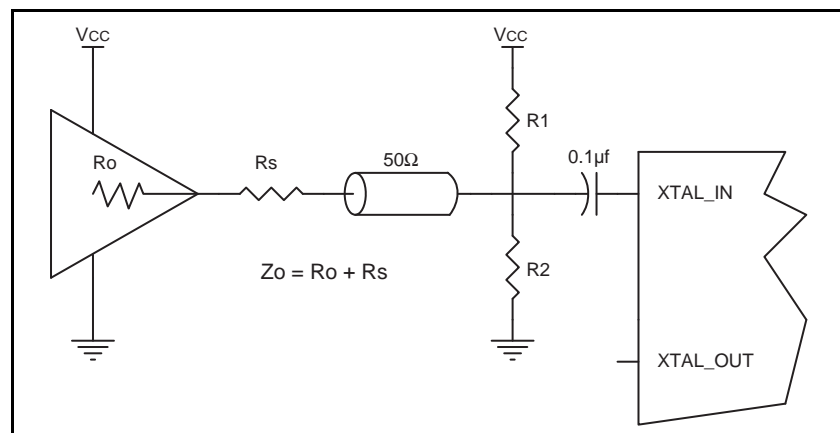


Figure 2. General Diagram for LVC MOS Driver to XTAL Input Interface

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

Figures 3A and 3B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

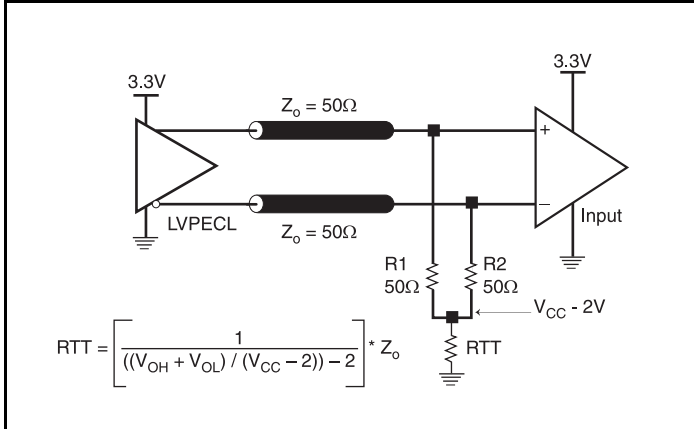


Figure 3A. 3.3V LVPECL Output Termination

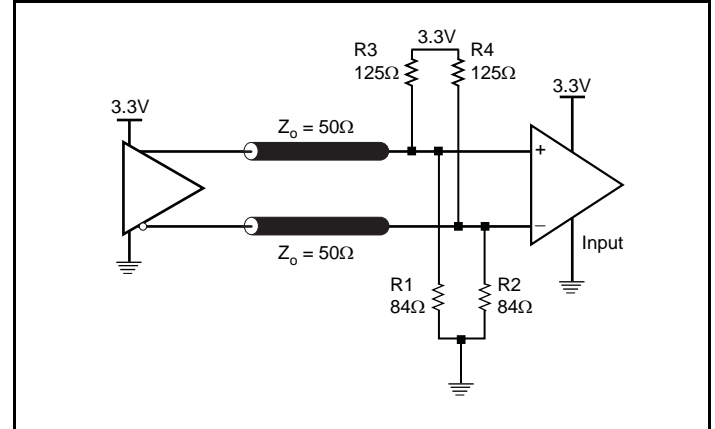


Figure 3B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 4A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC} - 2V$. For $V_{CC} = 2.5V$, the $V_{CC} - 2V$ is very close to ground

level. The $R3$ in Figure 4B can be eliminated and the termination is shown in Figure 4C.

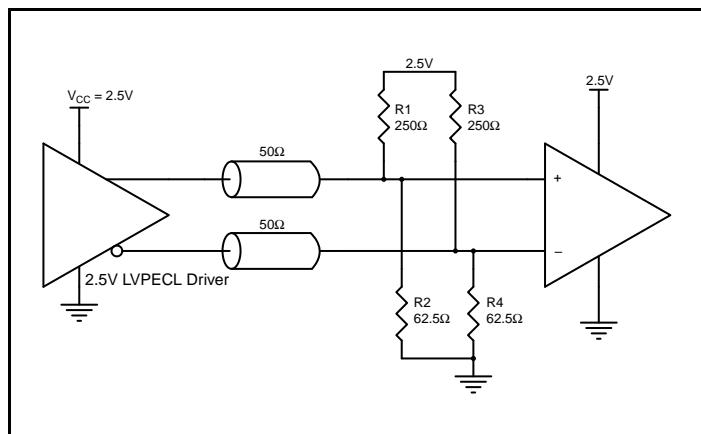


Figure 4A. 2.5V LVPECL Driver Termination Example

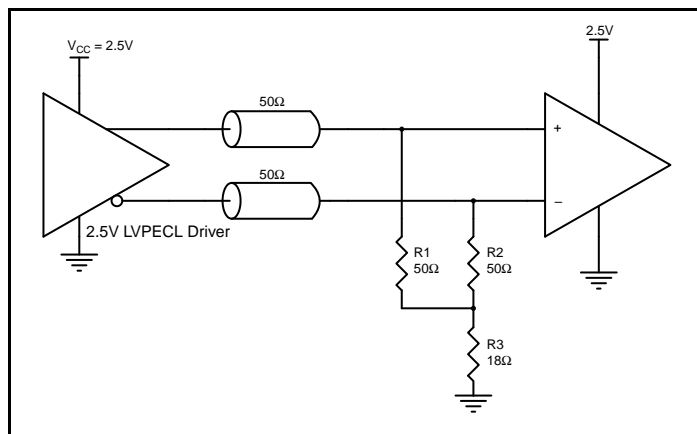


Figure 4B. 2.5V LVPECL Driver Termination Example

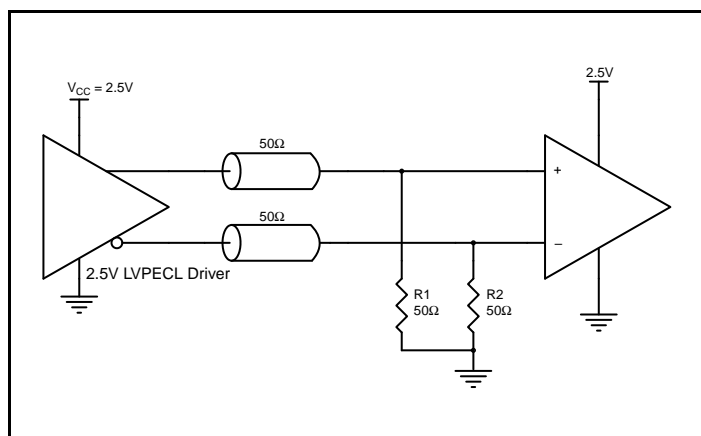


Figure 4C. 2.5V LVPECL Driver Termination Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 843751. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 843751 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 77mA = \mathbf{266.8mW}$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**

Total Power_{MAX} (3.465V, with all outputs switching) = 266.8mW + 30mW = **296.8mW**

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 96°C/W per Table 7 below.

Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:

$70^\circ C + 0.297W * 96^\circ C/W = 98.5^\circ C$. This is well below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 24 Lead TSSOP, Forced Convection

θ_{JA} vs. Air Flow			
Linear Feet per Second	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	96°C/W	87°C/W	82°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 5*.

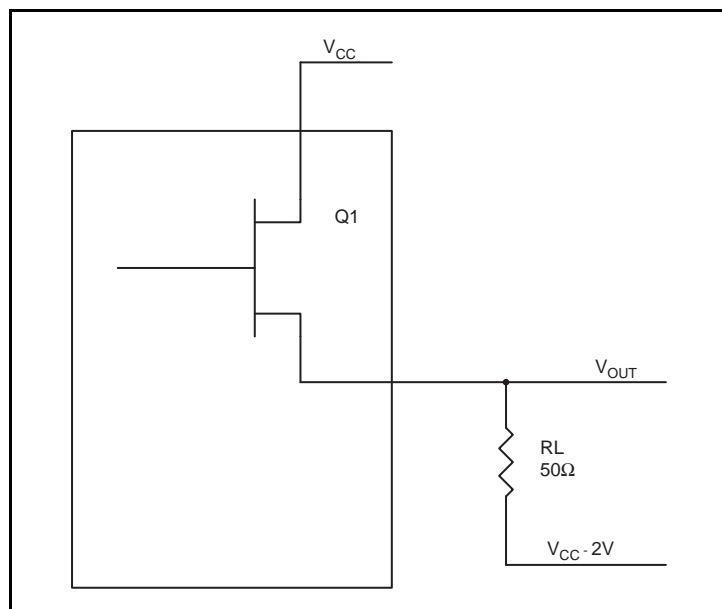


Figure 5. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} - 0.9V$
 $(V_{CC_MAX} - V_{OH_MAX}) = 0.9V$
- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CC_MAX} - 1.7V$
 $(V_{CC_MAX} - V_{OL_MAX}) = 1.7V$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = 30mW$$

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 8 Lead SOIC

θ_{JA} vs. Air Flow			
Linear Feet per Second	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	96°C/W	87°C/W	82°C/W

Transistor Count

The transistor count for 843751 is: 2986

Package Outline and Package Dimensions

Package Outline - M Suffix for 8 Lead SOIC

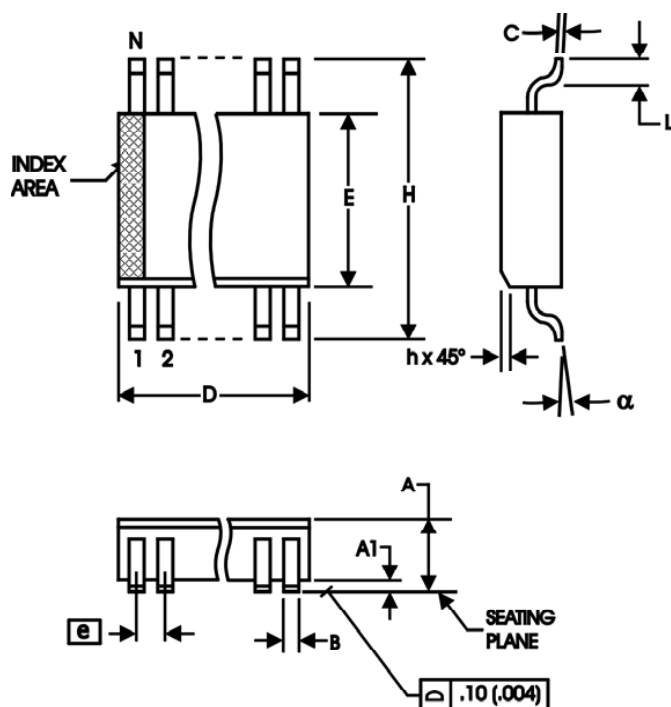


Table 9. Package Dimensions for 8 Lead SOIC

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 Basic	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843751AMLf	843751AL	Lead-Free, 8 Lead SOIC	Tube	0°C to 70°C
843751AMLFT	843751AL	Lead-Free, 8 Lead SOIC	Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B		1	PDN #CQ-15-04 Product Discontinuance Notice – Last Time buy Expires on August 14, 2016.	08/21/15

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