MN3611RE

Color CCD Linear Image Sensor with 720 Pixels each for R, G, and B Colors

■ Overview

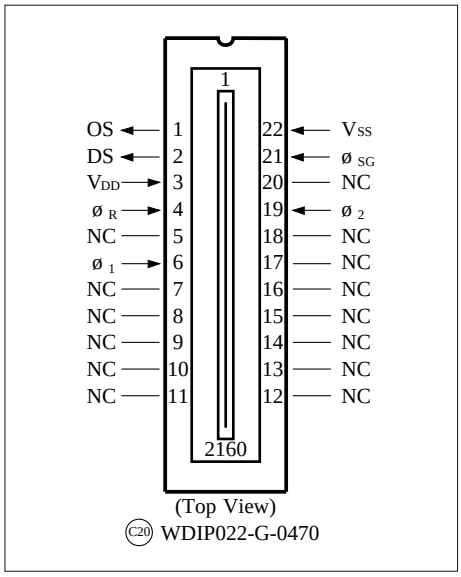
The MN3611RE is a high responsivity CCD color linear image sensor having low dark output floating photodiodes in the photodetector region, CCD analog shift registers for read out, and 720 pixels each for the primary colors R, G, and B.

It can read a B6 size color document with a high quality and a resolution of 170dpi.

■ Features

- 2160 (720 × R.G.B) floating photodiodes and an n-channel buried type CCD shift registers are built in a single chip.
- It is possible to read a B6 size color document with a high quality and a resolution of 170dpi.
- RGB primary colors type on chip color filters are used for color separation.
- Very high responsivity is obtained because voltage amplifier circuits are built in the chip.
- Use of photodiodes with a new structure has made the dark output voltage very low.
- Large signal output of typically 2V at saturation can be obtained.

■ Pin Assignments



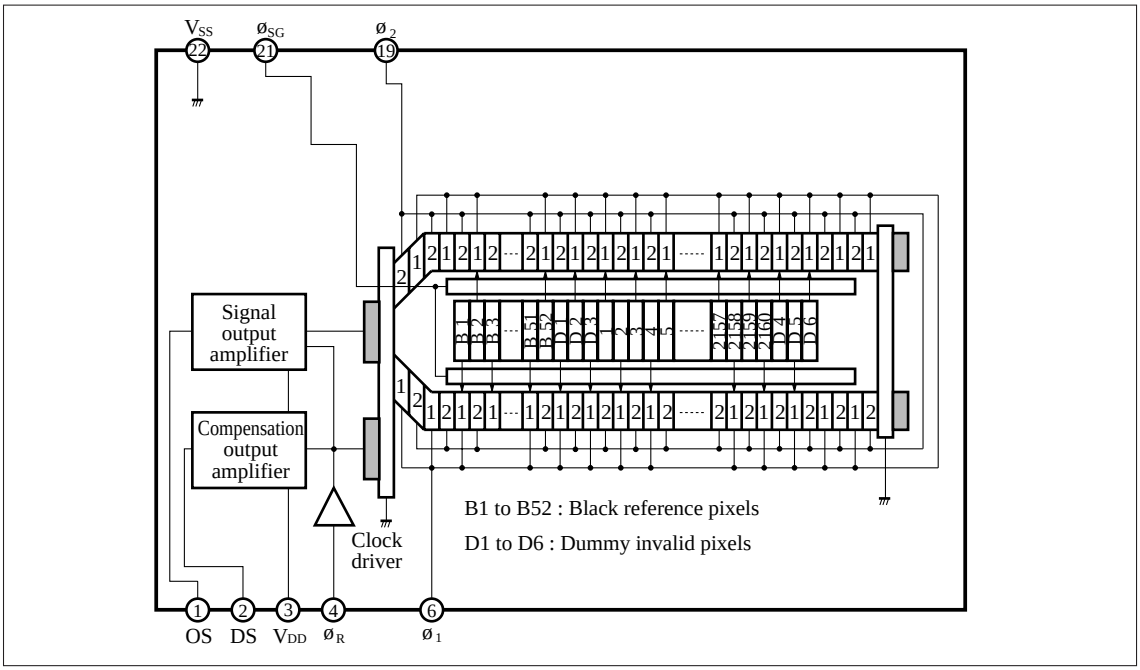
(Top View)

C20 WDIP022-G-0470

■ Application

- Reading out color images in a color scanner.

■ Block Diagram



■ Absolute Maximum Ratings (Ta=25˚C, V_{SS}=0V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	– 0.3 to +15	V
Input voltage	V_I	– 0.3 to +15	V
Output voltage	V_O	– 0.3 to +15	V
Operating temperature range	T_{opr}	–25 to + 60	˚C
Storage temperature range	T_{stg}	–40 to +100	˚C

■ Operating Conditions

• Voltage conditions (Ta=–25 to +60˚C, V_{SS}=0V)

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply voltage	V_{DD}		11.4	12.0	13.0	V
CCD shift register clock High level	$V_{øH}$		4.5	5.0	5.5	V
CCD shift register clock Low level	$V_{øL}$		0	0.2	0.5	V
Shift gate clock High level	V_{SH}		4.5	5.0	5.5	V
Shift gate clock Low level	V_{SL}		0	0.2	0.5	V
Reset gate clock High level	V_{RH}		4.5	5.0	5.5	V
Reset gate clock Low level	V_{RL}		0	0.2	0.5	V

• Timing conditions (Ta=–25 to +60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock frequency	f_C	See drive timing diagram. f_C=1/2T	—	0.5	1.0	MHz
Reset clock frequency (=data rate)	f_R	See drive timing diagram. f_R=1/T	—	1.0	2.0	MHz
Shift register clock rise time	t_{Cr}	See input/output timing diagram.	0	60	100	ns
Shift regisster clock fall time	t_{Cf}	See drive timing diagram.	0	60	100	ns
Shift clock ($ø_{SG}$) rise time	t_{Sr}	See input/output timing diagram. See drive timing diagram.	0	50	100	ns
Shift clock ($ø_{SG}$) fall time	t_{Sf}		0	50	100	ns
Shift clock set up time	t_{Ss}		0	100	—	ns
Shift clock pulse width	t_{Sw}		200	1000	—	ns
Shift clock hold time	t_{Sh}		0	100	—	ns
Reset clock rise time	t_{Rr}	See input/output timing diagram. See drive timing diagram.	0	15	30	ns
Reset clock fall time	t_{Rf}		0	15	30	ns
Reset clock pulse width	t_{Rw}		60	250	—	ns
Reset clock hold time	t_{Rh}		100	125	—	ns

■ Electrical Characteristics

• Clock input capacitance (Ta=–25 to +60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock input capacitance	$C_{ø1}$,$C_{ø2}$	f_{reg} =1MHz	—	350	400	pF
Reset clock input capacitance	$C_{øR}$	f_{reg} =1MHz	—	15	30	pF
Shift clock input capacitance	$C_{øSG}$	f_{reg} =1MHz	—	130	200	pF

• DC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply current	I_{DD}	V_{DD}=+12V	—	8	15	mA

• AC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Signal output delay time	tos		—	100	—	ns

■ Optical Characteristics

<Inspection conditions>

- Ta=25˚C, V_{DD}=12V, $V_{\phi H}$=V_{SH}=V_{RH}=5V (pulse), f_C=0.5MHz, f_R=1MHz, T_{int} (accumulation time)=10ms
- Light source: Daylight type fluorescent lamp with IR/UV cutting filter
- Optical system: A slit with an aperture dimensions of 20mm × 20mm is used at a distance of 200mm from the sensor (equivalent to F=10).
- Load resistance = 100k Ohms
- These specifications apply to the 2160 valid pixels excluding the dummy pixels D1 to D6.

Parameter		Symbol	Condition	min	typ	max	Unit
Responsivity	red	R_R		4.5	7.2	9.9	V/lx· s
	green	R_G		10.0	13.5	17.0	
	blue	R_B		6.5	9.6	12.7	
Photo response non-uniformity		PRNU	Note 1	—	—	15	%
Odd/even bit non-uniformity		O/E	Note 2	—	—	3	%
Saturation output voltage		V_{SAT}	Note 3	1.5	2.0	—	V
Saturation exposure		SE	Note 3		0.13	—	lx·s
Dark signal output voltage		V_{DRK}	Note 4	—	0.8	2.0	mV
Dark signal output non-uniformity		DSNU	Note 4	—	0.2	3.0	mV
Shift register total transfer efficiency		STTE		92	99	—	%
Output impedance		Z_O		—	—	1	kΩ
Dynamic range		DR	Note 5	—	2,500	—	
Signal output pin DC level		V_{OS}	Note 5	3.5	4.5	6.0	V
Compensation output pin DC level		V_{DS}	Note 6	3.5	4.5	6.0	V
Signal and compensation output pin DC level difference		$\|V_{OS} - V_{DS}\|$	Note 6	—	50	100	mV

Note 1) The photo response non-uniformity (PRNU) for each color is defined by the following equation, where X_{ave} is the average output voltage of the 720 valid pixels and Δx is the absolute value of the difference between X_{ave} and the voltage of the maximum (or minimum) output pixel, when the surface of the photo-sites is illuminated with light having a uniform distribution over the entire surface.

$$PRNU = \frac{\triangle x}{X_{ave}} \times 100\ (\%)$$

The incident light intensity shall be 50% of the standard saturation light intensity.

Note 2) The odd/even bit non-uniformity (O/E) for each color is defined by the following equation, where X_{ave} is the average output voltage of the 720 valid pixels for each color and Xn is the output voltage of the 'n'th pixel for each color, when the surface of the photo-sites is illuminated with light having a uniform distribution over the entire surface.

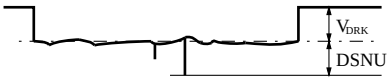
$$O/E = \frac{\sum_{n=1}^{719} |Xn - Xn_{+1}|}{719 \times X_{ave}} \times 100\ (\%)$$

The incident light intensity shall be 50% of the standard saturation light intensity.

Note 3) The Saturation output voltage (V_{SAT}) is defined as the output voltage at the point when the linearity of the photoelectric characteristics cannot be maintained as the incident light intensity is increased. [The light intensity of exposure at this point is called the saturation exposure (SE).]

Note 4) The dark signal output voltage (V_{DRK}) is defined as the average output voltage of the 2160 pixels in the dark condition at Ta=25˚C and T_{int}=10ms. Normally, the dark output voltage doubles for every 8 to 10˚C rise in Ta, and is proportional to T_{int}.

The dark signal output non-uniformity (DSNU) is defined as the difference between the maximum output voltage among all the valid pixels and V_{DRK} in the dark condition at Ta=25˚C and T_{int}=10ms.



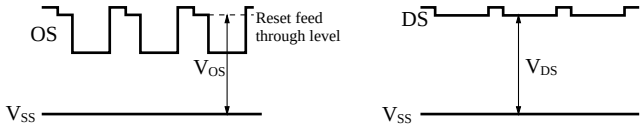
■ Optical Characteristics (continued)

Note 5) The dynamic range (DR) is defined by the following equation.

$$DR = \frac{V_{SAT}}{V_{DRK}}$$

Since the dark signal voltage is proportional to the accumulation time, the dynamic range becomes wider when the accumulation time is shorter.

Note 6) The signal output pin DC level (V_{OS}) and the compensation output pin DC level (V_{DS}) are the voltage values shown in the following figure.



■ Pin Descriptions

Pin No.	Symbol	Pin name	Condition
1	OS	Signal output	
2	DS	Compensation output	
3	V_{DD}	Power supply	
4	$ø_R$	Reset clock	
5	NC	Non connection	
6	$ø_1$	CCD Shift clock gate	
7	NC	Non connection	
8	NC	Non connection	
9	NC	Non connection	
10	NC	Non connection	
11	NC	Non connection	
12	NC	Non connection	
13	NC	Non connection	
14	NC	Non connection	
15	NC	Non connection	
16	NC	Non connection	
17	NC	Non connection	
18	NC	Non connection	
19	$ø_2$	CCD Shift clock gate	
20	NC	Non connection	
21	$ø_{SG}$	Shift clock gate	
22	V_{SS}	Ground	

Note) Connect all NC pins externally to V_{SS}.

■ Construction of the Image Sensor

The MN3611RE can be made up of the three sections of—a) photo detector region, b) CCD transfer region (shift register), and c) output region.

a) Photo detector region

- The photoelectric conversion device consists of an 11µm floating photodiode and a 3µm channel stopper for each pixel, and 2160 of these devices are linearly arranged side by side at a pitch of 14µm.
- The photo detector's windows are 14µm × 14µm squares and light incident on areas other than these windows is optically shut out.
- The photo detector is provided with 52 optically shielded pixels (black dummy pixels) which serve as the black reference.

b) CCD Transfer region (shift register)

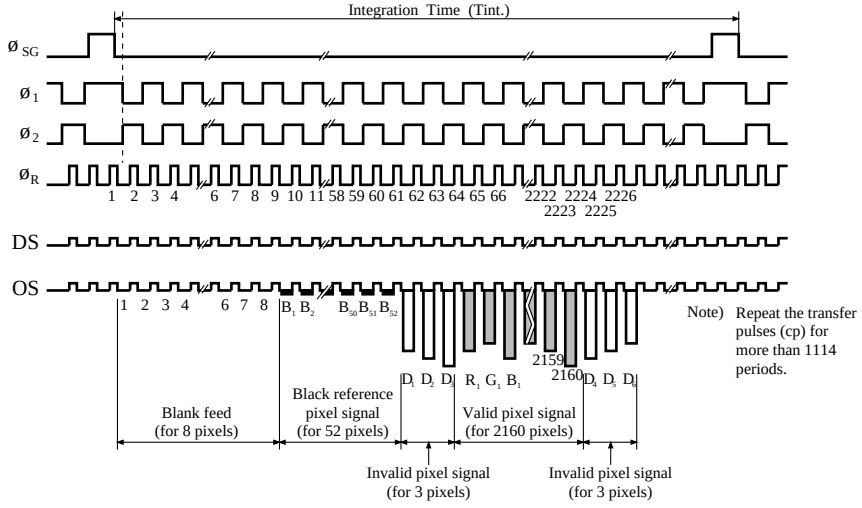
- The light output that has been photoelectrically converted is transferred to the CCD transfer for each odd and even pixel at the timing of the shift clock ($ø_{SG}$). The optical signal electric charge transferred to this analog shift register is successively transferred out and guided to the output region.
- A buried type CCD that can be driven by a two phase clock ($ø_1$, $ø_2$) is used for the analog shift register.

c) Output region

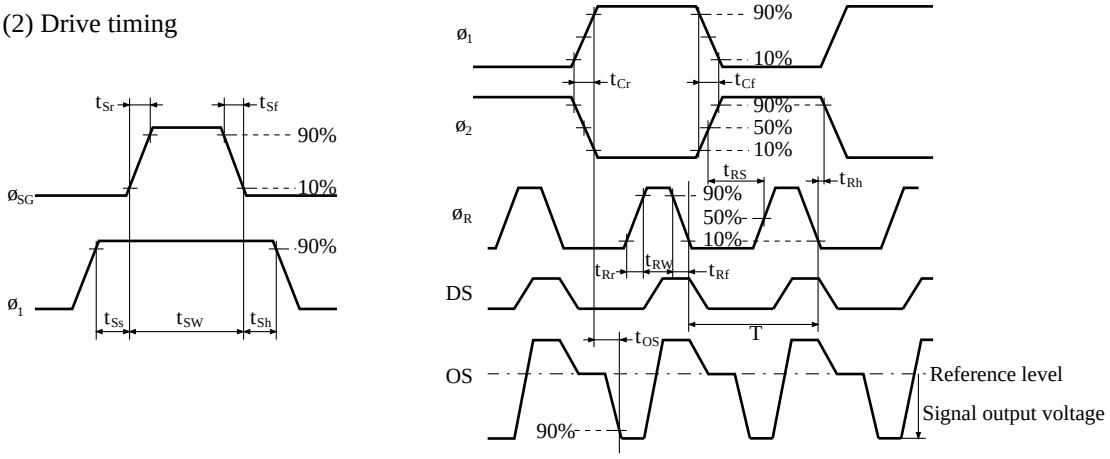
- The signal charge that is transferred to the output region is sent to the detector where impedance transformation is done using two source follower stages.
- The DC level component and the clock noise component not containing optical signals are output from the DS pin.
- By carrying out differential amplification of the two outputs OS and DS externally, it is possible to obtain an output signal with a high S/N ratio by reducing the clock noise, etc.

■ Timing Diagram

(1) I/O timing



(2) Drive timing



■ Graphs and Characteristics

Spectral Response Characteristics