

## 20-Channel, Serial-Input, Vacuum-Fluorescent Display Driver for Anode/Grid

### Features

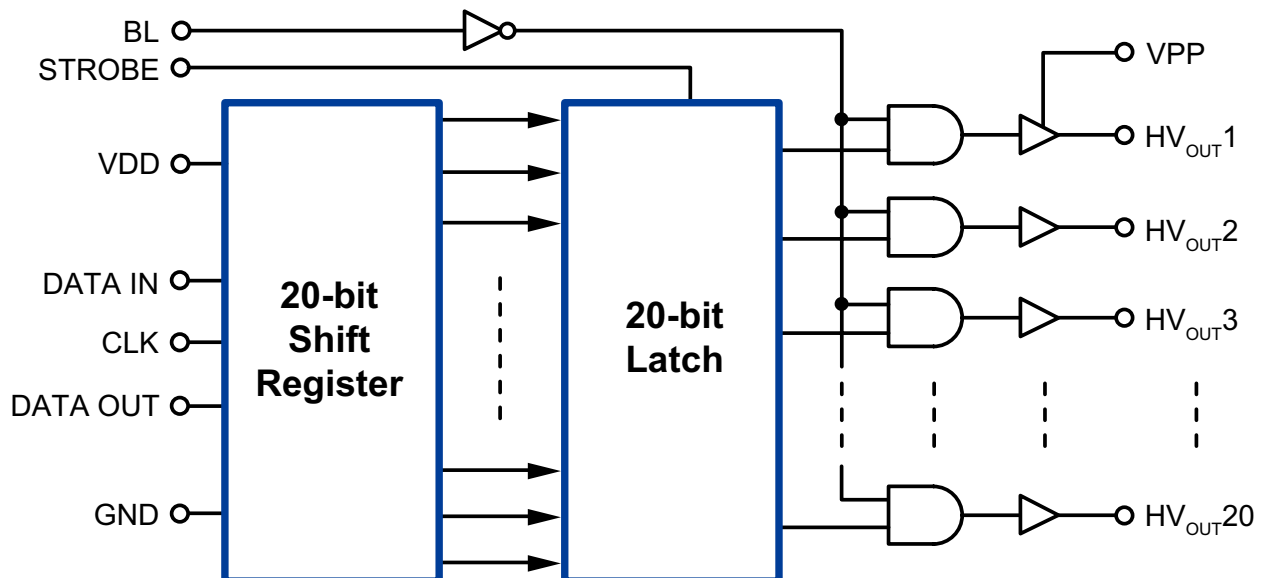
- ▶ HVCMOS® technology for high performance
- ▶ Operating voltage up to 80V
- ▶ High speed source driver
- ▶ 5.0V CMOS logic circuitry
- ▶ Up to 5.0MHz data input rate
- ▶ Excellent noise immunity
- ▶ Flexible high voltage supplies

### General Description

The Supertex HV5812 is a 20-channel, serial input, vacuum-fluorescent display driver. It combines a 20-bit CMOS shift register, data latches, and control circuitry with high voltage MOSFET outputs. The HV5812 is primarily designed for vacuum-fluorescent displays.

The CMOS shift register and latches allow direct interfacing with microprocessor based systems. Data input rates are typically over 5.0MHz with 5.0V logic supply. Especially useful for interdigit blanking, the BLANKING input disables the output source drives and turns on the sink drivers. Use with TTL may require external pull-up resistors to ensure an input logic high.

### Functional Block Diagram



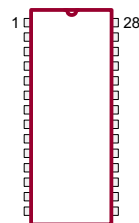
## Ordering Information

| Device | 28-Lead PDIP (.600in row spacing)<br>1.565x.580in body<br>.250in height (max)<br>.100in pitch | 28-Lead PLCC<br>.453x.453in body<br>.180in height (max)<br>.050in pitch | 28-Lead SOW<br>17.90x7.50mm body<br>2.65mm height (max)<br>1.27mm pitch |
|--------|-----------------------------------------------------------------------------------------------|-------------------------------------------------------------------------|-------------------------------------------------------------------------|
| HV5812 | HV5812P-G                                                                                     | HV5812PJ-G                                                              | HV5812WG-G                                                              |

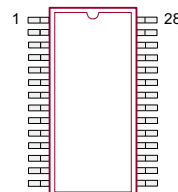
-G indicates package is RoHS compliant ("Green")



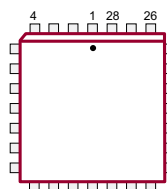
## Pin Configurations



28-Lead PDIP (P)



28-Lead SOW (WG)



28-Lead PLCC (PJ)

## Absolute Maximum Ratings

| Parameter                    | Value                   |
|------------------------------|-------------------------|
| Supply voltage, $V_{DD}$     | -0.5V to +7.5V          |
| Supply voltage, $V_{PP}$     | -0.5V to +90V           |
| Logic input levels           | -0.3V to $V_{DD}$ +0.3V |
| Maximum junction temperature | 125°C                   |
| Storage temperature range    | -55°C to +150°C         |
| Power dissipation:           |                         |
| 28-Lead PDIP (P)             | 2000mW                  |
| 28-Lead PLCC (PJ)            | 1900mW                  |
| 28-Lead SOW (WG)             | 1700mW                  |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to GND.

## Recommended Operating Conditions

| Sym      | Parameter                      | Min | Max  | Units |
|----------|--------------------------------|-----|------|-------|
| $V_{DD}$ | Supply voltage                 | 4.5 | 5.5  | V     |
| $V_{PP}$ | Supply voltage                 | 20  | 80   | V     |
| $T_j$    | Operating junction temperature | -40 | +125 | °C    |

**Power-up sequence should be the following:**

1. Connect ground.
2. Apply  $V_{DD}$ .
3. Set all inputs (Data, CLK, etc.) to a known state.
4. Apply  $V_{PP}$ .

The  $V_{PP}$  should not drop below  $V_{DD}$  during operation.

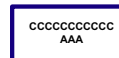
**Power-down sequence should be the reverse of the above.**

## Product Marking

Top Marking



Bottom Marking



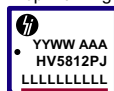
YY = Year Sealed  
WW = Week Sealed  
L = Lot Number  
C = Country of Origin\*  
A = Assembler ID\*  
— = "Green" Packaging

\*May be part of top marking

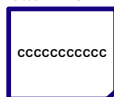
Package may or may not include the following marks: Si or

28-Lead PDIP (P)

Top Marking



Bottom Marking



YY = Year Sealed  
WW = Week Sealed  
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A = Assembler ID  
C = Country of Origin\*  
— = "Green" Packaging

\*May be part of top marking

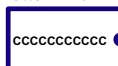
Package may or may not include the following marks: Si or

28-Lead PLCC (PJ)

Top Marking



Bottom Marking



YY = Year Sealed  
WW = Week Sealed  
A = Assembler ID  
L = Lot Number  
C = Country of Origin\*  
— = "Green" Packaging

\*May be part of top marking

Package may or may not include the following marks: Si or

28-Lead SOW (WG)

## Electrical Characteristics

### DC Characteristics (over recommended operating conditions, $T_A = 25^\circ\text{C}$ , unless otherwise noted)

| Sym        | Parameter                         |            | Min  | Typ   | Max  | Units         | Conditions                                                                     |
|------------|-----------------------------------|------------|------|-------|------|---------------|--------------------------------------------------------------------------------|
| $I_{DSS}$  | Output leakage current            |            | -    | -5.0  | -15  | $\mu\text{A}$ | $V_{OUT} = 0\text{V}$ , $T_A = +70^\circ\text{C}$                              |
| $V_{OH}$   | High-level output                 | $HV_{OUT}$ | 78   | 78.5  | -    | V             | $I_{OUT} = -25\text{mA}$ , $V_{PP} = 80\text{V}$ , $T_j = +25^\circ\text{C}$   |
|            |                                   |            | 77   | 78    | -    |               | $I_{OUT} = -25\text{mA}$ , $V_{PP} = 80\text{V}$ , $T_j = +125^\circ\text{C}$  |
|            |                                   | DATA OUT   | 4.5  | 4.7   | -    | V             | $I_{OUT} = -200\mu\text{A}$ , $V_{DD} = 5.0\text{V}$                           |
| $V_{OL}$   | Low-level output                  | $HV_{OUT}$ | -    | 1.5   | 3.0  | V             | $I_{OUT} = 1.0\text{mA}$ , $T_j = +25^\circ\text{C}$ , $V_{DD} = 5.0\text{V}$  |
|            |                                   |            | -    | 2.3   | 4.0  |               | $I_{OUT} = 1.0\text{mA}$ , $T_j = +125^\circ\text{C}$ , $V_{DD} = 5.0\text{V}$ |
|            |                                   | DATA OUT   | -    | 200   | 250  | V             | $I_{OUT} = +200\mu\text{A}$ , $V_{DD} = 5.0\text{V}$                           |
| $I_{SINK}$ | Output pull-down current          |            | 2.0  | 3.5   | -    | mA            | $V_{OUT} = 5.0\text{V}$ to $V_{PP}$ , $V_{DD} = 5.0\text{V}$                   |
| $V_{IH}$   | High level logic input voltage    |            | 3.5  | -     | 5.3  | V             | $V_{DD} = 5.0\text{V}$                                                         |
| $V_{IL}$   | Low level logic input voltage     |            | -0.3 | -     | 0.8  | V             | ---                                                                            |
| $I_{IH}$   | High level logic input current    |            | -    | 0.05  | 0.5  | $\mu\text{A}$ | $V_{IN} = V_{DD}$ , $V_{DD} = 5.0\text{V}$                                     |
| $I_{IL}$   | Low level logic input current     |            | -    | -0.05 | -0.5 | $\mu\text{A}$ | $V_{IN} = 0.8\text{V}$ , $V_{DD} = 5.0\text{V}$                                |
| $I_{DDQ}$  | Quiescent $V_{DD}$ supply current |            | -    | 100   | 300  | $\mu\text{A}$ | All outputs high, $V_{DD} = 5.0\text{V}$                                       |
|            |                                   |            | -    | 100   | 300  |               | All outputs low, $V_{DD} = 5.0\text{V}$                                        |
| $I_{PPQ}$  | Quiescent $V_{PP}$ supply current |            | -    | 10    | 100  | $\mu\text{A}$ | All outputs high, no load                                                      |
|            |                                   |            | -    | 10    | 100  |               | All outputs low, no load                                                       |

### AC Characteristics (over recommended operating conditions, $T_A = 25^\circ\text{C}$ , unless otherwise noted)

|             |                                                              |     |      |   |     |                                                          |
|-------------|--------------------------------------------------------------|-----|------|---|-----|----------------------------------------------------------|
| $t_{PHL}$   | Blanking to output delay                                     | -   | 2000 | - | ns  | $C_L = 30\text{pF}$ , 50% to 50%, $V_{DD} = 5.0\text{V}$ |
| $t_{PLH}$   |                                                              | -   | 1000 | - |     |                                                          |
| $t_f$       | Output fall time                                             | -   | 1450 | - | ns  | $C_L = 30\text{pF}$ , 90% to 10%, $V_{DD} = 5.0\text{V}$ |
| $t_r$       | Output rise time                                             | -   | 650  | - | ns  | $C_L = 30\text{pF}$ , 10% to 90%, $V_{DD} = 5.0\text{V}$ |
| $t_{SU}$    | Data set-up time                                             | 75  | -    | - | ns  | See timing diagram                                       |
| $t_h$       | Data hold time                                               | 75  | -    | - | ns  | See timing diagram                                       |
| $t_{pwd}$   | Minimum data pulse width                                     | 150 | -    | - | ns  | See timing diagram                                       |
| $t_{pwclk}$ | Minimum clock pulse width                                    | 150 | -    | - | ns  | See timing diagram                                       |
| $t_{cks}$   | Minimum time between clock activation and strobe             | 300 | -    | - | ns  | See timing diagram                                       |
| $t_{pws}$   | Minimum strobe pulse width                                   | 100 | -    | - | ns  | See timing diagram                                       |
| $t_{sto}$   | Typical time between strobe activation and output transition | -   | 500  | - | ns  | See timing diagram                                       |
| $f_{CLK}$   | Maximum clock frequency                                      | -   | 8.0  | - | MHz | $T_j = +25^\circ\text{C}$ , $V_{DD} = 5.0\text{V}$       |
|             |                                                              | -   | 5.0  | - |     | $T_j = +125^\circ\text{C}$ , $V_{DD} = 5.0\text{V}$      |

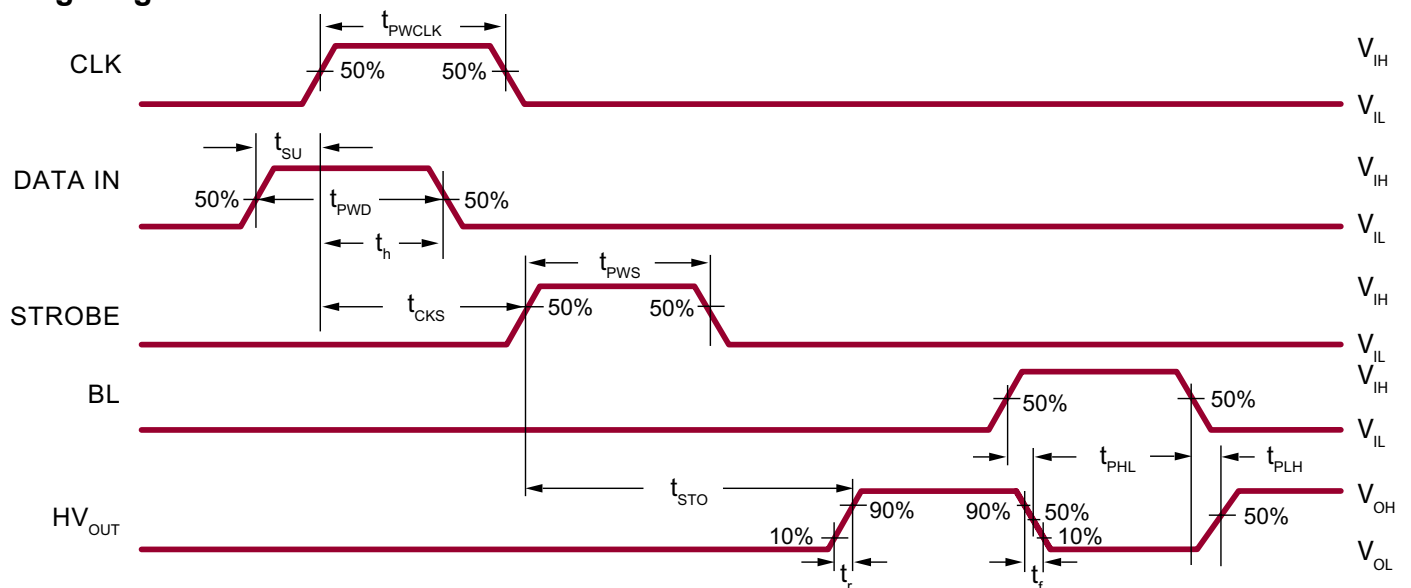
Function Table

| Serial Data Input | Clock Input | Shift Register Contents |                |                    |                  |                  | Serial Data Output | Strobe Input | Latch Content  |                |                    |                  |                | Blanking | Output Content |                |                    |                  |                |
|-------------------|-------------|-------------------------|----------------|--------------------|------------------|------------------|--------------------|--------------|----------------|----------------|--------------------|------------------|----------------|----------|----------------|----------------|--------------------|------------------|----------------|
|                   |             | I <sub>1</sub>          | I <sub>2</sub> | I <sub>3</sub> ... | I <sub>N-1</sub> | I <sub>N</sub>   |                    |              | I <sub>1</sub> | I <sub>2</sub> | I <sub>3</sub> ... | I <sub>N-1</sub> | I <sub>N</sub> |          | I <sub>1</sub> | I <sub>2</sub> | I <sub>3</sub> ... | I <sub>N-1</sub> | I <sub>N</sub> |
| H                 | L to H      | H                       | R <sub>1</sub> | R <sub>2</sub> ... | R <sub>N-2</sub> | R <sub>N-1</sub> | R <sub>N-1</sub>   | -            | -              | -              | -                  | -                | -              | -        | -              | -              | -                  | -                | -              |
| L                 | L to H      | L                       | R <sub>1</sub> | R <sub>2</sub> ... | R <sub>N-2</sub> | R <sub>N-1</sub> | R <sub>N-1</sub>   | -            | -              | -              | -                  | -                | -              | -        | -              | -              | -                  | -                | -              |
| X                 | H to L      | R <sub>1</sub>          | R <sub>2</sub> | R <sub>3</sub> ... | R <sub>N-1</sub> | R <sub>N</sub>   | R <sub>N</sub>     | -            | -              | -              | -                  | -                | -              | -        | -              | -              | -                  | -                | -              |
| -                 | -           | X                       | X              | X ...              | X                | X                | X                  | L            | R <sub>1</sub> | R <sub>2</sub> | R <sub>3</sub> ... | R <sub>N-1</sub> | R <sub>N</sub> | -        | -              | -              | -                  | -                | -              |
| -                 | -           | P <sub>1</sub>          | P <sub>2</sub> | P <sub>3</sub> ... | P <sub>N-1</sub> | P <sub>N</sub>   | P <sub>N</sub>     | H            | P <sub>1</sub> | P <sub>2</sub> | P <sub>3</sub> ... | P <sub>N-1</sub> | P <sub>N</sub> | L        | P <sub>1</sub> | P <sub>2</sub> | P <sub>3</sub> ... | P <sub>N-1</sub> | P <sub>N</sub> |
| -                 | -           | -                       | -              | -                  | -                | -                | -                  | -            | X              | X              | X ...              | X                | X              | H        | L              | L              | L ...              | L                | L              |

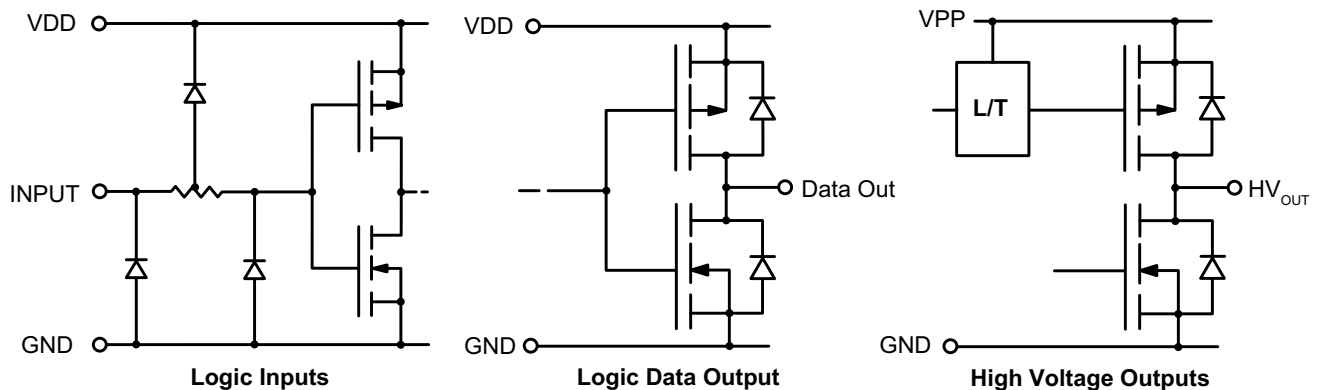
**Note:**

L = Low logic level  
 H = High logic level  
 X = Irrelevant  
 P = Present state  
 R = Previous state

Timing Diagram



Input and Output Equivalent Circuits



**28-Lead PDIP Pin Assignment (P)**

| Pin # | Function             |
|-------|----------------------|
| 1     | VPP                  |
| 2     | Data Out             |
| 3     | HV <sub>OUT</sub> 20 |
| 4     | HV <sub>OUT</sub> 19 |
| 5     | HV <sub>OUT</sub> 18 |
| 6     | HV <sub>OUT</sub> 17 |
| 7     | HV <sub>OUT</sub> 16 |
| 8     | HV <sub>OUT</sub> 15 |
| 9     | HV <sub>OUT</sub> 14 |
| 10    | HV <sub>OUT</sub> 13 |

| Pin # | Function             |
|-------|----------------------|
| 11    | HV <sub>OUT</sub> 12 |
| 12    | HV <sub>OUT</sub> 11 |
| 13    | BLANKING             |
| 14    | GND                  |
| 15    | CLOCK                |
| 16    | STROBE               |
| 17    | HV <sub>OUT</sub> 10 |
| 18    | HV <sub>OUT</sub> 9  |
| 19    | HV <sub>OUT</sub> 8  |
| 20    | HV <sub>OUT</sub> 7  |

| Pin # | Function            |
|-------|---------------------|
| 21    | HV <sub>OUT</sub> 6 |
| 22    | HV <sub>OUT</sub> 5 |
| 23    | HV <sub>OUT</sub> 4 |
| 24    | HV <sub>OUT</sub> 3 |
| 25    | HV <sub>OUT</sub> 2 |
| 26    | HV <sub>OUT</sub> 1 |
| 27    | Data In             |
| 28    | VDD                 |

**28-Lead PLCC Pin Assignment (PJ)**

| Pin # | Function             |
|-------|----------------------|
| 1     | VPP                  |
| 2     | Data Out             |
| 3     | HV <sub>OUT</sub> 20 |
| 4     | HV <sub>OUT</sub> 19 |
| 5     | HV <sub>OUT</sub> 18 |
| 6     | HV <sub>OUT</sub> 17 |
| 7     | HV <sub>OUT</sub> 16 |
| 8     | HV <sub>OUT</sub> 15 |
| 9     | HV <sub>OUT</sub> 14 |
| 10    | HV <sub>OUT</sub> 13 |

| Pin # | Function             |
|-------|----------------------|
| 11    | HV <sub>OUT</sub> 12 |
| 12    | HV <sub>OUT</sub> 11 |
| 13    | BLANKING             |
| 14    | GND                  |
| 15    | CLOCK                |
| 16    | STROBE               |
| 17    | HV <sub>OUT</sub> 10 |
| 18    | HV <sub>OUT</sub> 9  |
| 19    | HV <sub>OUT</sub> 8  |
| 20    | HV <sub>OUT</sub> 7  |

| Pin # | Function            |
|-------|---------------------|
| 21    | HV <sub>OUT</sub> 6 |
| 22    | HV <sub>OUT</sub> 5 |
| 23    | HV <sub>OUT</sub> 4 |
| 24    | HV <sub>OUT</sub> 3 |
| 25    | HV <sub>OUT</sub> 2 |
| 26    | HV <sub>OUT</sub> 1 |
| 27    | Data In             |
| 28    | VDD                 |

**28-Lead SOW Pin Assignment (WG)**

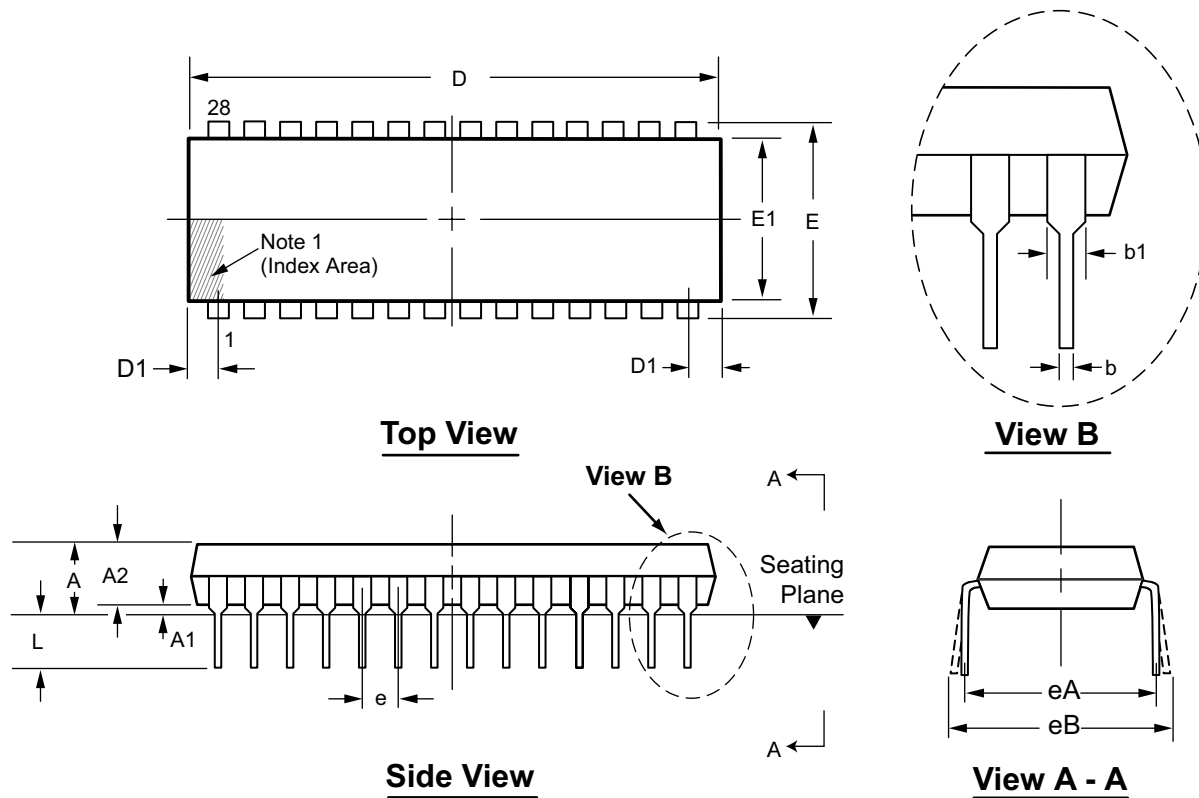
| Pin # | Function             |
|-------|----------------------|
| 1     | VPP                  |
| 2     | Data Out             |
| 3     | HV <sub>OUT</sub> 20 |
| 4     | HV <sub>OUT</sub> 19 |
| 5     | HV <sub>OUT</sub> 18 |
| 6     | HV <sub>OUT</sub> 17 |
| 7     | HV <sub>OUT</sub> 16 |
| 8     | HV <sub>OUT</sub> 15 |
| 9     | HV <sub>OUT</sub> 14 |
| 10    | HV <sub>OUT</sub> 13 |

| Pin # | Function             |
|-------|----------------------|
| 11    | HV <sub>OUT</sub> 12 |
| 12    | HV <sub>OUT</sub> 11 |
| 13    | BLANKING             |
| 14    | GND                  |
| 15    | CLOCK                |
| 16    | STROBE               |
| 17    | HV <sub>OUT</sub> 10 |
| 18    | HV <sub>OUT</sub> 9  |
| 19    | HV <sub>OUT</sub> 8  |
| 20    | HV <sub>OUT</sub> 7  |

| Pin # | Function            |
|-------|---------------------|
| 21    | HV <sub>OUT</sub> 6 |
| 22    | HV <sub>OUT</sub> 5 |
| 23    | HV <sub>OUT</sub> 4 |
| 24    | HV <sub>OUT</sub> 3 |
| 25    | HV <sub>OUT</sub> 2 |
| 26    | HV <sub>OUT</sub> 1 |
| 27    | Data In             |
| 28    | VDD                 |

## 28-Lead PDIP (.600in Row Spacing) Package Outline (P)

1.565x.580in body, .250in height (max), .100in pitch



**Note:**

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol                |     | A     | A1    | A2   | b                 | b1   | D     | D1                | E                 | E1   | e           | eA          | eB    | L    |
|-----------------------|-----|-------|-------|------|-------------------|------|-------|-------------------|-------------------|------|-------------|-------------|-------|------|
| Dimension<br>(inches) | MIN | .140* | .015  | .125 | .014              | .030 | 1.380 | .065 <sup>†</sup> | .590 <sup>†</sup> | .485 | .100<br>BSC | .600<br>BSC | .600* | .115 |
|                       | NOM | -     | -     | -    | -                 | -    | -     | -                 | -                 | -    |             |             | -     | -    |
|                       | MAX | .250  | .055* | .195 | .023 <sup>†</sup> | .070 | 1.565 | .085*             | .625              | .580 |             |             | .700  | .200 |

JEDEC Registration MS-011, Variation AB, Issue B, June, 1988.

\* This dimension is not specified in the JEDEC drawing.

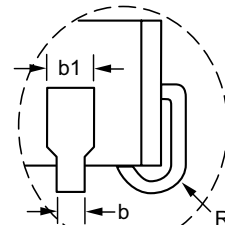
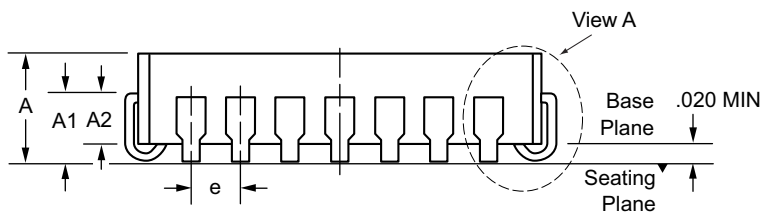
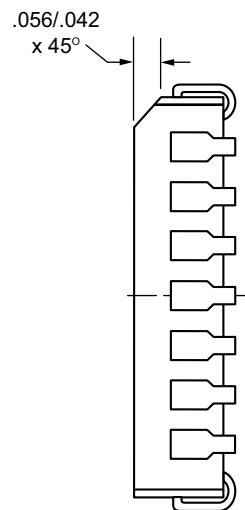
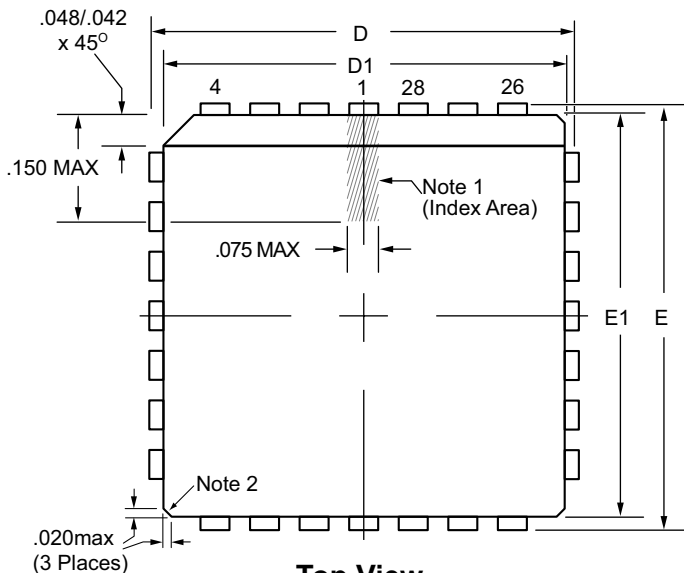
† This dimension differs from the JEDEC drawing.

**Drawings not to scale.**

**Supertex Doc. #: DSPD-28DIPP, Version B041009.**

## 28-Lead PLCC Package Outline (PJ)

**.453x.453in. body, .180in. height (max), .050in. pitch**



### Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Actual shape of this feature may vary.

| Symbol             |     | A    | A1   | A2   | b    | b1   | D    | D1   | E    | E1   | e        | R    |
|--------------------|-----|------|------|------|------|------|------|------|------|------|----------|------|
| Dimension (inches) | MIN | .165 | .090 | .062 | .013 | .026 | .485 | .450 | .485 | .450 | .050 BSC | .025 |
|                    | NOM | .172 | .105 | -    | -    | -    | .490 | .453 | .490 | .453 |          | .035 |
|                    | MAX | .180 | .120 | .083 | .021 | .032 | .495 | .456 | .495 | .456 |          | .045 |

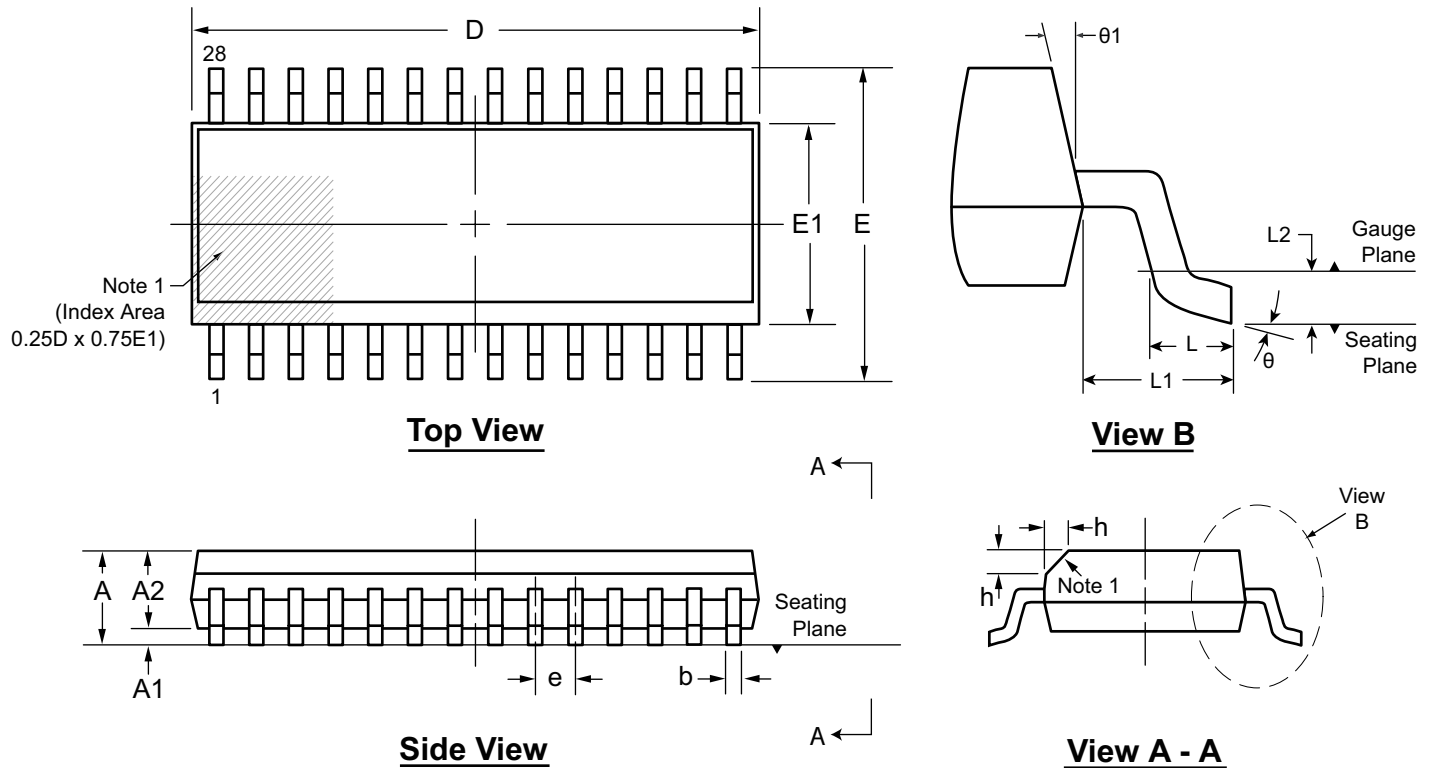
JEDEC Registration MS-018, Variation AB, Issue A, June, 1993.

Drawings not to scale.

Supertex Doc. #: DSPD-28PLCCPJ, Version B031111.

## 28-Lead SOW (Wide Body) Package Outline (WG)

17.90x7.50mm body, 2.65mm height (max), 1.27mm pitch



**Note:**

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol            |     | A     | A1   | A2    | b    | D      | E      | E1    | e           | h    | L    | L1          | L2          | θ  | θ1  |
|-------------------|-----|-------|------|-------|------|--------|--------|-------|-------------|------|------|-------------|-------------|----|-----|
| Dimension<br>(mm) | MIN | 2.15* | 0.10 | 2.05  | 0.31 | 17.70* | 9.97*  | 7.40* | 1.27<br>BSC | 0.25 | 0.40 | 1.40<br>REF | 0.25<br>BSC | 0° | 5°  |
|                   | NOM | -     | -    | -     | -    | 17.90  | 10.30  | 7.50  |             | -    | -    |             |             | -  | -   |
|                   | MAX | 2.65  | 0.30 | 2.55* | 0.51 | 18.10* | 10.63* | 7.60* |             | 0.75 | 1.27 |             |             | 8° | 15° |

JEDEC Registration MS-013, Variation AE, Issue E, Sep. 2005.

\* This dimension is not specified in the JEDEC drawing.

**Drawings are not to scale.**

**Supertex Doc. #: DSPD-28SOWWG, Version D041309.**

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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