

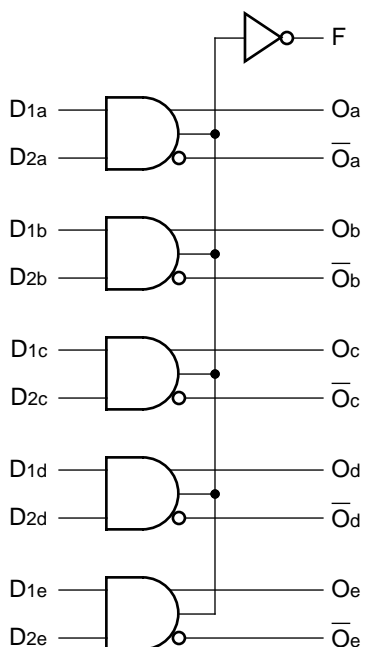
## FEATURES

- Max. propagation delay of 1050ps
- IEE min. of -60mA
- Extended supply voltage option:  
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75kΩ input pull-down resistors
- 40% faster than Fairchild 300K at lower power
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

## DESCRIPTION

The SY100S304 is an ultra-fast quint AND/NAND gate designed for use in high-performance ECL systems. This device also features a Function (F) output which is the wire-NOR of the AND gate outputs. The inputs on the device have 75kΩ pull-down resistors.

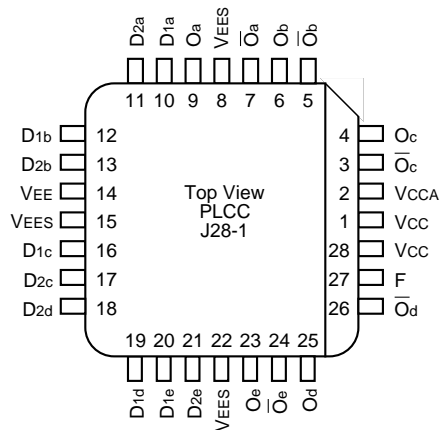
## BLOCK DIAGRAM



## PIN NAMES

Pin	Function
Dna – Dne	Data Inputs (n-1...5)
E	Enable Input
Oa – Oe	Data Outputs
$\overline{Oa} - \overline{Oe}$	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S304JC	J28-1	Commercial	SY100S304JC	Sn-Pb
SY100S304JCTR <sup>(1)</sup>	J28-1	Commercial	SY100S304JC	Sn-Pb
SY100S304JZ <sup>(2)</sup>	J28-1	Commercial	SY100S304JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S304JZTR <sup>(1, 2)</sup>	J28-1	Commercial	SY100S304JZ with Pb-Free bar-line indicator	Matte-Sn

- Notes:
- 1. Tape and Reel.
  - 2. Pb-Free package is recommended for new designs.

## DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

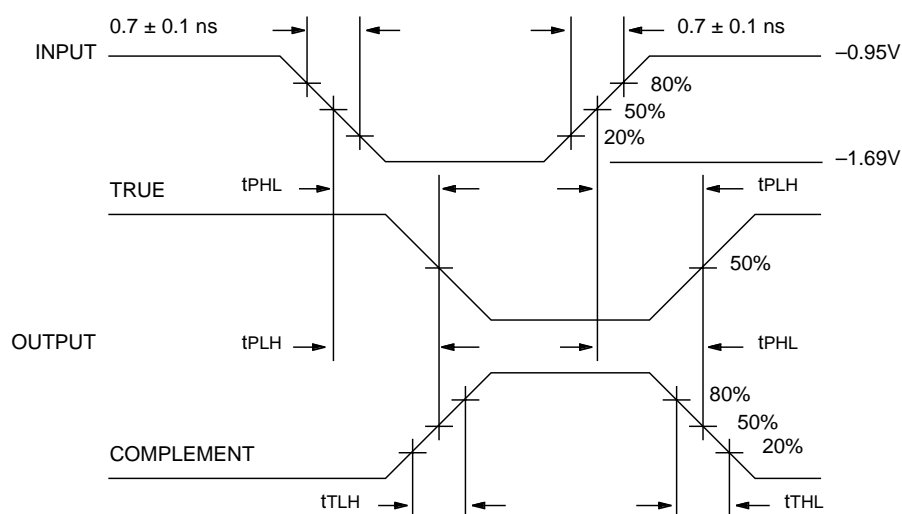
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$I_{IH}$	Input HIGH Current D2a — D2e D1a — D1e	—	—	250 250	$\mu A$	$V_{IN} = V_{IH} (Max.)$
$I_{EE}$	Power Supply Current	-60	-40	-30	mA	Inputs Open

## AC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Dna — Dne to O, $\bar{O}$	300	1050	300	1050	300	1050	ps	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to F	600	1550	600	1550	600	1550	ps	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

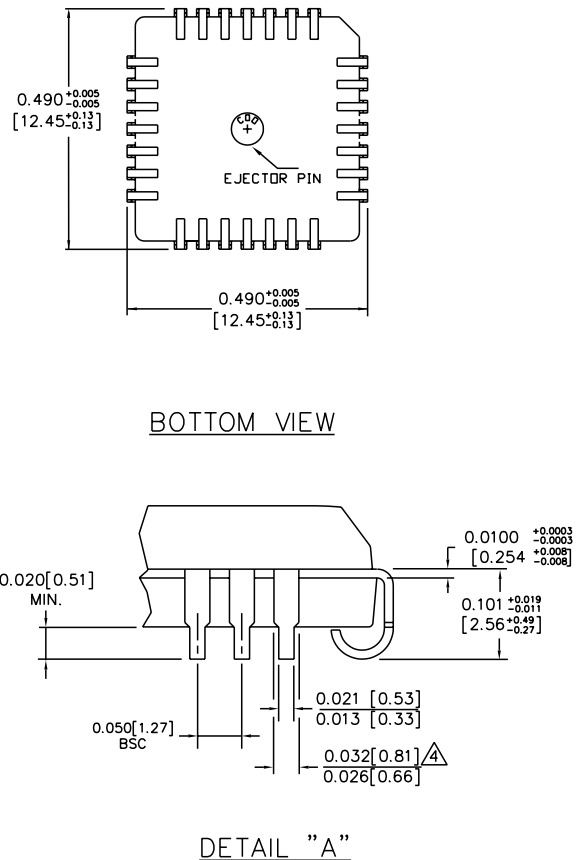
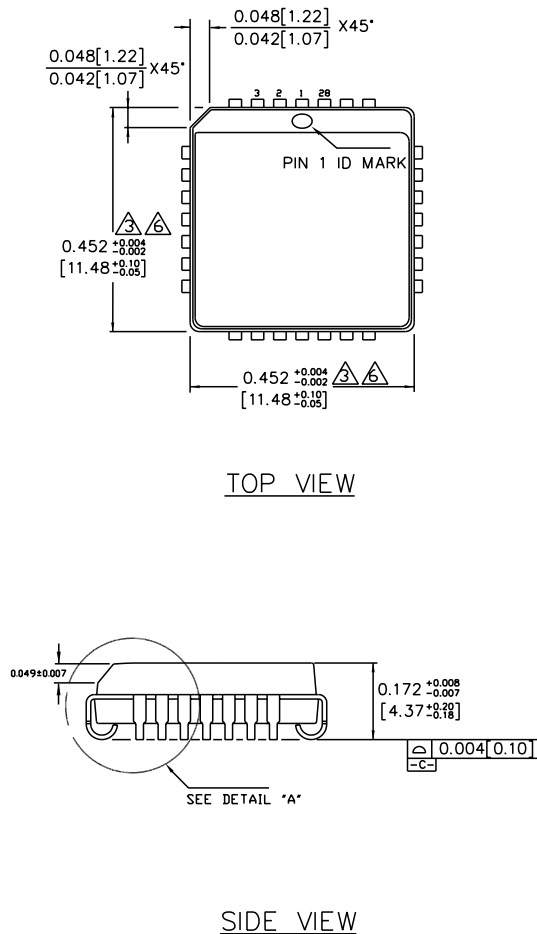
## TIMING DIAGRAM



Propagation Delay and Transition Times

### NOTE:

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

**28-PIN PLCC (J28-1)****NOTES:**

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. A

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