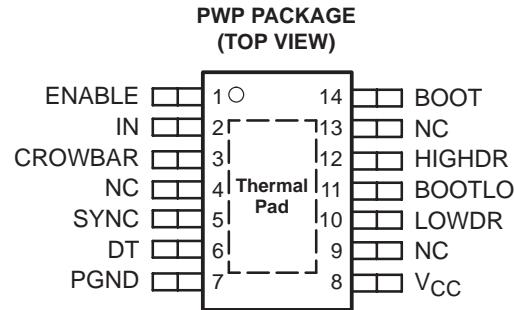
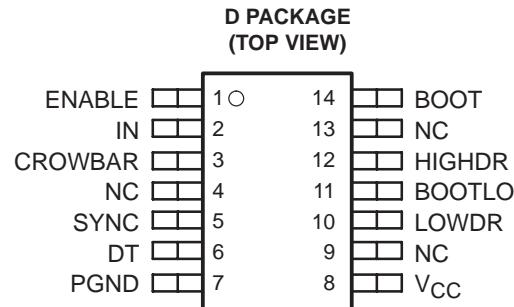


TPS2830, TPS2831
FAST SYNCHRONOUS-BUCK MOSFET DRIVERS
WITH DEAD-TIME CONTROL

SLVS196C – JANUARY1999 – REVISED JANUARY 2001

- Floating Bootstrap or Ground-Reference High-Side Driver
- Adaptive Dead-Time Control
- 50-ns Max Rise/Fall Times and 100-ns Max Propagation Delay – 3.3-nF Load
- Ideal for High-Current Single or Multiphase Power Supplies
- 2.4-A Typical Peak Output Current
- 4.5-V to 15-V Supply Voltage Range
- Internal Schottky Bootstrap Diode
- SYNC Control for Synchronous or Nonsynchronous Operation
- CROWBAR for OVP, Protects Against Faulted High-Side Power FETs
- Low Supply Current....3-mA Typical
- –40°C to 125°C Operating Virtual Junction Temperature Range
- Available in SOIC and TSSOP PowerPAD Packages



NC – No internal connection

description

The TPS2830 and TPS2831 are MOSFET drivers for synchronous-buck power stages. These devices are ideal for designing a high-performance power supply using switching controllers that do not have MOSFET drivers. The drivers are designed to deliver 2.4-A peak currents into large capacitive loads. The high-side driver can be configured as a ground-reference driver or as a floating bootstrap driver. An adaptive dead-time control circuit eliminates shoot-through currents through the main power FETs during switching transitions, providing higher efficiency for the buck regulator. The TPS2830/31 drivers have additional control functions: ENABLE, SYNC, and CROWBAR. Both drivers are off when ENABLE is low. The driver is configured as a nonsynchronous-buck driver, disabling the low side driver when SYNC is low. The CROWBAR function turns on the low-side power FET, overriding the IN signal, for over-voltage protection against faulted high-side power FETs.

The TPS2830 has a noninverting input. The TPS2831 has an inverting input. The TPS2830/31 drivers are available in 14-terminal SOIC and thermally-enhanced TSSOP PowerPAD™ packages, and operate over a virtual junction temperature range of –40°C to 125°C.

Related Synchronous MOSFET Drivers

DEVICE NAME	ADDITIONAL FEATURES	INPUTS	
TPS2832	W/O ENABLE, SYNC, and CROWBAR	CMOS	Noninverted
TPS2833			Inverted
TPS2834	ENABLE, SYNC, and CROWBAR	TTL	Noninverted
TPS2835			Inverted
TPS2836	W/O ENABLE, SYNC, and CROWBAR	TTL	Noninverted
TPS2837			Inverted



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TPS2830, TPS2831
FAST SYNCHRONOUS-BUCK MOSFET DRIVERS
WITH DEAD-TIME CONTROL

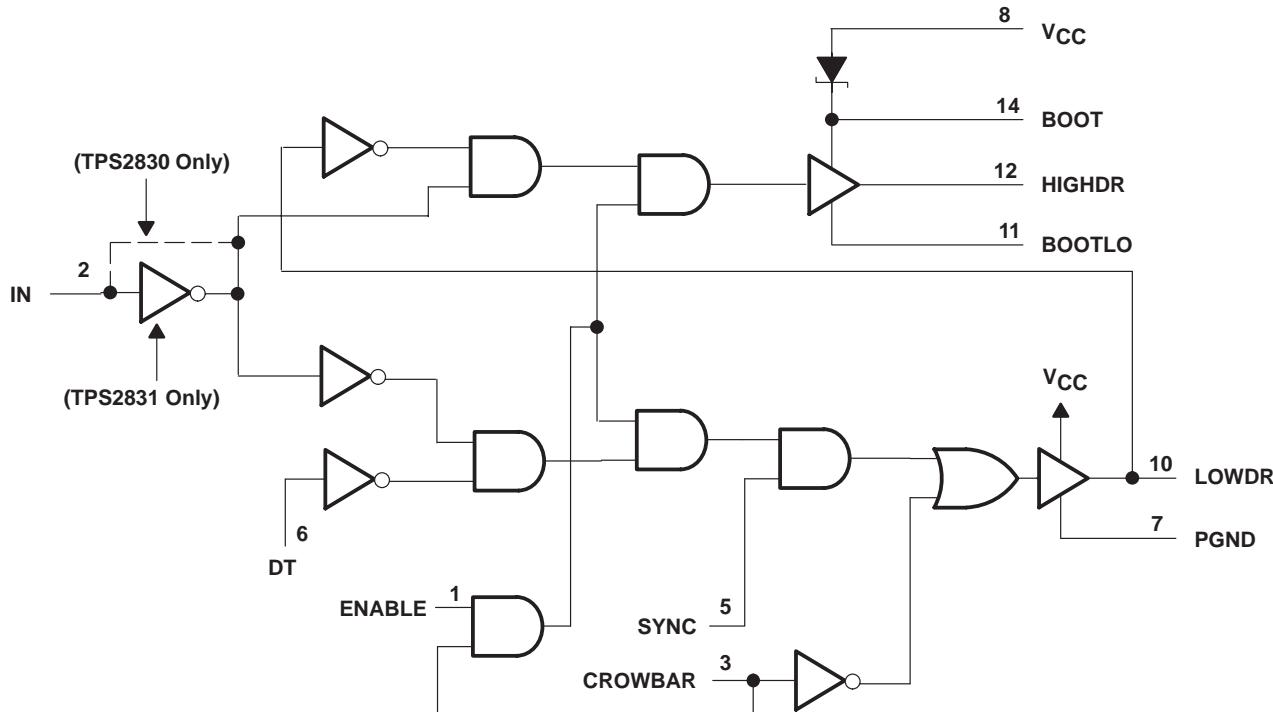
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AVAILABLE OPTIONS

T _J	PACKAGED DEVICES	
	SOIC (D)	TSSOP (PWP)
–40°C to 125°C	TPS2830D TPS2831D	TPS2830PWP TPS2831PWP

The D and PWP packages are available taped and reeled. Add R suffix to device type (e.g., TPS2830DR)

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
BOOT	14	I	Bootstrap terminal. A ceramic capacitor is connected between BOOT and BOOTLO terminals to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically between 0.1 μ F and 1 μ F. A 1-M Ω resistor should be connected across the bootstrap capacitor to provide a discharge path when the driver has been powered down.
BOOTLO	11	O	This terminal connects to the junction of the high-side and low-side MOSFETs.
CROWBAR	3	I	CROWBAR can be driven by an external OVP circuit to protect against a short across the high-side MOSFET. If CROWBAR is driven low, the low-side driver will be turned on and the high-side driver will be turned off, independent of the status of all other control terminals.
DT	6	I	Dead-time control terminal. Connect DT to the junction of the high-side and low-side MOSFETs.
ENABLE	1	I	If ENABLE is low, both drivers are off.
HIGHDR	12	O	Output drive for the high-side power MOSFET
IN	2	I	Input signal to the MOSFET drivers (noninverting input for the TPS2830; inverting input for the TPS2831).
LOWDR	10	O	Output drive for the low-side power MOSFET
NC	4, 9, 13		No internal connection
PGND	7		Power ground. Connect to the FET power ground
SYNC	5	I	Synchronous Rectifier Enable terminal. If SYNC is low, the low-side driver is always off; If SYNC is high, the low-side driver provides gate drive to the low-side MOSFET.
V _{CC}	8	I	Input supply. Recommended that a 1- μ F capacitor be connected from V _{CC} to PGND.

detailed description

low-side driver

The low-side driver is designed to drive low R_{ds(on)} N-channel MOSFETs. The current rating of the driver is 2 A, source and sink.

high-side driver

The high-side driver is designed to drive low R_{ds(on)} N-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The high-side driver can be configured as a GND-reference driver or as a floating bootstrap driver. The internal bootstrap diode is a Schottky, for improved drive efficiency. The maximum voltage that can be applied from BOOT to ground is 30 V.

dead-time (DT) control†

Dead-time control prevents shoot through current from flowing through the main power FETs during switching transitions by controlling the turn-on times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate drive voltage to the low-side FET is low, and the low-side driver is not allowed to turn on until the voltage at the junction of the power FETs (V_{drain}) is low; the DT terminal connects to the junction of the power FETs.

ENABLE†

The ENABLE terminal enables the drivers. When enable is low, the output drivers are low.

INT†

The IN terminal is the input control signal for the drivers. The TPS2830 has a noninverting input; the TPS2831 has an inverting input.

†High-level input voltages on ENABLE, SYNC, CROWBAR, IN, and DT must be greater than or equal to 0.7V_{CC}.

TPS2830, TPS2831 FAST SYNCHRONOUS-BUCK MOSFET DRIVERS WITH DEAD-TIME CONTROL

SLVS196C – JANUARY1999 – REVISED JANUARY 2001

detailed description (continued)

SYNCT

The SYNC terminal controls whether the drivers operate in synchronous or nonsynchronous mode. In synchronous mode, the low-side FET is operated as a synchronous rectifier. In nonsynchronous mode, the low-side FET is always off.

CROWBART[†]

The CROWBAR terminal overrides the normal operation of the driver. When the CROWBAR terminal is low, the low-side FET turns on to act as a clamp, protecting the output voltage of the dc/dc converter against over voltages due to a short across the high-side FET. VIN should be fused to protect the low-side FET.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V _{CC} (see Note 1)	-0.3 V to 16 V
Input voltage range: BOOT to PGND (high-side driver ON)	-0.3 V to 30 V
BOOTLO to PGND	-0.3 V to 16 V
BOOT to BOOTLO	-0.3 V to 16 V
ENABLE, SYNC, and CROWBAR (see Note 2)	-0.3 V to 16 V
IN (see Note 2)	-0.3 V to 16 V
DT (see Note 2)	-0.3 V to 30 V
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T _J	-40°C to 125°C
Storage temperature range, T _{stg}	-65°C to 150°C
Lead temperature soldering 1.6 mm (1/16 inch) from case for 10 seconds	260°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Unless otherwise specified, all voltages are with respect to PGND.

2. High-level input voltages on the ENABLE, SYNC, CROWBAR, IN, and DT terminals must be greater than or equal to 0.7V_{CC}.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C	DERATING FACTOR	T _A = 70°C	T _A = 85°C
PWP with solder [§]	2668	26.68 mW/°C	1467	1067
PWP without solder [§]	1024	10.24 mW/°C	563	409
D	749	7.49 mW/°C	412	300

JUNCTION-CASE THERMAL RESISTANCE TABLE

PWP	Junction-case thermal resistance	2.07 °C/W

[§] Test Board Conditions:

1. Thickness: 0.062"
2. 3" × 3" (for packages <27 mm long)
3. 4" × 4" (for packages >27 mm long)
4. 2 oz copper traces located on the top of the board (0.071 mm thick)
5. Copper areas located on the top and bottom of the PCB for soldering
6. Power and ground planes, 1 oz copper (0.036 mm thick)
7. Thermal vias, 0.33 mm diameter, 1.5 mm pitch
8. Thermal isolation of power plane

For more information, refer to TI technical brief, literature number SLMA002.

[†]High-level input voltages on ENABLE, SYNC, CROWBAR, IN, and DT must be greater than or equal to 0.7V_{CC}.



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recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	15		V
Input voltage	BOOT to PGND	4.5	28		V

**electrical characteristics over recommended operating virtual junction temperature range,
 $V_{CC} = 6.5$ V, ENABLE = High, $C_L = 3.3$ nF (unless otherwise noted)**

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range		4.5	15		V
V_{CC}	Quiescent current	$V_{ENABLE} = \text{LOW}$, $V_{CC} = 15$ V		100		μA
		$V_{ENABLE} = \text{HIGH}$, $V_{CC} = 15$ V		0.1		mA
		$V_{ENABLE} = \text{HIGH}$, $V_{CC} = 12$ V, $f_{SWX} = 200$ kHz, BOOTLO grounded, $C_{HIGHDR} = 50$ pF, $C_{LOWDR} = 50$ pF, See Note 3		3		

NOTE 3: Ensured by design, not production tested.

output drivers

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Peak output-current	High-side sink (see Note 4)	$V_{BOOT} - V_{BOOTLO} = 4.5$ V, $V_{HIGHDR} = 4$ V	0.7	1.1		A
		$V_{BOOT} - V_{BOOTLO} = 6.5$ V, $V_{HIGHDR} = 5$ V	1.1	1.5		
		$V_{BOOT} - V_{BOOTLO} = 12$ V, $V_{HIGHDR} = 10.5$ V	2	2.4		
	High-side source (see Note 4)	$V_{BOOT} - V_{BOOTLO} = 4.5$ V, $V_{HIGHDR} = 0.5$ V	1.2	1.4		A
		$V_{BOOT} - V_{BOOTLO} = 6.5$ V, $V_{HIGHDR} = 1.5$ V	1.3	1.6		
		$V_{BOOT} - V_{BOOTLO} = 12$ V, $V_{HIGHDR} = 1.5$ V	2.3	2.7		
	Low-side sink (see Note 4)	$V_{CC} = 4.5$ V, $V_{LOWDR} = 4$ V	1.3	1.8		A
		$V_{CC} = 6.5$ V, $V_{LOWDR} = 5$ V	2	2.5		
		$V_{CC} = 12$ V, $V_{LOWDR} = 10.5$ V	3	3.5		
	Low-side source (see Note 4)	$V_{CC} = 4.5$ V, $V_{LOWDR} = 0.5$ V	1.4	1.7		A
		$V_{CC} = 6.5$ V, $V_{LOWDR} = 1.5$ V	2	2.4		
		$V_{CC} = 12$ V, $V_{LOWDR} = 1.5$ V	2.5	3		
Output resistance	High-side sink (see Note 4)	$V_{BOOT} - V_{BOOTLO} = 4.5$ V, $V_{HIGHDR} = 0.5$ V		5		Ω
		$V_{BOOT} - V_{BOOTLO} = 6.5$ V, $V_{HIGHDR} = 0.5$ V		5		
		$V_{BOOT} - V_{BOOTLO} = 12$ V, $V_{HIGHDR} = 0.5$ V		5		
	High-side source (see Note 4)	$V_{BOOT} - V_{BOOTLO} = 4.5$ V, $V_{HIGHDR} = 4$ V		75		Ω
		$V_{BOOT} - V_{BOOTLO} = 6.5$ V, $V_{HIGHDR} = 6$ V		75		
		$V_{BOOT} - V_{BOOTLO} = 12$ V, $V_{HIGHDR} = 11.5$ V		75		
	Low-side sink (see Note 4)	$V_{DRV} = 4.5$ V, $V_{LOWDR} = 0.5$ V		9		Ω
		$V_{DRV} = 6.5$ V, $V_{LOWDR} = 0.5$ V		7.5		
		$V_{DRV} = 12$ V, $V_{LOWDR} = 0.5$ V		6		
	Low-side source (see Note 4)	$V_{DRV} = 4.5$ V, $V_{LOWDR} = 4$ V		75		Ω
		$V_{DRV} = 6.5$ V, $V_{LOWDR} = 6$ V		75		
		$V_{DRV} = 12$ V, $V_{LOWDR} = 11.5$ V		75		

NOTES: 3. Ensured by design, not production tested.

4. The pullup/pulldown circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{ds(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

TPS2830, TPS2831
FAST SYNCHRONOUS-BUCK MOSFET DRIVERS
WITH DEAD-TIME CONTROL

SLVS196C – JANUARY1999 – REVISED JANUARY 2001

**electrical characteristics over recommended operating virtual junction temperature range,
 $V_{CC} = 6.5$ V, ENABLE = High, $C_L = 3.3$ nF (unless otherwise noted) (continued)**

dead-time control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	LOWDR	0.7 V_{CC}			V
V_{IL}	Low-level input voltage			1		V
V_{IH}	High-level input voltage	DT	0.7 V_{CC}			V
V_{IL}	Low-level input voltage			1		V

NOTE 3: Ensured by design, not production tested.

digital control terminals (IN, CROWBAR, ENABLE, SYNC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	Over the V_{CC} range	0.7 V_{CC}			V
V_{IL}	Low-level input voltage			1		V

**switching characteristics over recommended operating virtual junction temperature range,
ENABLE = High, $C_L = 3.3$ nF (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rise time	HIGHDR output (see Note 3)	$V_{BOOT} = 4.5$ V, $V_{BOOTLO} = 0$ V		60		ns
		$V_{BOOT} = 6.5$ V, $V_{BOOTLO} = 0$ V		50		
		$V_{BOOT} = 12$ V, $V_{BOOTLO} = 0$ V		50		
	LOWDR output (see Note 3)	$V_{CC} = 4.5$ V		40		ns
		$V_{CC} = 6.5$ V		30		
		$V_{CC} = 12$ V		30		
Fall time	HIGHDR output (see Note 3)	$V_{BOOT} = 4.5$ V, $V_{BOOTLO} = 0$ V		60		ns
		$V_{BOOT} = 6.5$ V, $V_{BOOTLO} = 0$ V		50		
		$V_{BOOT} = 12$ V, $V_{BOOTLO} = 0$ V		50		
	LOWDR output (see Note 3)	$V_{CC} = 4.5$ V		40		ns
		$V_{CC} = 6.5$ V		30		
		$V_{CC} = 12$ V		30		
Propagation delay time	HIGHDR going low (excluding dead time) (see Note 3)	$V_{BOOT} = 4.5$ V, $V_{BOOTLO} = 0$ V		130		ns
		$V_{BOOT} = 6.5$ V, $V_{BOOTLO} = 0$ V		100		
		$V_{BOOT} = 12$ V, $V_{BOOTLO} = 0$ V		75		
	LOWDR going high (excluding dead time) (see Note 3)	$V_{BOOT} = 4.5$ V, $V_{BOOTLO} = 0$ V		80		ns
		$V_{BOOT} = 6.5$ V, $V_{BOOTLO} = 0$ V		70		
		$V_{BOOT} = 12$ V, $V_{BOOTLO} = 0$ V		60		
Propagation delay time	LOWDR going low (excluding dead time) (see Note 3)	$V_{CC} = 4.5$ V		80		ns
		$V_{CC} = 6.5$ V		70		
		$V_{CC} = 12$ V		60		
Driver nonoverlap time	DT to LOWDR and LOWDR to HIGHDR (see Note 3)	$V_{CC} = 4.5$ V	40	170		ns
		$V_{CC} = 6.5$ V	25	135		
		$V_{CC} = 12$ V	15	85		

NOTE 3: Ensured by design, not production tested.

TYPICAL CHARACTERISTICS

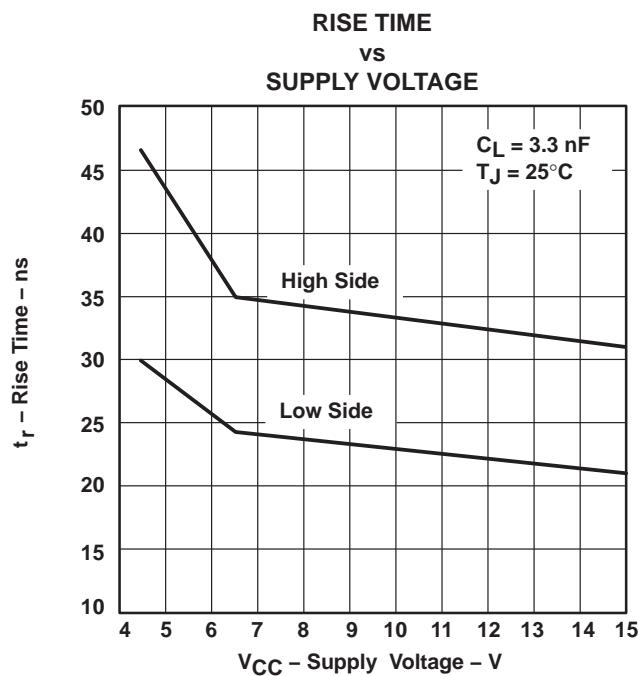


Figure 1

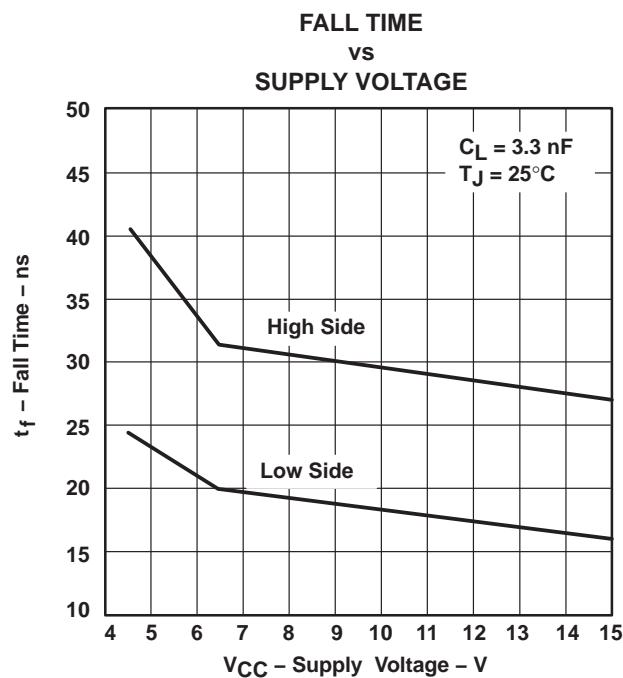


Figure 2

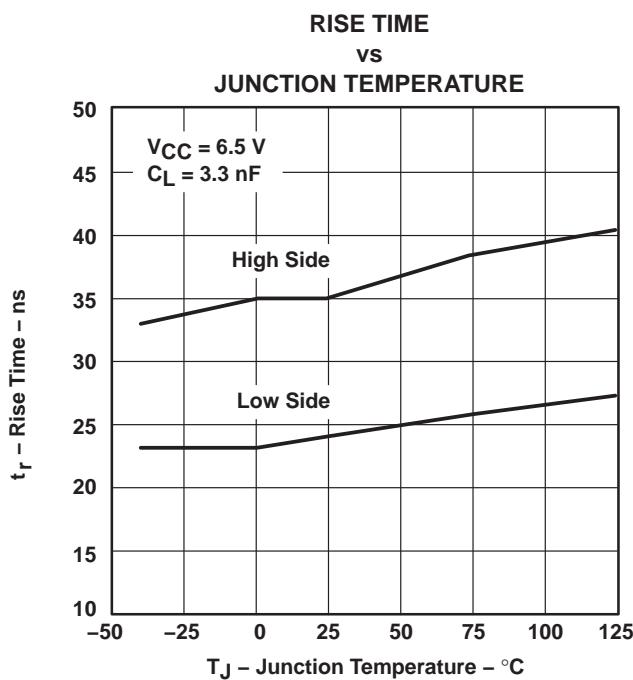


Figure 3

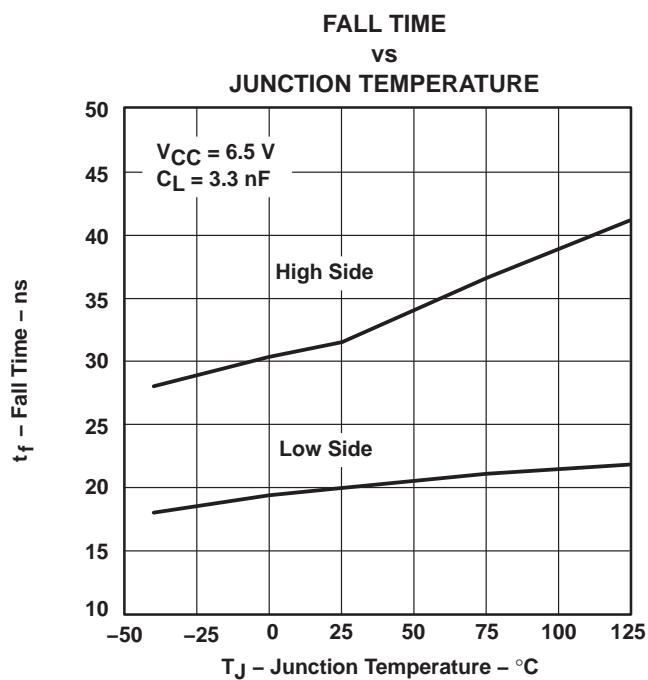
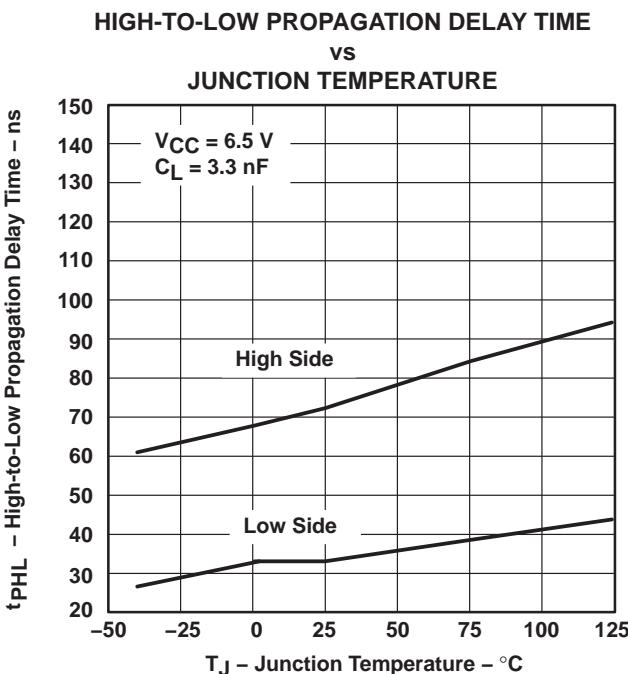
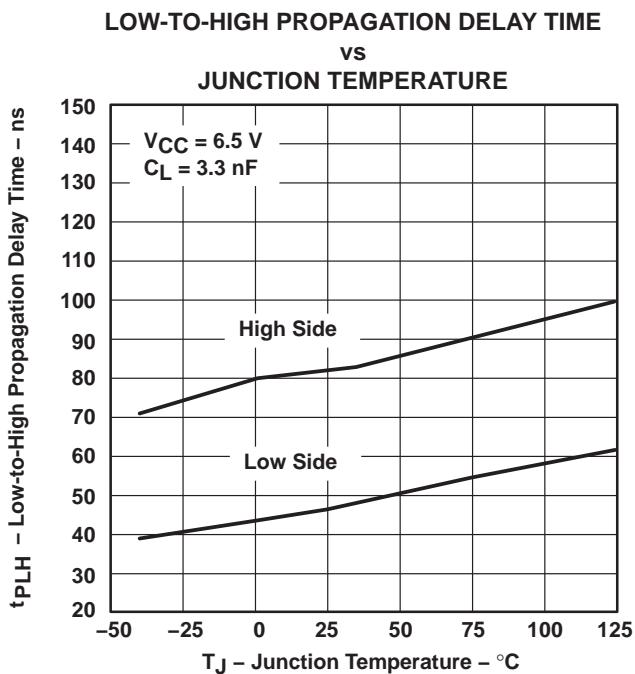
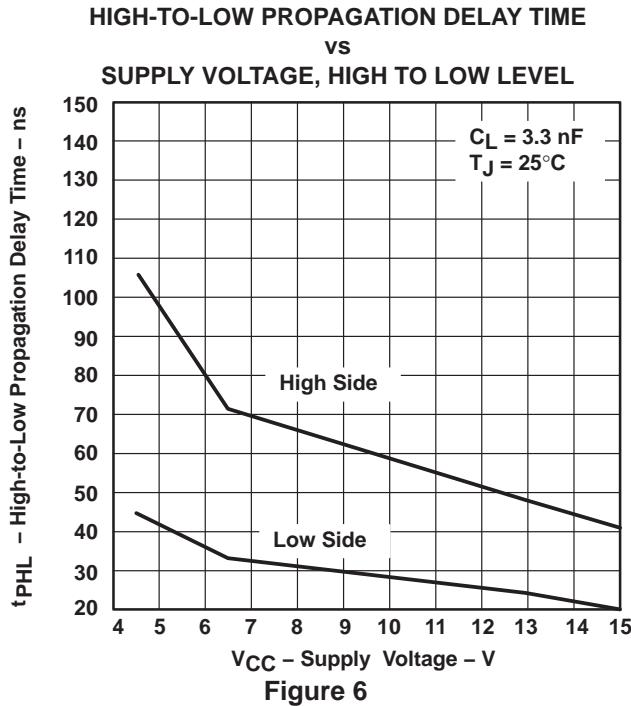
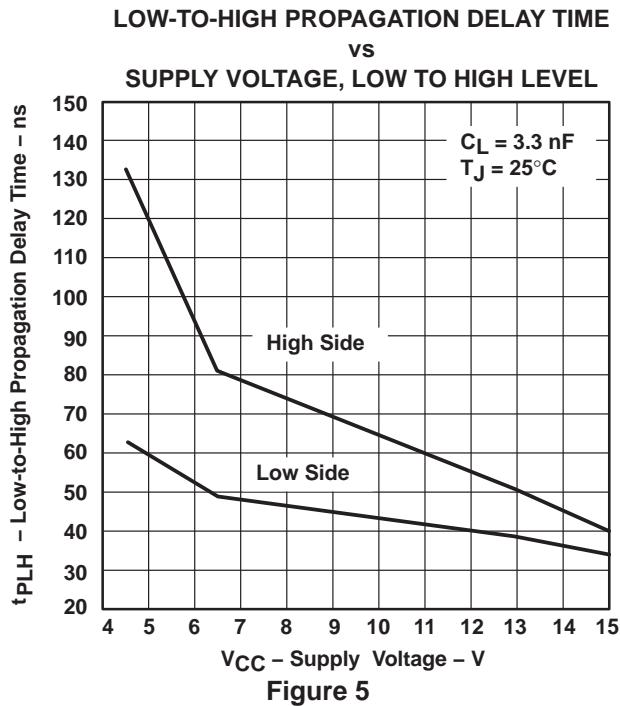


Figure 4

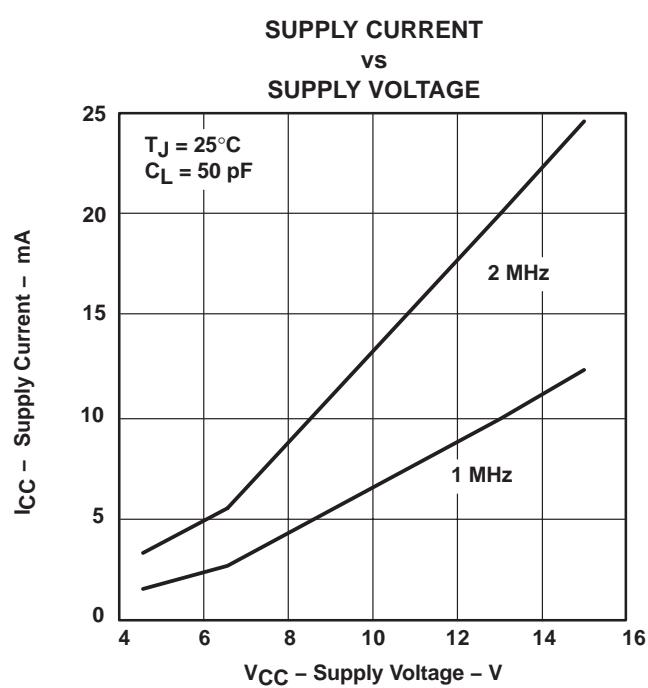
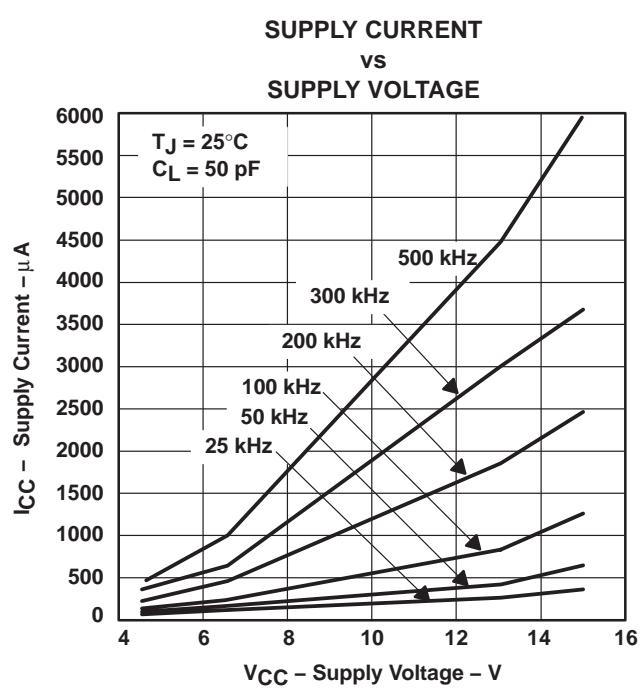
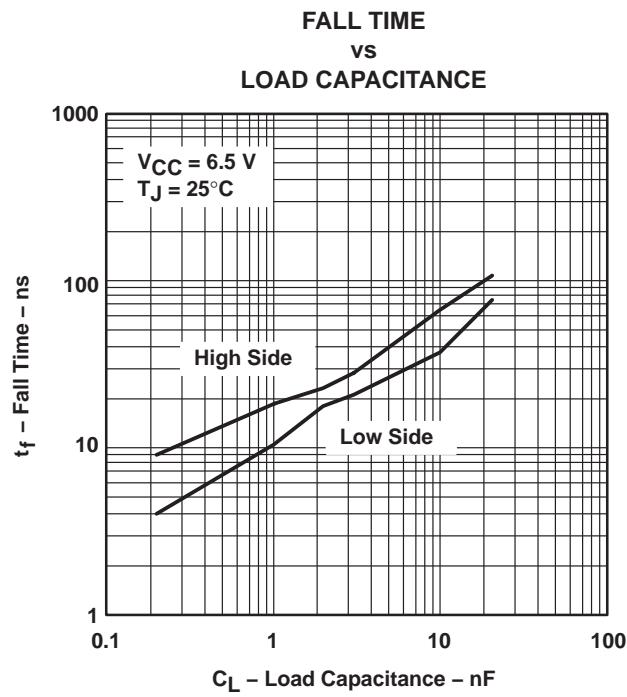
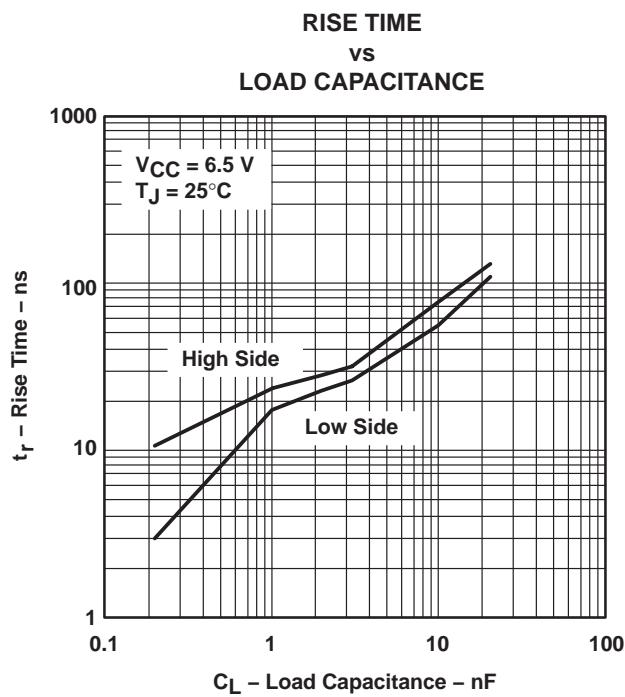
TPS2830, TPS2831
FAST SYNCHRONOUS-BUCK MOSFET DRIVERS
WITH DEAD-TIME CONTROL

SLVS196C – JANUARY1999 – REVISED JANUARY 2001

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



TPS2830, TPS2831
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WITH DEAD-TIME CONTROL

SLVS196C – JANUARY1999 – REVISED JANUARY 2001

TYPICAL CHARACTERISTICS

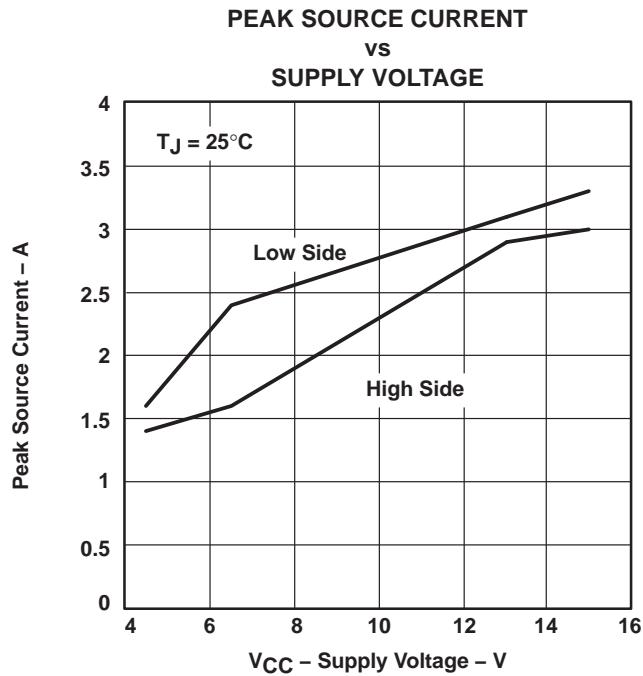


Figure 13

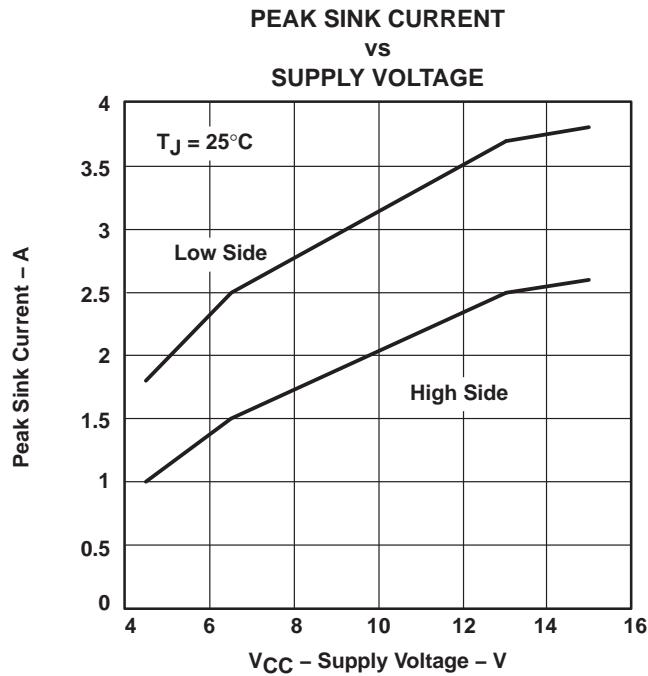


Figure 14

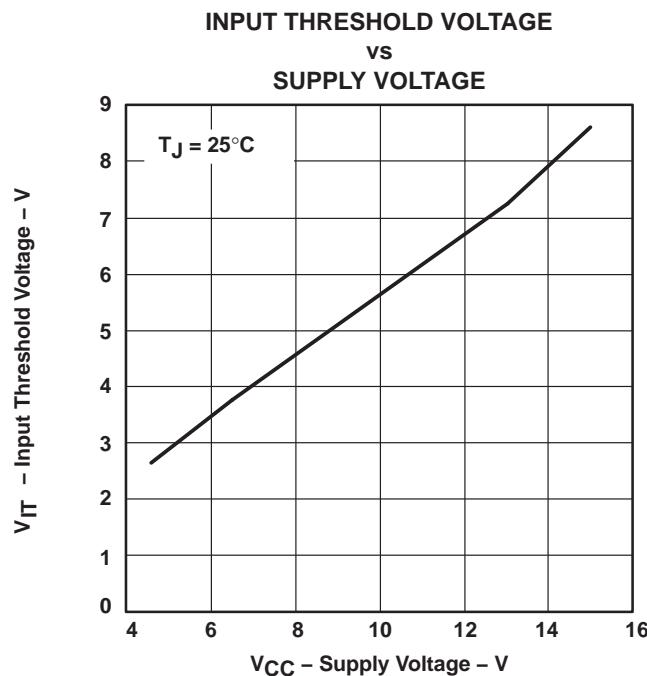


Figure 15

APPLICATION INFORMATION

Figure 16 shows the circuit schematic of a 100-kHz synchronous-buck converter implemented with a TL5001A pulse-width-modulation (PWM) controller and a TPS2831 driver. The converter operates over an input range from 4.5 V to 12 V and has a 3.3-V output. The circuit can supply 3 A continuous load. The converter achieves an efficiency of 94% for $V_{IN} = 5$ V, $I_{load} = 1$ A, and 93% for $V_{IN} = 5$ V, $I_{load} = 3$ A.

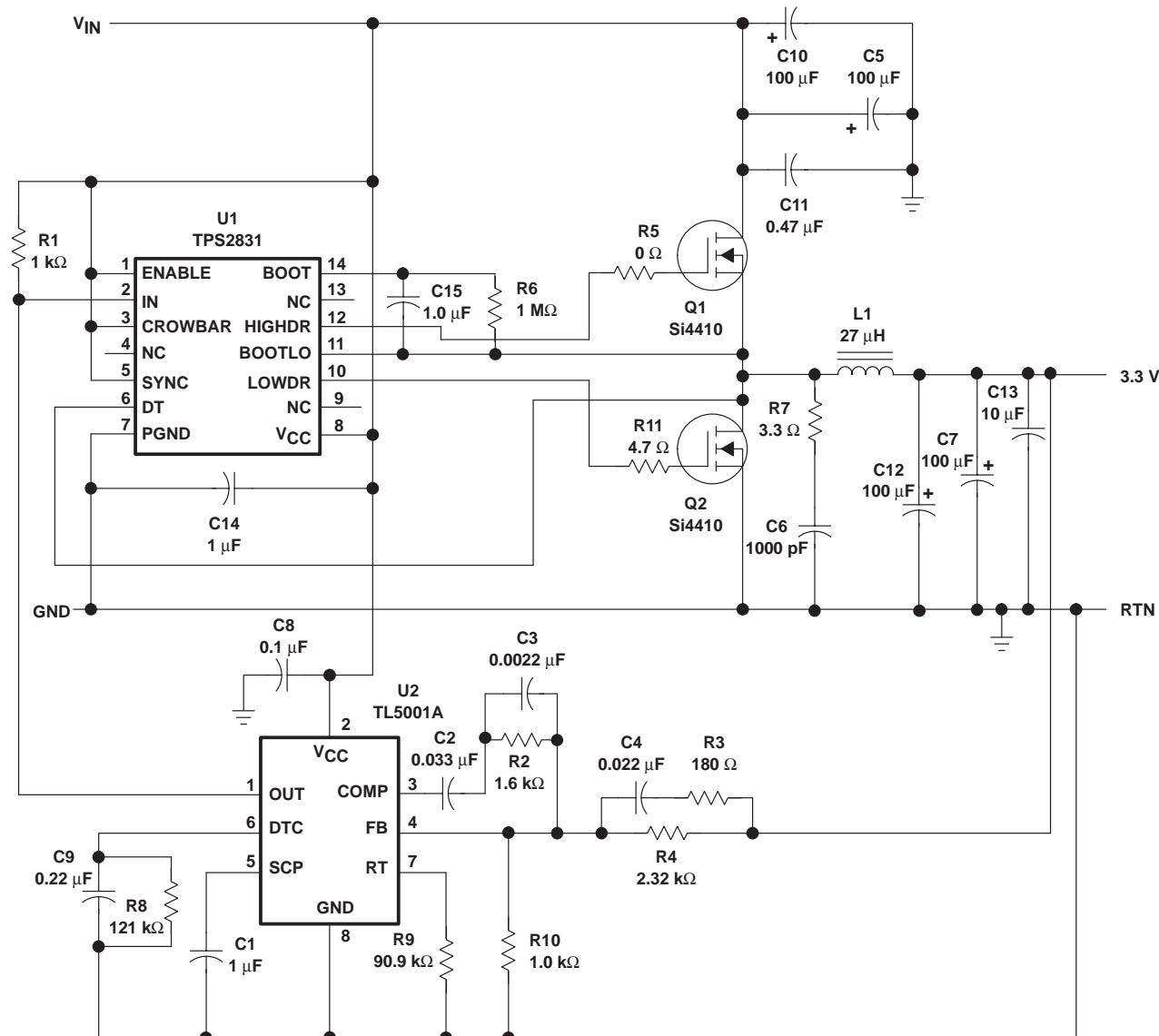


Figure 16. 3.3-V 3-A Synchronous-Buck Converter Circuit

**TPS2830, TPS2831
FAST SYNCHRONOUS-BUCK MOSFET DRIVERS
WITH DEAD-TIME CONTROL**

SLVS196C – JANUARY1999 – REVISED JANUARY 2001

APPLICATION INFORMATION

Great care should be taken when laying out the PC board. The power-processing section is the most critical and will generate large amounts of EMI if not properly configured. The junction of Q1, Q2, and L1 should be very tight. The connection from Q1 drain to the positive sides of C5, C10, and C11 and the connection from Q2 source to the negative sides of C5, C10, and C11 should be as short as possible. The negative terminals of C7 and C12 should also be connected to Q2 source.

Next, the traces from the MOSFET driver to the power switches should be considered. The BOOTLO signal from the junction of Q1 and Q2 carries the large gate drive current pulses and should be as heavy as the gate drive traces. The bypass capacitor (C14) should be tied directly across V_{CC} and PGND.

The next most sensitive node is the FB node on the controller (terminal 4 on the TL5001A) This node is very sensitive to noise pickup and should be isolated from the high-current power stage and be as short as possible. The ground around the controller and low-level circuitry should be tied to the power ground as the output. If these three areas are properly laid out, the rest of the circuit should not have any other EMI problems and the power supply will be relatively free of noise.



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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2830D	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2830
TPS2830D.A	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2830
TPS2830PWP	Active	Production	HTSSOP (PWP) 14	90 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2830
TPS2830PWP.A	Active	Production	HTSSOP (PWP) 14	90 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2830
TPS2830PWPR	Active	Production	HTSSOP (PWP) 14	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2830
TPS2830PWPR.A	Active	Production	HTSSOP (PWP) 14	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2830
TPS2831D	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2831
TPS2831D.A	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2831

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

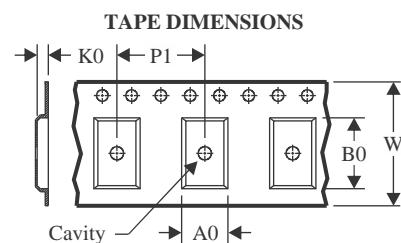
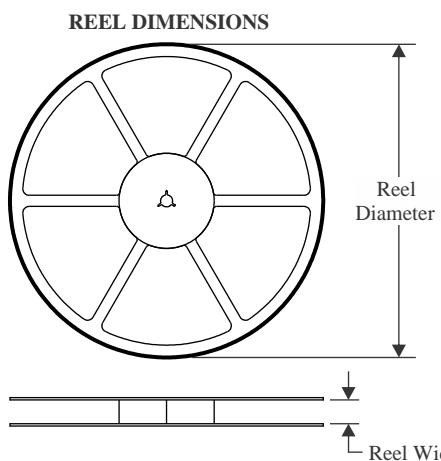
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2830PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2830PWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0

TUBE


*All dimensions are nominal

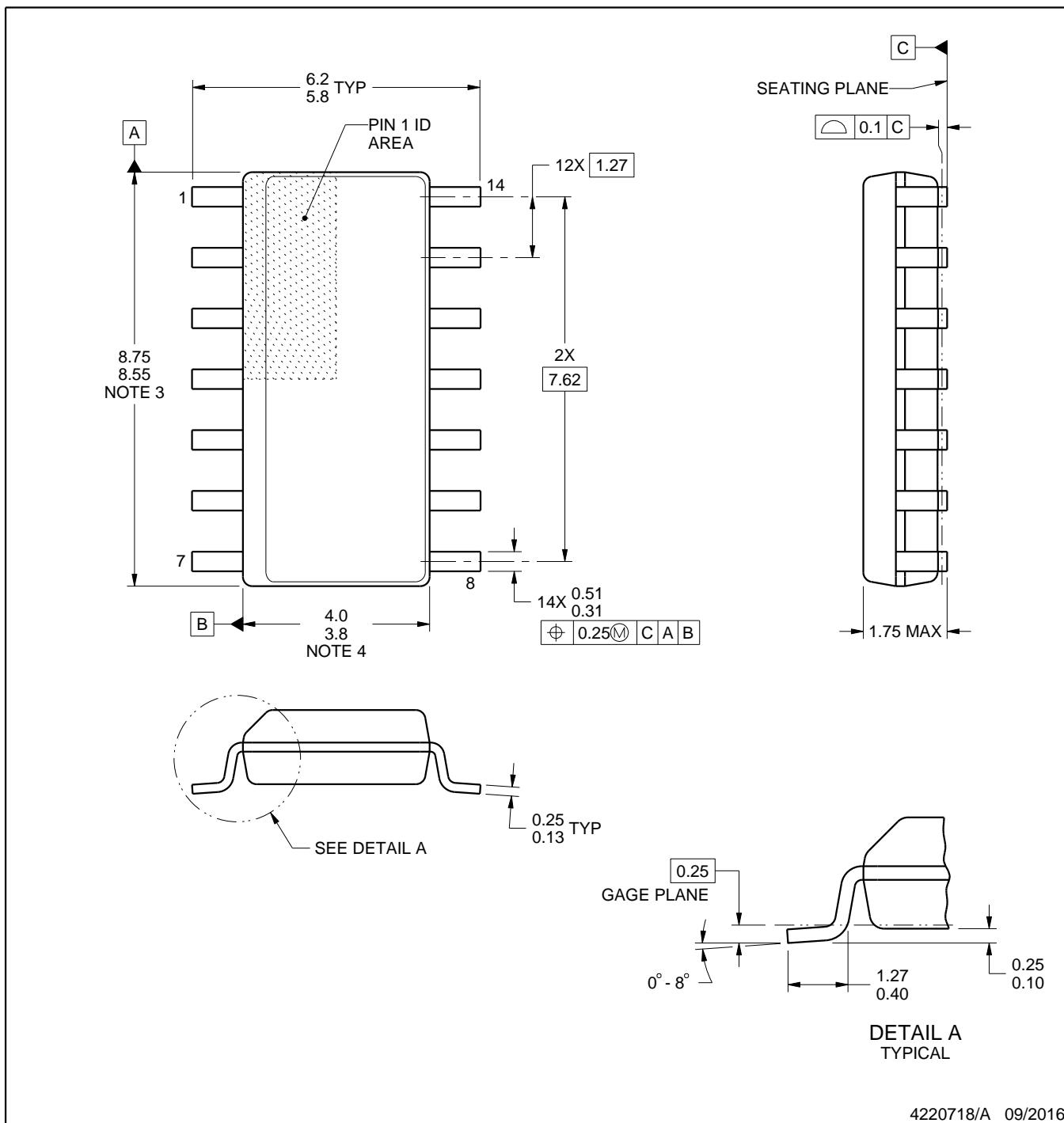
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
TPS2830D	D	SOIC	14	50	505.46	6.76	3810	4
TPS2830D.A	D	SOIC	14	50	505.46	6.76	3810	4
TPS2830PWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5
TPS2830PWP.A	PWP	HTSSOP	14	90	530	10.2	3600	3.5
TPS2831D	D	SOIC	14	50	505.46	6.76	3810	4
TPS2831D.A	D	SOIC	14	50	505.46	6.76	3810	4

PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

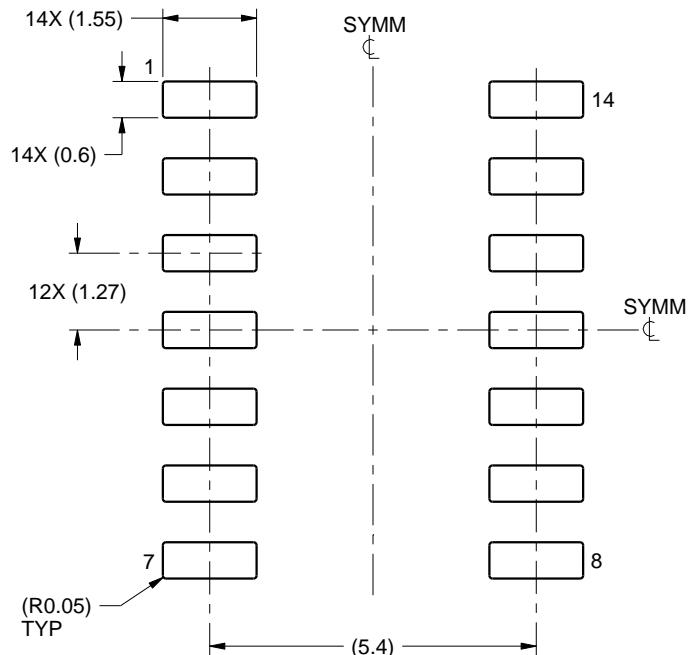
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

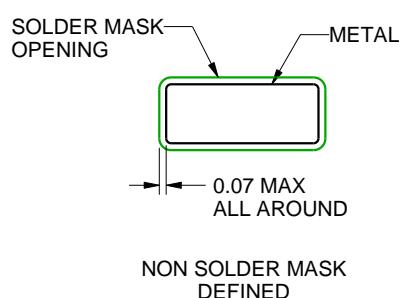
D0014A

SOIC - 1.75 mm max height

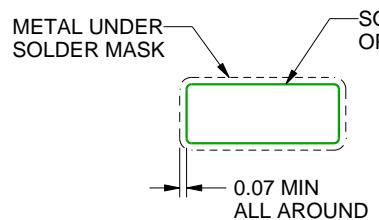
SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

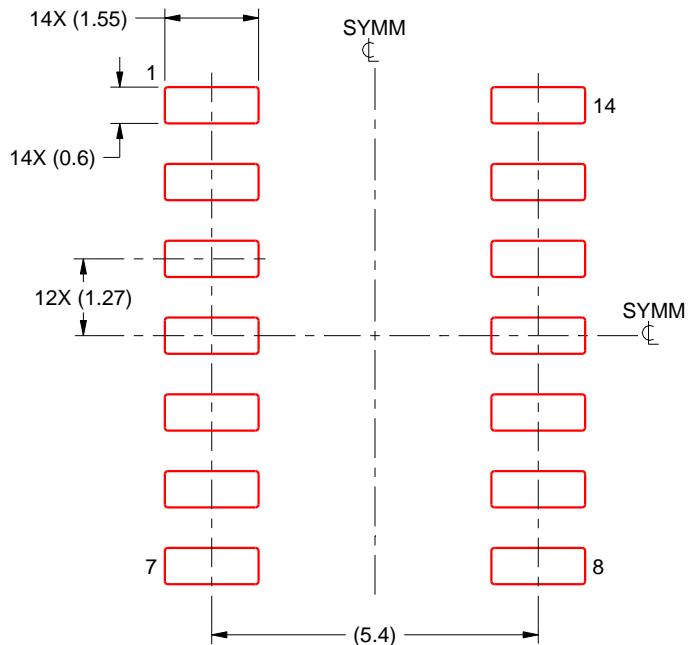
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

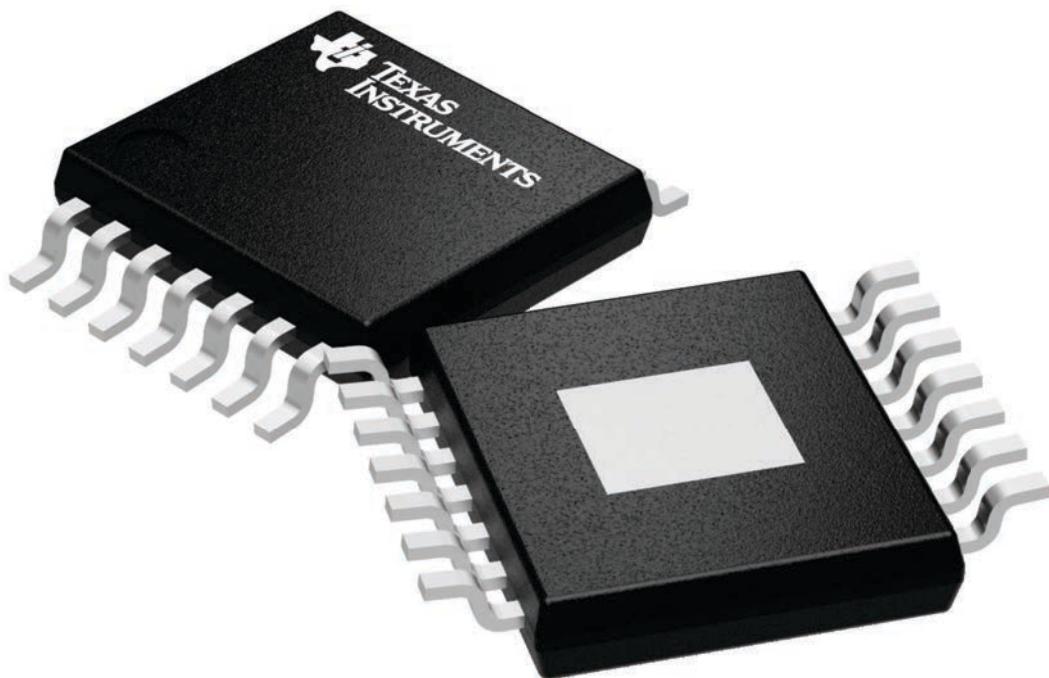
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224995/A

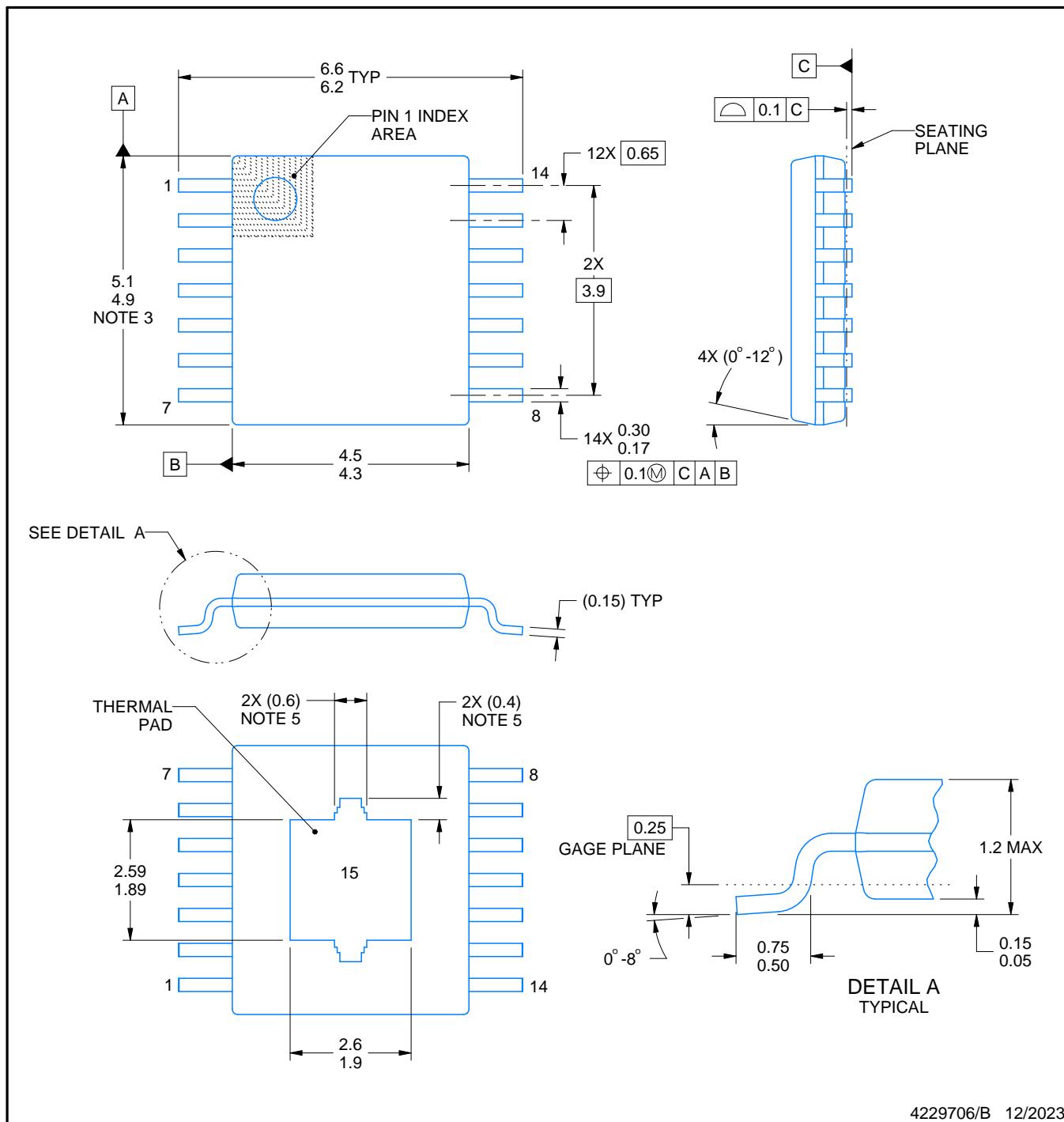
PACKAGE OUTLINE

PWP0014K



PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

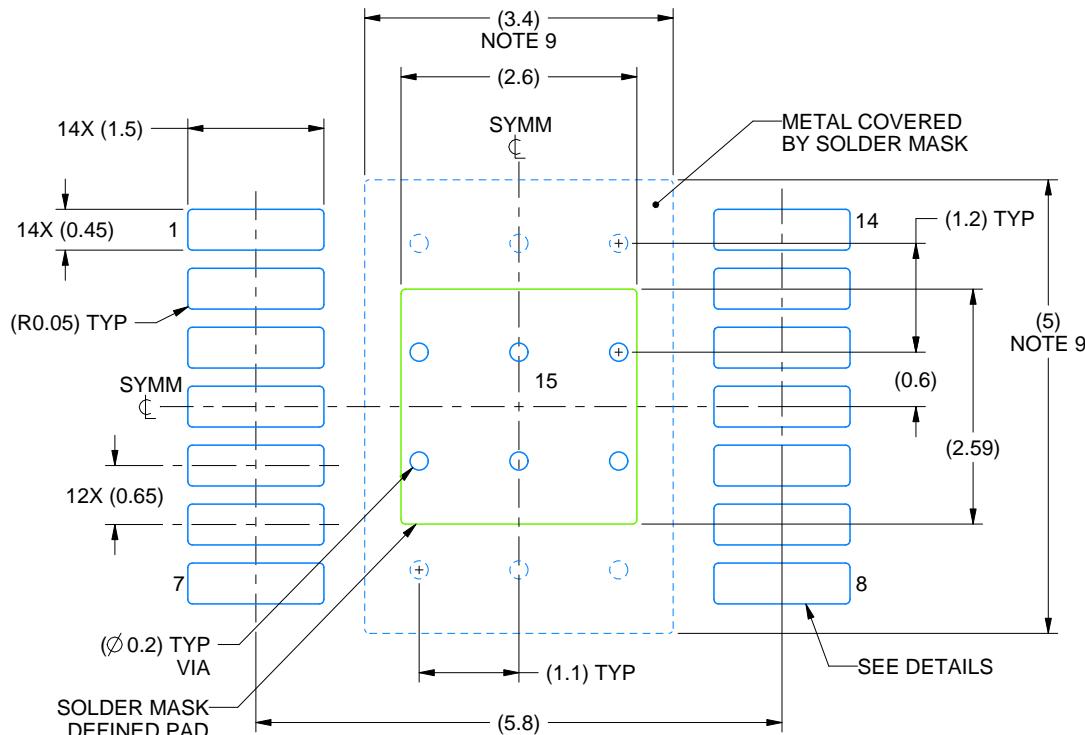
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

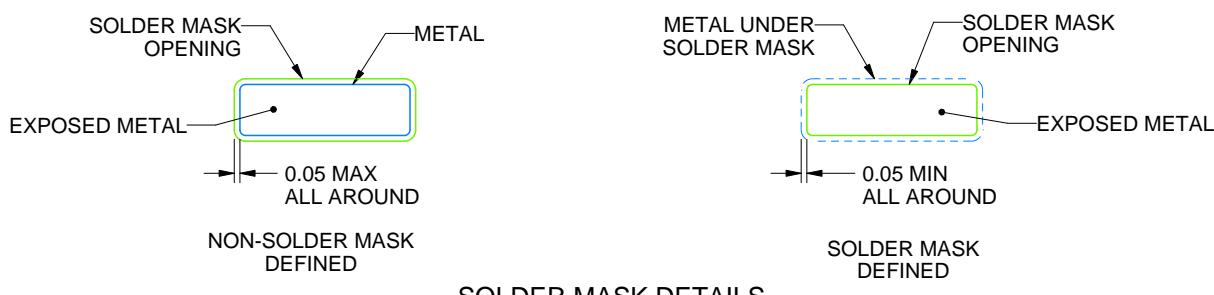
PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



4229706/R 12/2023

NOTES: (continued)

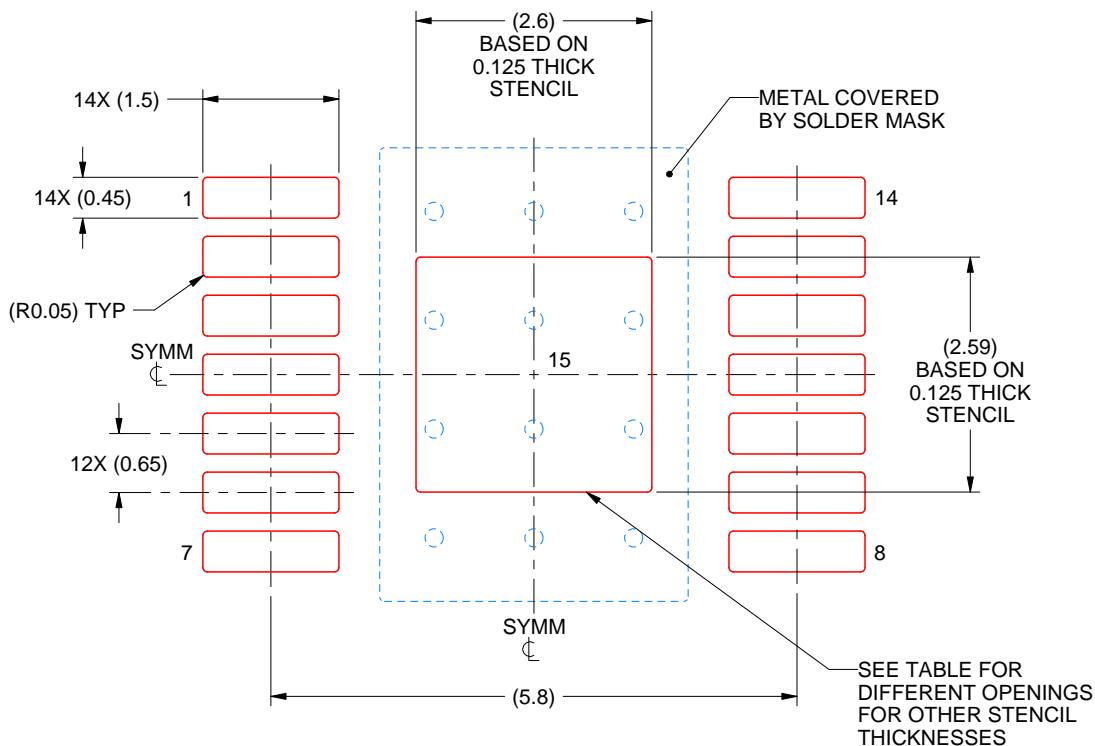
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

4229706/B 12/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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