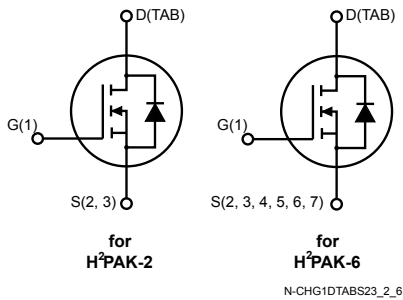
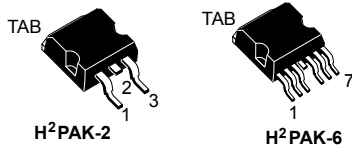


Automotive-grade N-channel 100 V, 2.1 mΩ typ., 180 A STripFET F7 Power MOSFETs in an H²PAK-2 and H²PAK-6 packages

Features



N-CHG1DTABS23_2_6

Order code	V _{DS}	R _{DS(on)} max.	I _D
STH315N10F7-2	100 V	2.3 mΩ	180 A
STH315N10F7-6			

- AEC-Q101 qualified
- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

These N-channel Power MOSFETs utilize STripFET F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Product status

STH315N10F7-2

STH315N10F7-6

Product summary

Order code	STH315N10F7-2
Marking	315N10F7
Package	H ² PAK-2
Packing	Tape and reel
Order code	STH315N10F7-6
Marking	315N10F7
Package	H ² PAK-6
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	180	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	180	A
$I_{DM}^{(2)}$	Drain current (pulsed)	720	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	315	W
	Derating factor	2.1	W/ $^\circ\text{C}$
$E_{AS}^{(3)}$	Single pulse avalanche energy	1	J
T_j	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature range		

1. Current limited by package.
2. Pulse width limited by safe operating area.
3. Starting $T_j=25\text{ }^\circ\text{C}$, $I_D=60\text{ A}$, $V_{DD}=50\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.48	$^\circ\text{C/W}$
$R_{thJB}^{(1)}$	Thermal resistance, junction-to-board	35	$^\circ\text{C/W}$

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 3. On/Off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	100			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			100	μA
I_{GSS}	Gate-body leakage current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.5	3.5	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 60\text{ A}$		2.1	2.3	m Ω

1. Defined by design, not subject to production test.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	12800	-	pF
C_{oss}	Output capacitance		-	3500	-	pF
C_{rss}	Reverse transfer capacitance		-	170	-	pF
Q_g	Total gate charge	$V_{DD} = 50\text{ V}$, $I_D = 180\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	180	-	nC
Q_{gs}	Gate-source charge		-	78	-	nC
Q_{gd}	Gate-drain charge		-	34	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\text{ V}$, $I_D = 90\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	62	-	ns
t_r	Rise time		-	108	-	ns
$t_{d(off)}$	Turn-off delay time		-	148	-	ns
t_f	Fall time		-	40	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		180	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		720	A
$V_{SD}^{(2)}$	Source-drain current	$I_{SD} = 60\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 180\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	85		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 80\text{ V}$, $T_J = 150\text{ }^{\circ}\text{C}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	200		nC
I_{RRM}	Reverse recovery current		-	4.7		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

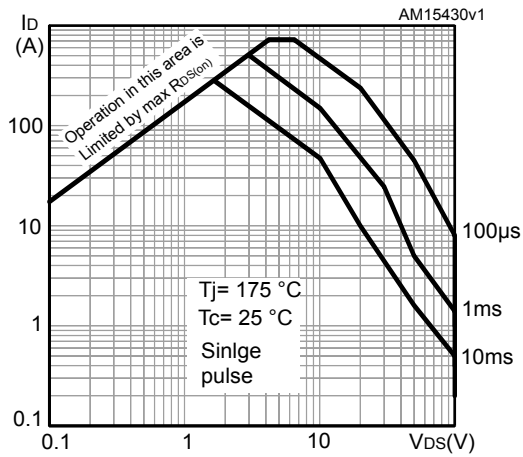


Figure 2. Thermal impedance

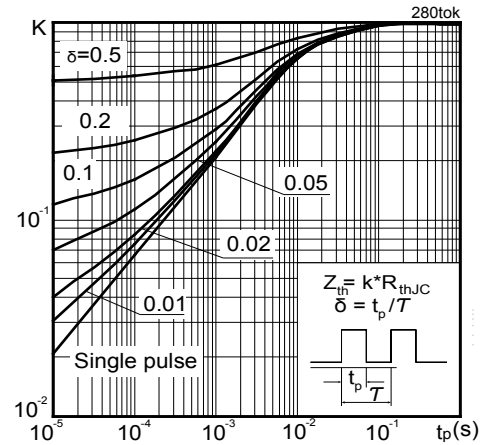


Figure 3. Output characteristics

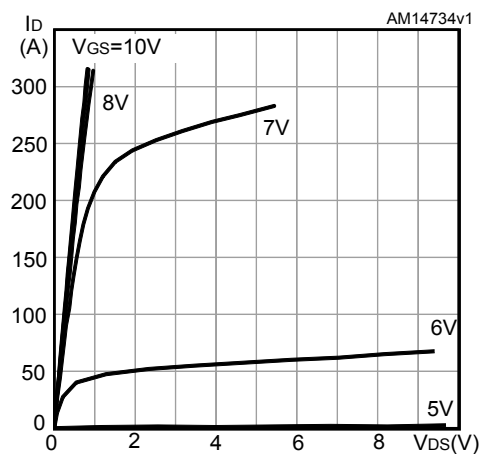


Figure 4. Transfer characteristics

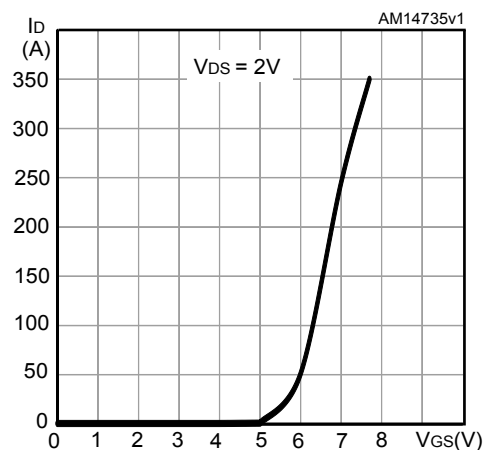


Figure 5. Gate charge vs gate-source voltage

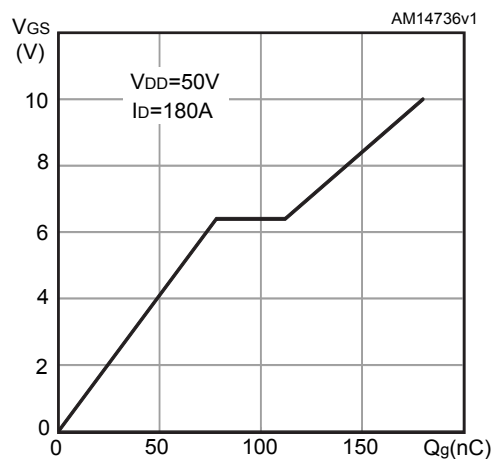


Figure 6. Static drain-source on-resistance

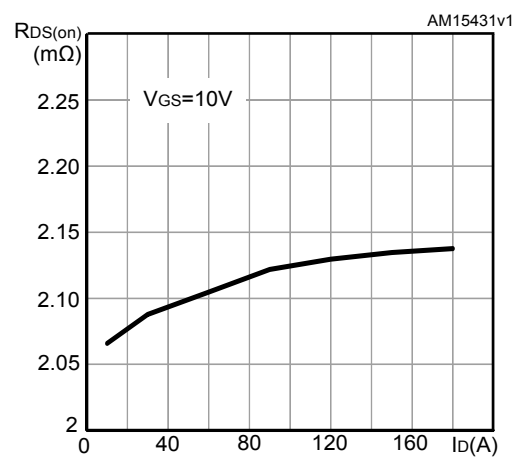


Figure 7. Normalized $V_{(BR)DSS}$ vs temperature

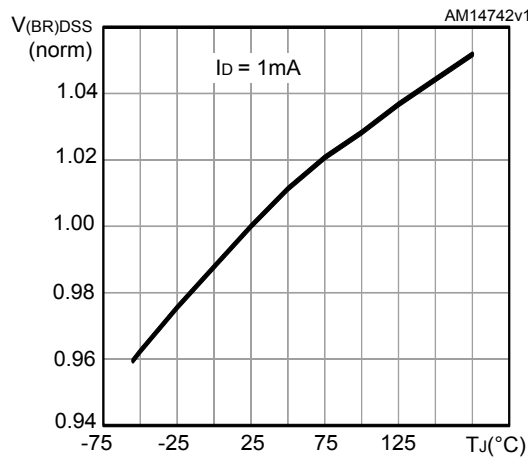


Figure 8. Capacitance variations

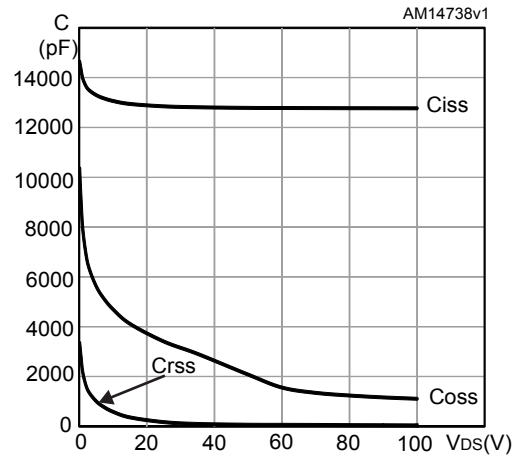


Figure 9. Source-drain diode forward characteristics

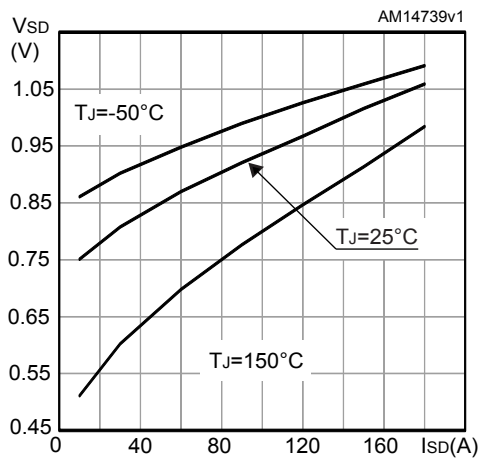


Figure 10. Normalized gate threshold voltage vs temperature

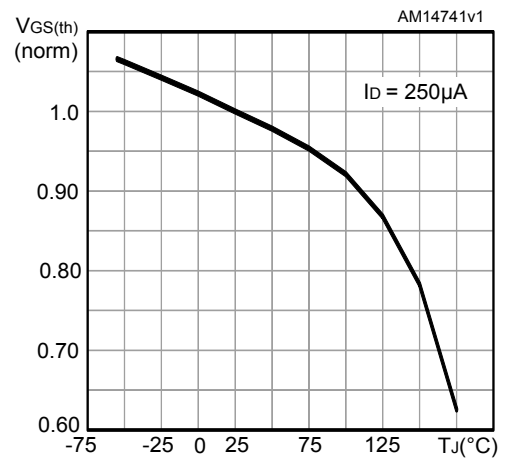
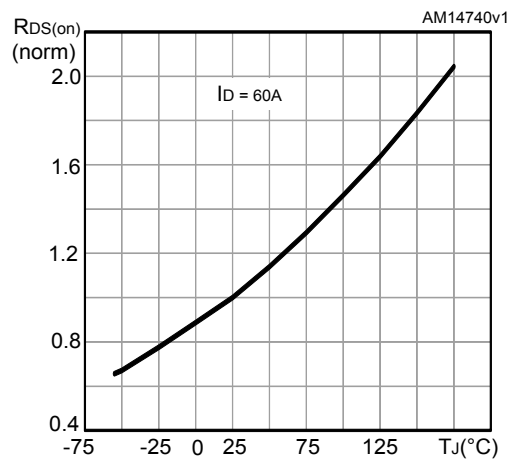
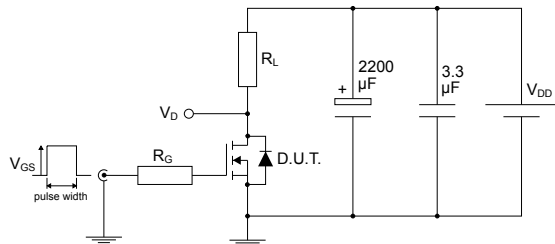


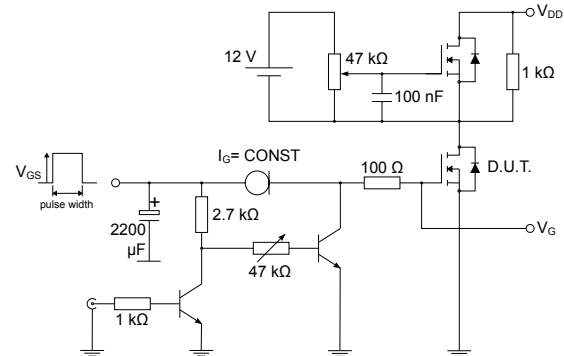
Figure 11. Normalized on-resistance vs temperature



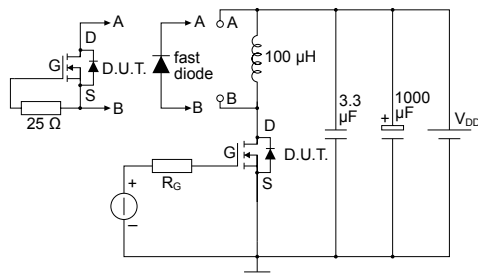
3 Test circuits

Figure 12. Test circuit for resistive load switching times


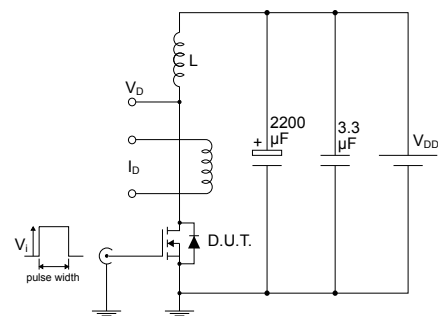
AM01468v1

Figure 13. Test circuit for gate charge behavior


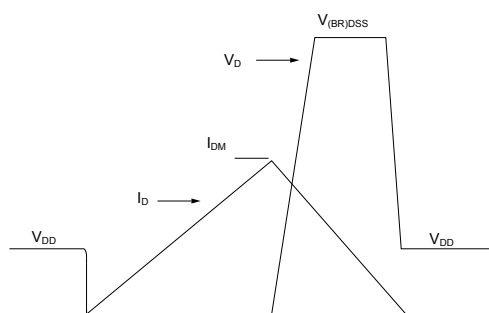
AM01469v1

Figure 14. Test circuit for inductive load switching and diode recovery times


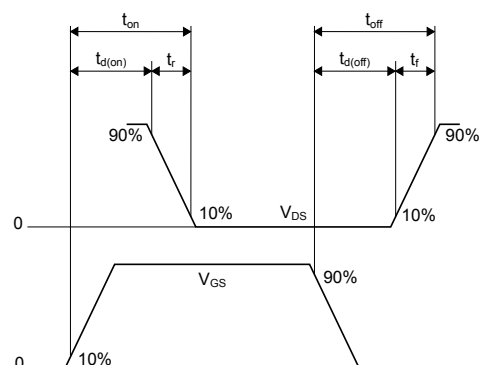
AM01470v1

Figure 15. Unclamped inductive load test circuit


AM01471v1

Figure 16. Unclamped inductive waveform


AM01472v1

Figure 17. Switching time waveform


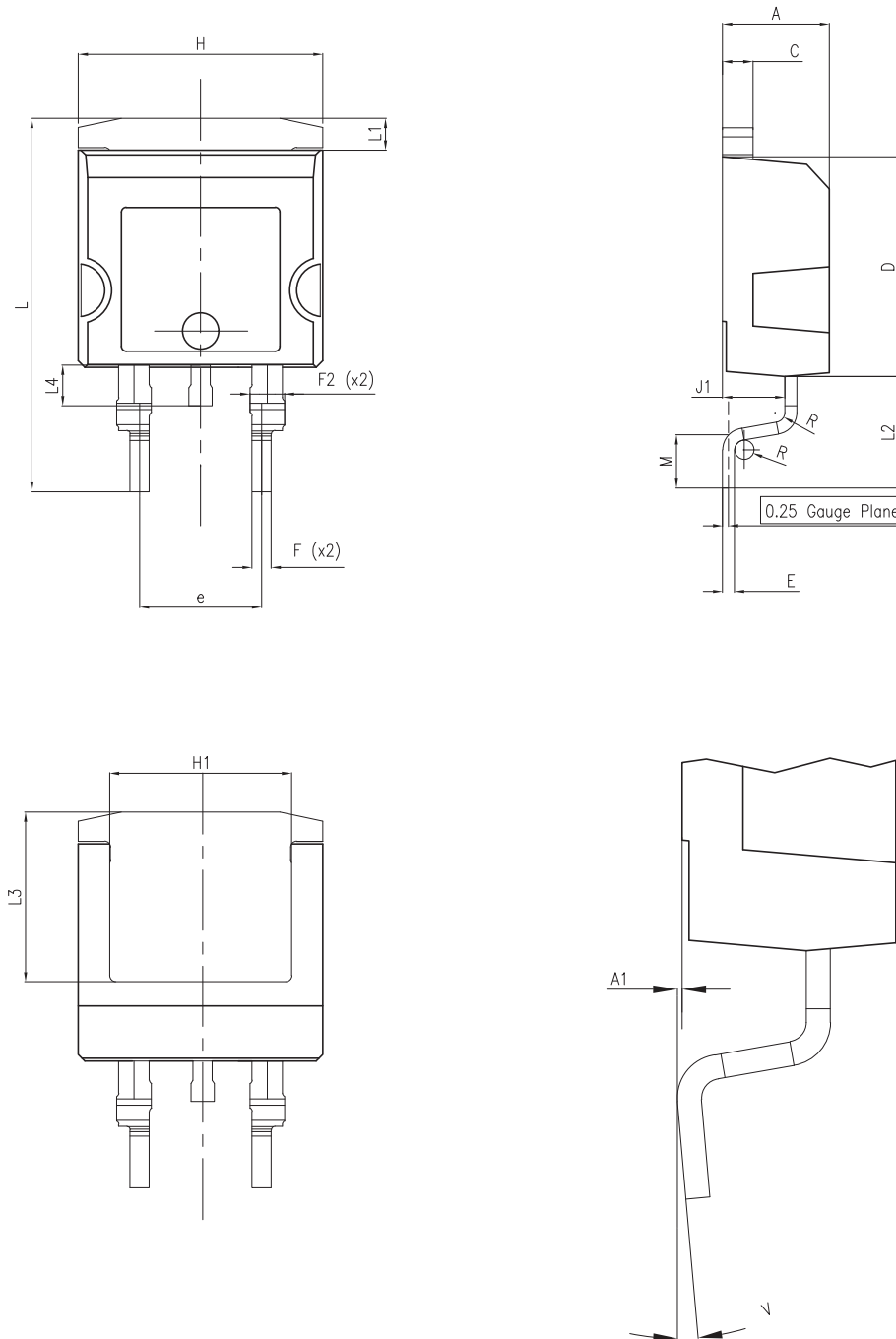
AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 H²PAK-2 package information

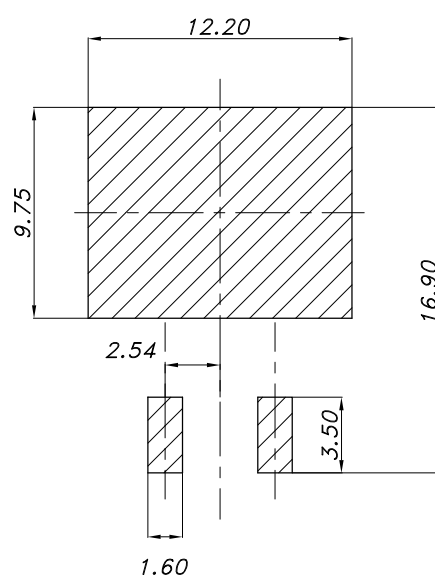
Figure 18. H²PAK-2 package outline



8159712_10

Table 7. H²PAK-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.70
A1	0.03		0.20
C	1.17		1.37
D	8.95		9.35
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
F2	1.14		1.70
H	10.00		10.40
H1	7.40		7.80
J1	2.49		2.69
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.50		1.70
M	2.60		2.90
R	0.20		0.60
V	0°		8°

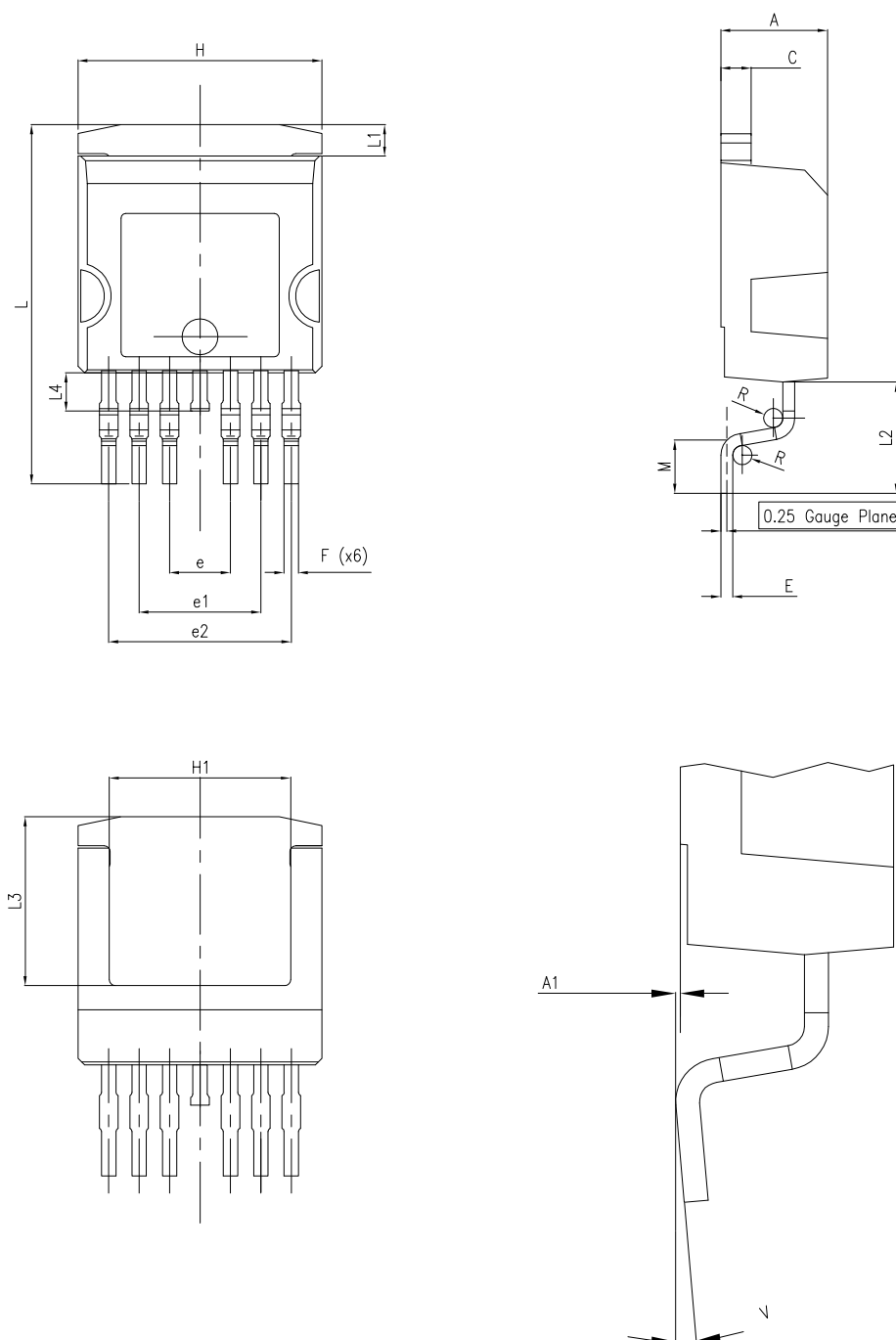
Figure 19. H²PAK-2 recommended footprint


8159712_10

Note: Dimensions are in mm.

4.2 H²PAK-6 package information

Figure 20. H²PAK-6 package outline

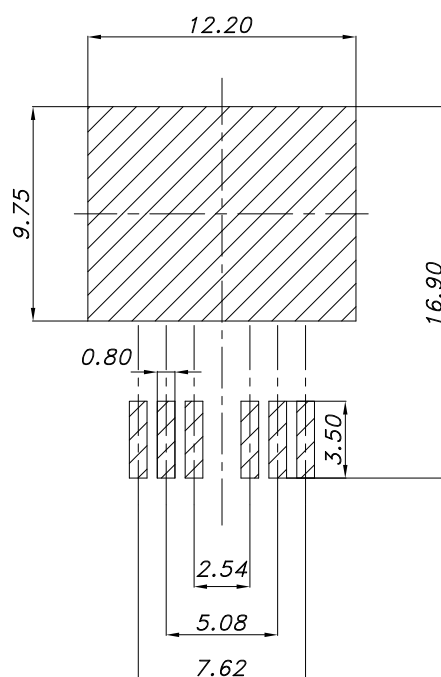


8159693_Rev_9

Table 8. H²PAK-6 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.70
A1	0.03		0.20

Dim.	mm		
	Min.	Typ.	Max.
C	1.17		1.37
e	2.34	2.54	2.74
e1	4.88		5.28
e2	7.42		7.82
E	0.45		0.60
F	0.50		0.70
H	10.00		10.40
H1	7.40		7.80
L	14.75		15.25
L1	1.27		1.40
L2	4.35		4.95
L3	6.85		7.25
L4	1.50		1.75
M	1.90		2.50
R	0.20		0.60
V	0°		8°

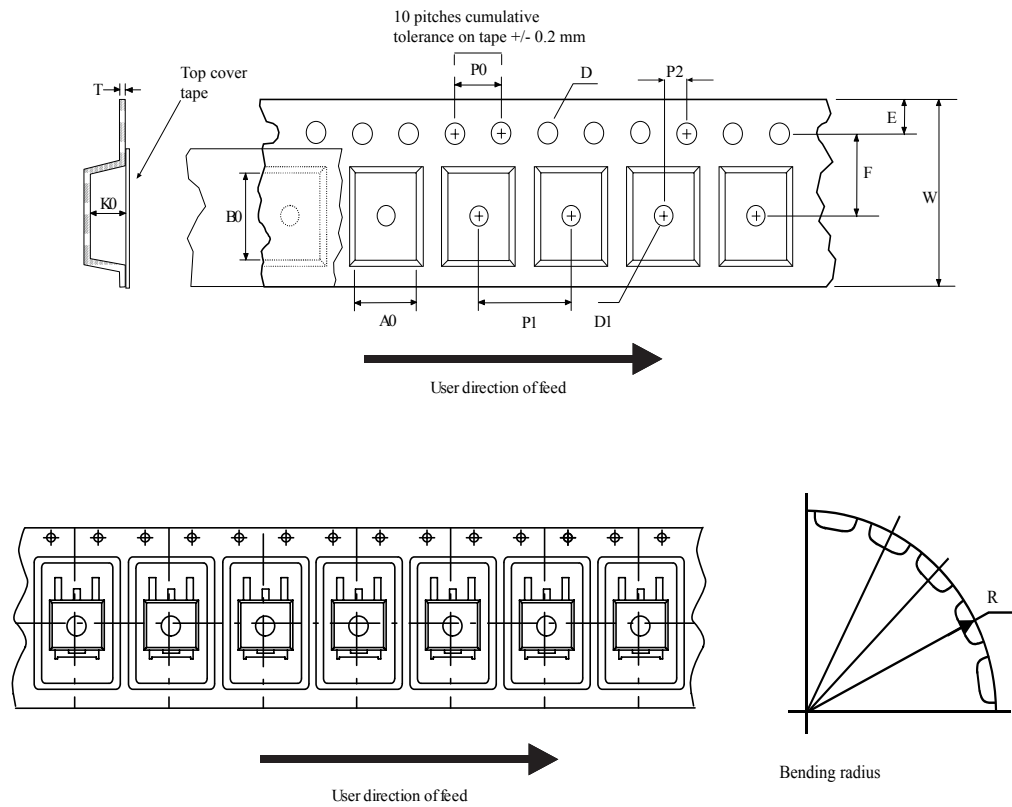
Figure 21. H²PAK-6 recommended footprint


8159693_footprint_Rev_9

Note: *Dimensions are in mm.*

4.3 Packing information

Figure 22. Tape outline



AM08852v2

Figure 23. Reel outline

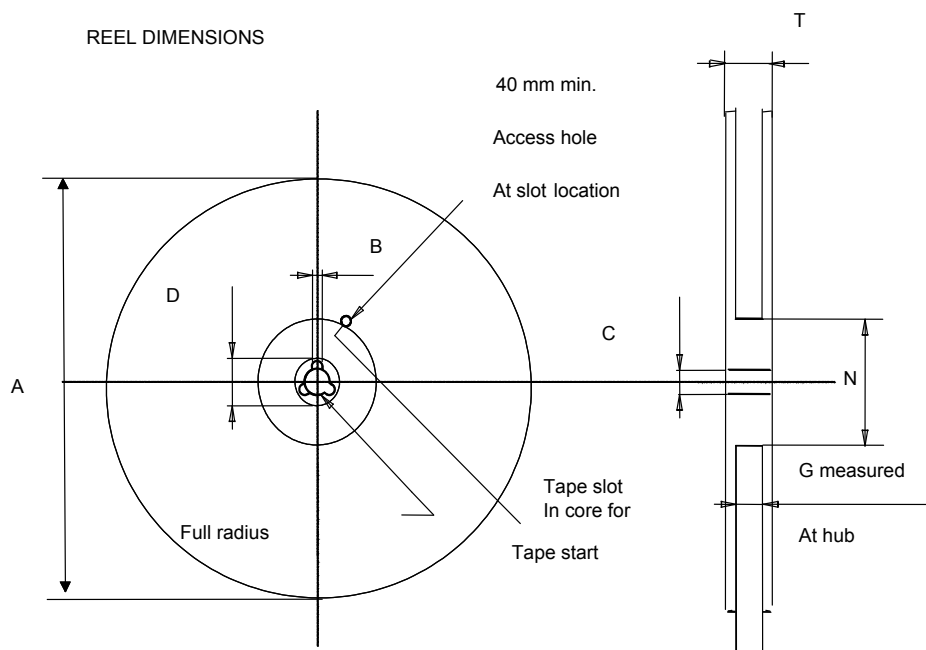


Table 9. Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.30	0.40			
W	23.7	24.3			

Revision history

Table 10. Document revision history

Date	Version	Changes
02-Aug-2013	1	Initial release.
03-Sep-2013	2	– Modified: <i>Table 1</i> , RDS(on) typical value in <i>Table 4</i> – Minor text changes
27-May-2014	3	– Modified: title and <i>Features</i> in cover page – Updated: <i>Section 4: Package mechanical data</i> – Minor text changes
12-Sep-2014	4	– Modified: title, features and description in cover page.
03-May-2021	5	Updated <i>Table 1. Absolute maximum ratings</i> . Minor text changes.
28-Mar-2025	6	Updated Table 9. Tape and reel mechanical data .

Contents

1	Electrical ratings	2
2	Electrical characteristics.....	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	7
4	Package information.....	8
4.1	H ² PAK-2 package information	8
4.2	H ² PAK-6 package information	10
4.3	Packing information	12
	Revision history	14

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