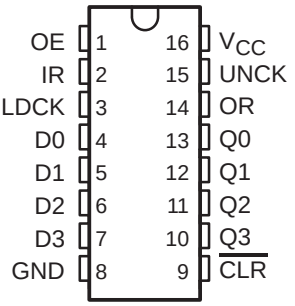
- **Independent Synchronous Inputs and Outputs**
- **16 Words by 4 Bits Each**
- **3-State Outputs Drive Bus Lines Directly**
- **Data Rates up to 10 MHz**
- **Fall-Through Time 50 ns Typical**
- **Data Terminals Arranged for Printed Circuit Board Layout**
- **Expandable Using External Gating**
- **Packaged in Standard Plastic 300-mil DIPs**

N PACKAGE
(TOP VIEW)



description

The SN74LS224A 64-bit, low-power Schottky memory is organized as 16 words by 4 bits each. It can be expanded in multiples of 15m + 1 words or 4n bits, or both (where n is the number of packages in the vertical array and m is the number of packages in the horizontal array); however, some external gating is required. For longer words, the input ready (IR) signals of the first-rank packages and output ready (OR) signals of the last-rank packages must be ANDed for proper synchronization.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written to and read from its array at independent data rates. These FIFOs are designed to process data at rates up to 10 MHz in a bit-parallel format, word by word.

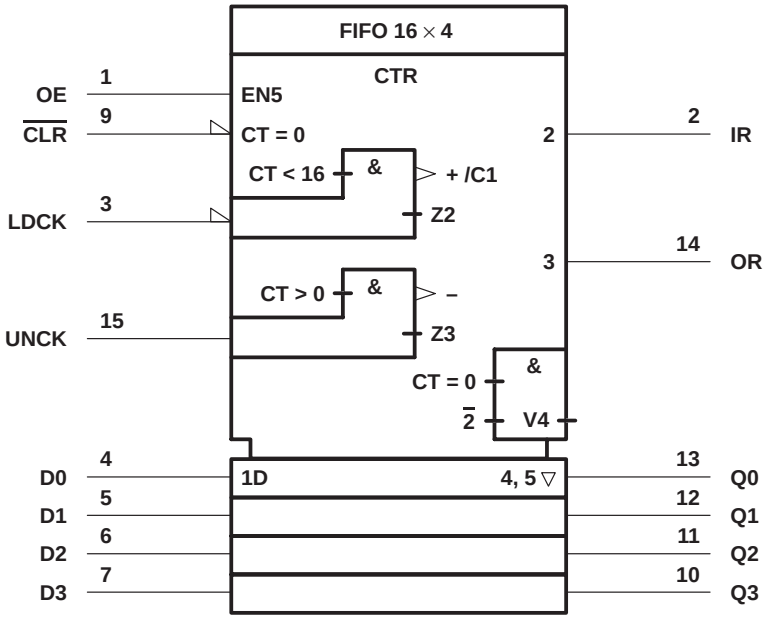
The load clock (LDCK) normally is held low, and data is written into memory on the high-to-low transition of LDCK. The unload clock (UNCK) normally is held high, and data is read out on the low-to-high transition of UNCK. The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the IR and OR flags that indicate not-full and not-empty conditions. IR is high only when the memory is not full and LDCK is low. OR is high only when the memory is not empty and UNCK is high.

A low level on the clear ($\overline{\text{CLR}}$) input resets the internal stack-control pointers and also sets IR high and OR low to indicate that old data remaining at the data outputs is invalid. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable (OE) input is low. OE does not affect the IR and OR outputs.

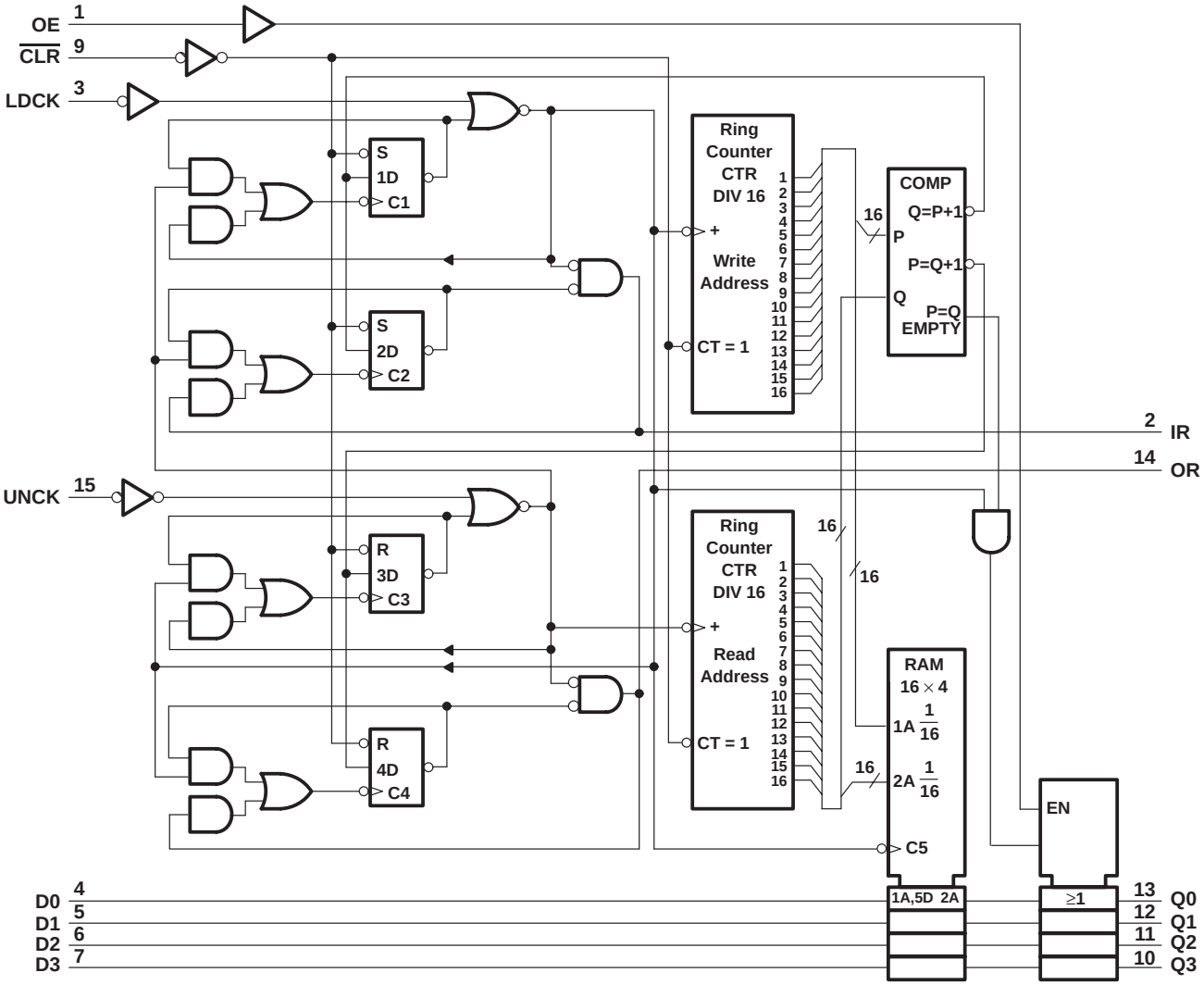
The SN74LS224A is characterized for operation from 0°C to 70°C.

logic symbol†

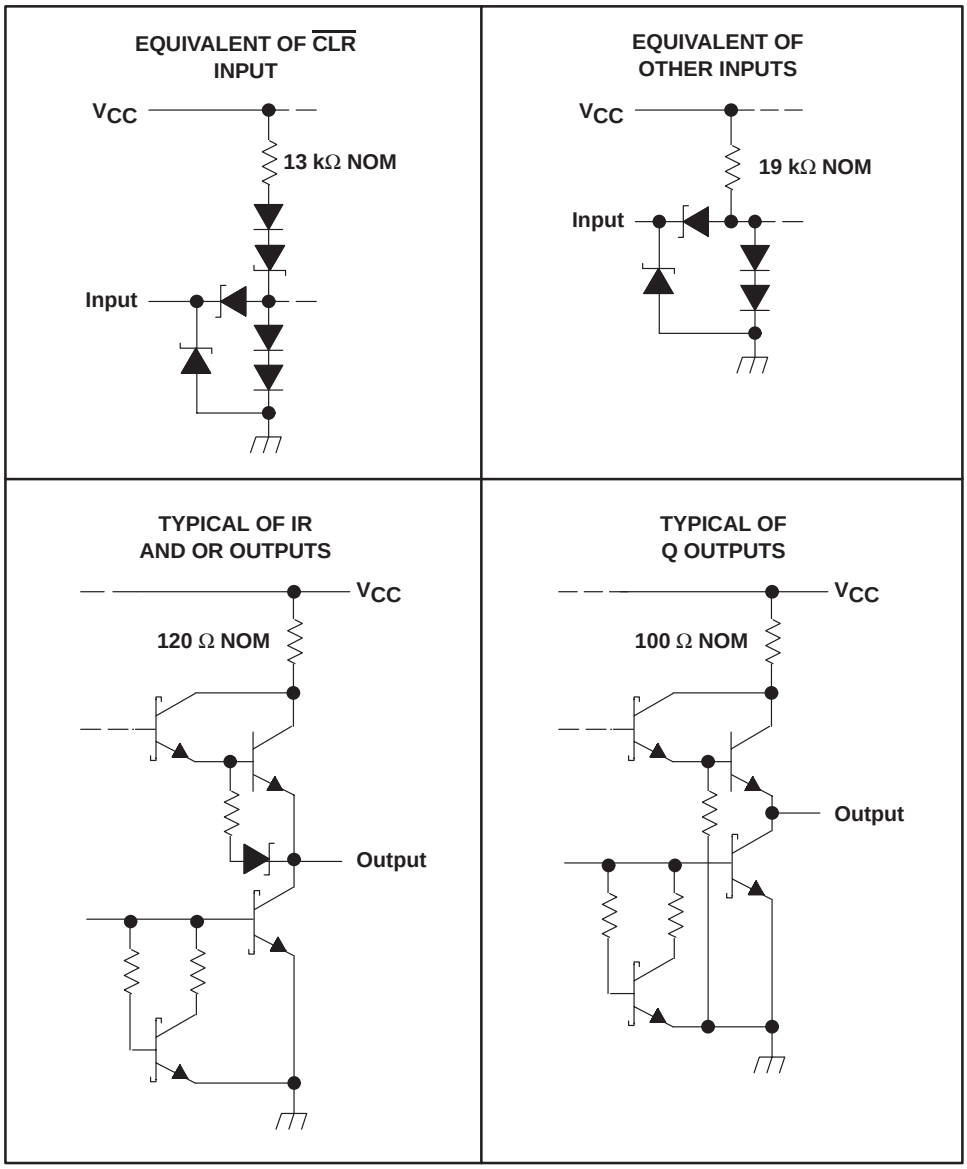


† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. This symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

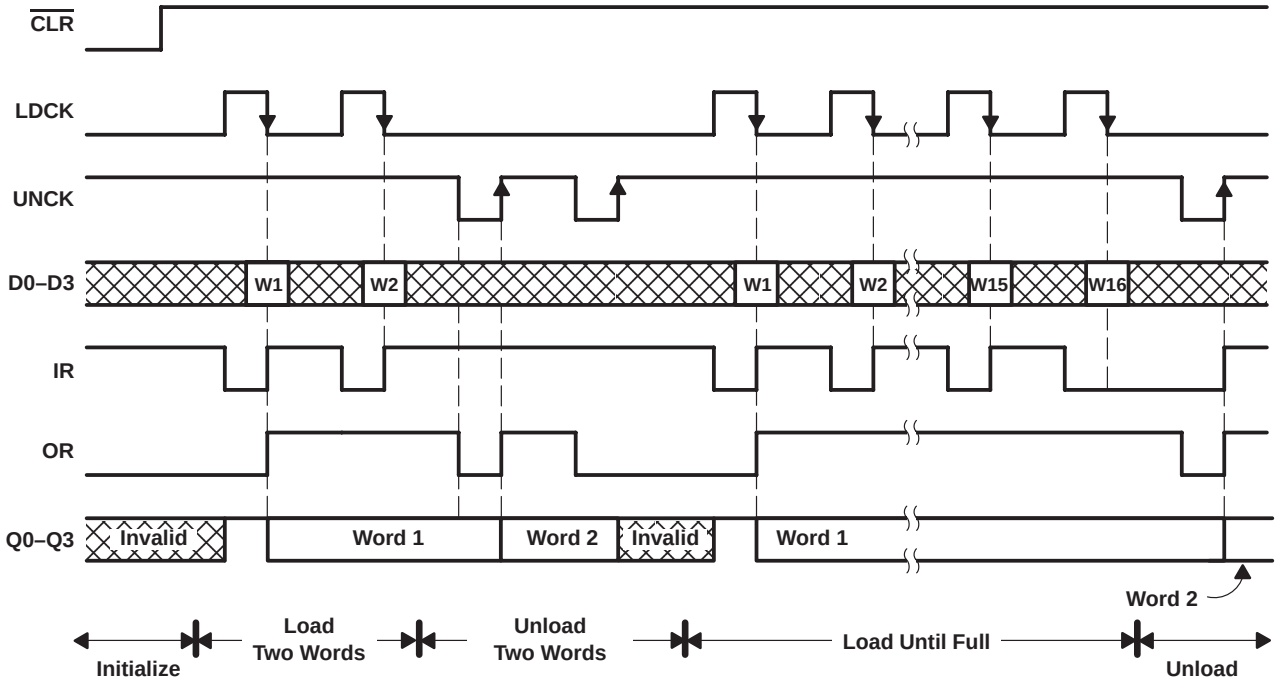
logic diagram (positive logic)



schematics of inputs and outputs



timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range, V_I . . . . . –0.5 V to 7 V
Off-state output voltage range, V_O . . . . . –0.5 V to 5.5 V
Package thermal impedance, θ_{JA} (see Note 2) . . . . . 78°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			–2.6	mA
		IR, OR			–0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		IR, OR			8	
T_A	Operating free-air temperature		0		70	°C

NOTE 3: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the V_{IL}, V_{IH}, or minimum pulse-duration limits can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA			–1.5	V
V_{OH}	Q outputs	V_{CC} = 4.75 V,	I_{OH} = –2.6 mA	2.4	3.4		V
	IR, OR	V_{CC} = 4.75 V,	I_{OH} = –0.4 mA	2.7	3.4		
V_{OL}	Q outputs	V_{CC} = 4.75 V	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
	IR, OR	V_{CC} = 4.75 V	I_{OL} = 4 mA		0.25	0.4	
			I_{OL} = 8 mA		0.35	0.5	
I_{OZH}	Q outputs	V_{CC} = 5.25 V,	V_O = 2.7 V			20	µA
I_{OZL}	Q outputs	V_{CC} = 5.25 V,	V_O = 0.4 V			–20	µA
I_I		V_{CC} = 5.25 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.25 V,	V_I = 2.7 V			20	µA
I_{IL}		V_{CC} = 5.25 V,	V_I = 0.4 V			–0.4	mA
I_{OS}‡	Q outputs	V_{CC} = 5.25 V		–30		–130	mA
	IR, OR			–20		–100	
I_{CC}		V_{CC} = 5.25 V	Outputs high		84	135	mA
			Outputs low		87	155	
			Outputs disabled		89	155	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

timing requirements over recommended operating conditions (see Note 3 and Figure 1)

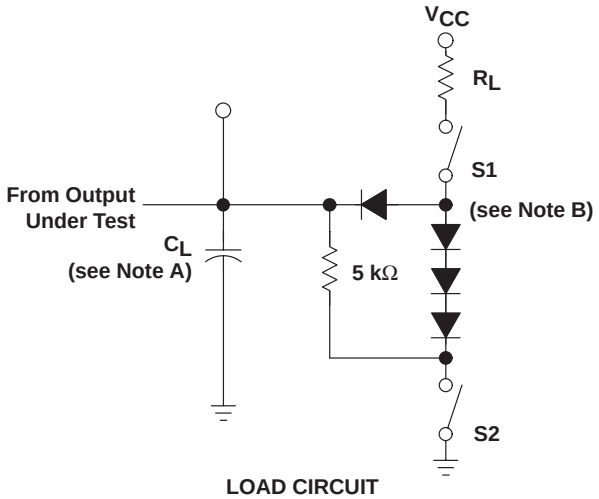
			MIN	NOM	MAX	UNIT
t_w	Pulse duration	LDCK high	60			ns
		LDCK low	15			
		UNCK low	30			
		UNCK high	30			
		$\overline{CLR}$ low	20			
t_{su}	Setup time	Data to LDCK↓	50			ns
		LDCK↓ before UNCK↓	50			
		UNCK↑ before LDCK↑	50			
t_h	Hold time	Data from LDCK↓	10			ns

NOTE 3: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the V_{IL}, V_{IH}, or minimum pulse-duration limits can cause a false clock or improper operation of the internal read and write pointers.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

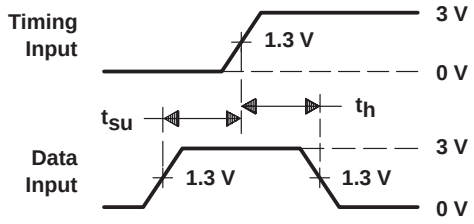
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TYP	MAX	UNIT
t_{PLH}	IRE↑	IR	R_L = 2 kΩ, C_L = 15 pF	N/A	N/A	ns
t_{PHL}	IRE↓			N/A	N/A	
t_{PLH}	ORE↑	OR	R_L = 2 kΩ, C_L = 15 pF	N/A	N/A	ns
t_{PHL}	ORE↓			N/A	N/A	
t_{PLH}	LDCK↓	IR	R_L = 2 kΩ, C_L = 15 pF	25	40	ns
t_{PHL}	LDCK↑			36	50	
t_{PLH}	LDCK↓	OR	R_L = 2 kΩ, C_L = 15 pF	48	70	ns
t_{PLH}	UNCK↑	OR	R_L = 2 kΩ, C_L = 15 pF	29	45	ns
t_{PHL}	UNCK↓			28	45	
t_{PLH}	UNCK↑	IR	R_L = 2 kΩ, C_L = 15 pF	49	70	ns
t_{PLH}	$\overline{CLR}$↓	IR	R_L = 2 kΩ, C_L = 15 pF	36	55	ns
t_{PHL}		OR		25	40	
t_{PHL}	LDCK↓	Q	R_L = 667 Ω, C_L = 45 pF	34	50	ns
t_{PLH}	UNCK↑	Q	R_L = 667 Ω, C_L = 45 pF	54	80	ns
t_{PHL}				45	70	
t_{PZL}	OE↑	Q	R_L = 667 Ω, C_L = 45 pF	22	35	ns
t_{PZH}				21	35	
t_{PLZ}	OE↓	Q	R_L = 667 Ω, C_L = 5 pF	16	30	ns
t_{PHZ}				18	30	ns

PARAMETER MEASUREMENT INFORMATION

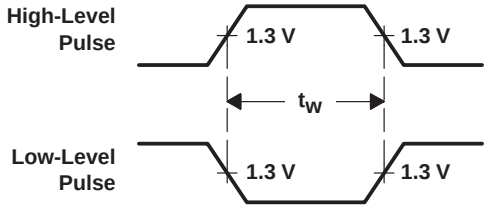


LOAD CIRCUIT

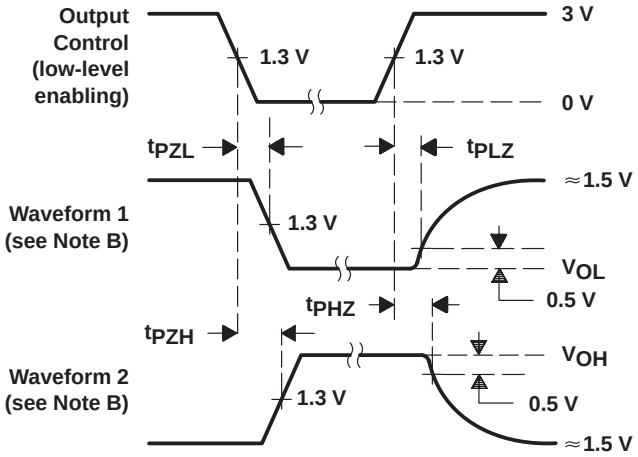
TEST	S1	S2
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed
t_{PLZ}/t_{PHZ}	Closed	Closed
t_{PLH}/t_{PHL}	Closed	Closed



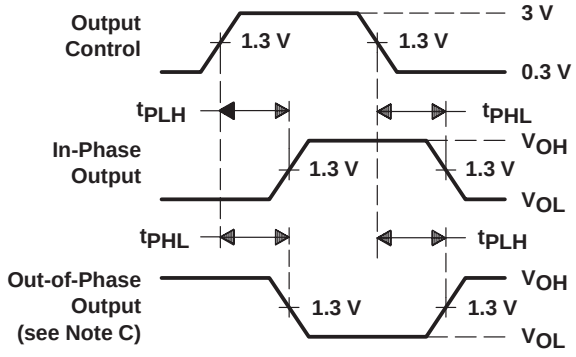
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, t_r < 15 ns, t_f < 6 ns, Z_O ≈ 50 Ω.
D. All diodes are 1N916 or 1N3064.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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