

TinyLogic UHS Dual 2-Input NAND Gate

NC7WZ00

Description

The NC7WZ00 is a dual 2-Input NAND Gate from onsemi's Ultra High Speed Series of TinyLogic. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V V_{CC} operating range. The inputs and output are high impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 5.5 V independent of V_{CC} operating voltage.

Features

- Space Saving US8 Surface Mount Package
- MicroPak™ Leadless Package
- Ultra High Speed: t_{PD} 2.4 ns Typ. into 50 pF at 5 V V_{CC}
- High Output Drive: ± 24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V – 5.5 V
- Matches the Performance of LCX when Operated at 3.3 V V_{CC}
- Power Down High Impedance Inputs / Output
- Overvoltage Tolerant Inputs Facilitate 5 V to 3 V Translation
- Proprietary Noise / EMI Reduction Circuitry Implemented
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

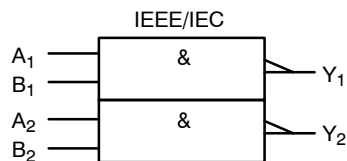
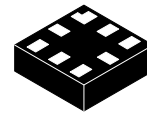
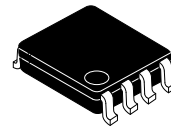


Figure 1. Logic Symbol

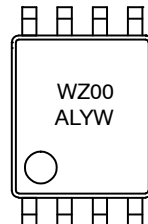
MARKING DIAGRAMS



UQFN8
1.6X1.6, 0.5P
CASE 523AY



US8
CASE 846AN



N6, WZ00 = Specific Device Code
 KK = 2-Digit Lot Run Traceability Code
 XY = 2-Digit Date Code Format
 Z = Assembly Plant Code
 A = Assembly Site
 L = Wafer Lot Number
 YW = Assembly Start Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

Pin Configurations

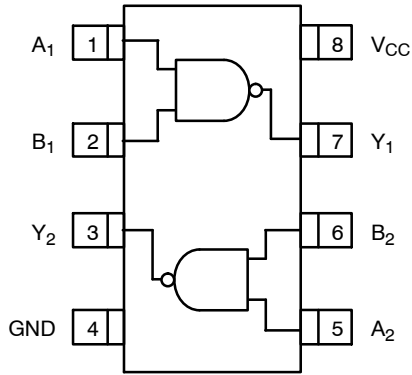


Figure 2. Connection Diagram (Top View)

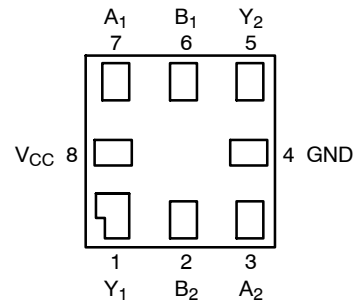
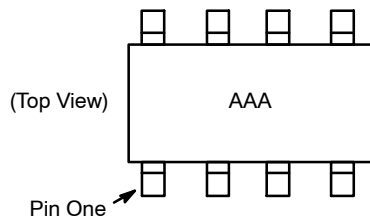


Figure 4. Pad Assignments for MicroPak (Top Thru View)



AAA represents Product Code Top Mark – see ordering code
 NOTE: Orientation of Top Mark determines Pin One location.
 Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Figure 3. Pin One Orientation Diagram

PIN DESCRIPTION

Pin Names	Description
A_n, B_n	Inputs
Y_n	Output

FUNCTION TABLE ($Y = \overline{AB}$)

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
 L = LOW Logic Level

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V _{CC}	Supply Voltage		-0.5	6.5	V
V _{IN}	DC Input Voltage		-0.5	6.5	V
V _{OUT}	DC Output Voltage		-0.5	6.5	V
I _{IK}	DC Input Diode Current	V _{IN} < 0 V	-	-50	mA
I _{OK}	DC Output Diode Current	V _{OUT} < 0 V	-	-50	mA
I _{OUT}	DC Output Current		-	±50	mA
I _{CC} / I _{GND}	DC V _{CC} / GND Current		-	±100	mA
T _{STG}	Storage Temperature		-65	+150	°C
T _J	Junction Temperature Under Bias		-	150	°C
T _L	Junction Lead Temperature (Soldering, 10 Seconds)		-	260	°C
P _D	Power Dissipation in Still Air		-	500	mW
			-	539	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V _{CC}	Supply Voltage Operating		1.65	5.5	V
	Supply Voltage Data Retention		1.5	5.5	
V _{IN}	Input Voltage		0	5.5	V
V _{OUT}	Output Voltage		0	V _{CC}	V
T _A	Operating Temperature		-40	+85	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} = 1.65 V ±0.15 V, 2.5 V ±0.2 V	0	20	ns/V
		V _{CC} = 3.3 V ±0.3 V	0	10	
		V _{CC} = 5.0 V ±0.5 V	0	5	
θ _{JA}	Thermal Resistance		-	250	°C/W
			-	232	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTRICAL CHARACTERISTICS

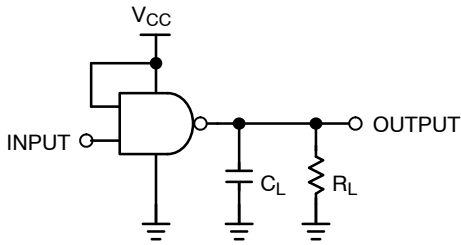
Symbol	Parameter	V _{CC} (V)	Conditions		T _A = +25°C			T _A = −40 to +85°C		Unit
					Min	Typ	Max	Min	Max	
V _{IH}	HIGH Level Input Voltage	1.65 – 1.95			0.65 V _{CC}	–	–	0.65 V _{CC}	–	V
		2.3 – 5.5			0.70 V _{CC}	–	–	0.70 V _{CC}	–	
V _{IL}	LOW Level Input Voltage	1.65 – 1.95			–	–	0.35 V _{CC}	–	0.35 V _{CC}	V
		2.3 – 5.5			–	–	0.30 V _{CC}	–	0.30 V _{CC}	
V _{OH}	HIGH Level Output Voltage	1.65	V _{IN} = V _{IL}	I _{OH} = −100 μA	1.55	1.65	–	1.55	–	V
		2.3			2.2	2.3	–	2.2	–	
		3.0			2.9	3.0	–	2.9	–	
		4.5			4.4	4.5	–	4.4	–	
		1.65		I _{OH} = −4 mA	1.29	1.52	–	1.69	–	
		2.3		I _{OH} = −8 mA	1.9	2.15	–	1.9	–	
		3.0		I _{OH} = −16 mA	2.4	2.80	–	2.4	–	
		3.0		I _{OH} = −24 mA	2.3	2.68	–	2.3	–	
		4.5		I _{OH} = −32 mA	3.8	4.20	–	3.8	–	
V _{OL}	LOW Level Output Voltage	1.65	V _{IN} = V _{IH}	I _{OL} = 100 μA	–	0.0	0.1	–	0.1	V
		2.3			–	0.0	0.1	–	0.1	
		3.0			–	0.0	0.1	–	0.1	
		4.5			–	0.0	0.1	–	0.1	
		1.65		I _{OL} = 4 mA	–	0.08	0.24	–	0.24	
		2.3		I _{OL} = 8 mA	–	0.10	0.3	–	0.3	
		3.0		I _{OL} = 16 mA	–	0.15	0.4	–	0.4	
		3.0		I _{OL} = 24 mA	–	0.22	0.55	–	0.55	
		4.5		I _{OL} = 32 mA	–	0.22	0.55	–	0.55	
I _{IN}	Input Leakage Current	1.65 – 5.5	V _{IN} = 5.5 V, GND		–	–	±0.1	–	±1	μA
I _{OFF}	Power Off Leakage Current	0.0	V _{IN} or V _{OUT} = 5.5 V		–	–	1	–	10	μA
I _{CC}	Quiescent Supply Current	1.65 – 5.5	V _{IN} = 5.5 V, GND		–	–	1	–	10	μA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C			T _A = -40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay (Figure 5, 7)	1.8 ±0.15	C _L = 15 pF, R _L = 1 MΩ,	–	5.3	9.6	–	9.8	ns
		2.5 ±0.2		–	3.2	5.3	–	5.7	
		3.3 ±0.3		–	2.4	3.7	–	4.0	
		5.0 ±0.5		–	1.9	2.9	–	3.2	
		3.3 ±0.3	C _L = 50 pF, R _L = 500 Ω,	–	3.0	4.6	–	4.9	
		5.0 ±0.5		–	2.4	3.6	–	3.9	
C _{IN}	Input Capacitance	0		–	2.5	–	–	–	pF
C _{PD}	Power Dissipation Capacitance (Figure 6)	3.3	(Note 2)	–	13	–	–	–	pF
		5.0		–	17	–	–	–	

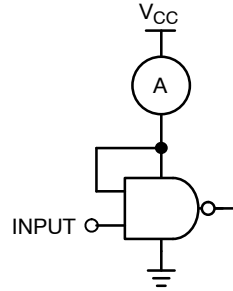
2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (see Figure 6) C_{PD} is related to I_{CCD} dynamic operating current by the expression:
I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CCstatic}).

AC Loading and Waveforms



C_L includes load and stray capacitance
Input PRR = 1.0 MHz, t_W = 500 ns

Figure 5. AC Test Circuit



Input = AC Waveform; t_r = t_f = 1.8 ns;
PRR = 10 MHz; Duty Cycle = 50%.

Figure 6. I_{CCD} Test Circuit

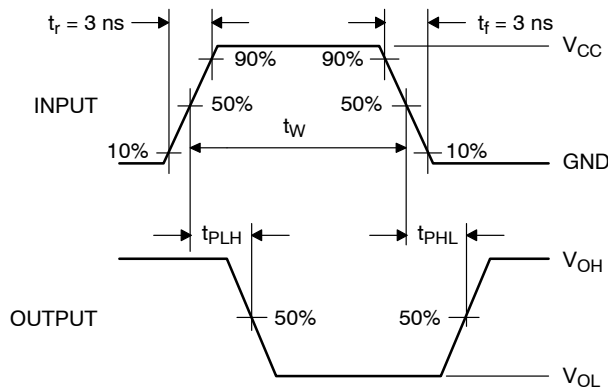


Figure 7. AC Waveforms

NC7WZ00

ORDERING INFORMATION

Order Number	Top Mark	Package	Shipping [†]
NC7WZ00K8X	WZ00	8-Lead US8, JEDEC MO-187, Variation CA 3.1 mm Wide	3000 / Tape & Reel
NC7WZ00L8X	N6	8-Lead MicroPak, 1.6 mm Wide	5000 / Tape & Reel

DISCONTINUED (Note 4)

NC7WZ00K8X-L22236	WZ00	8-Lead US8, JEDEC MO-187, Variation CA 3.1 mm Wide	3000 / Tape & Reel
NC7WZ00L8X-L22185	N6	8-Lead MicroPak, 1.6 mm Wide	5000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

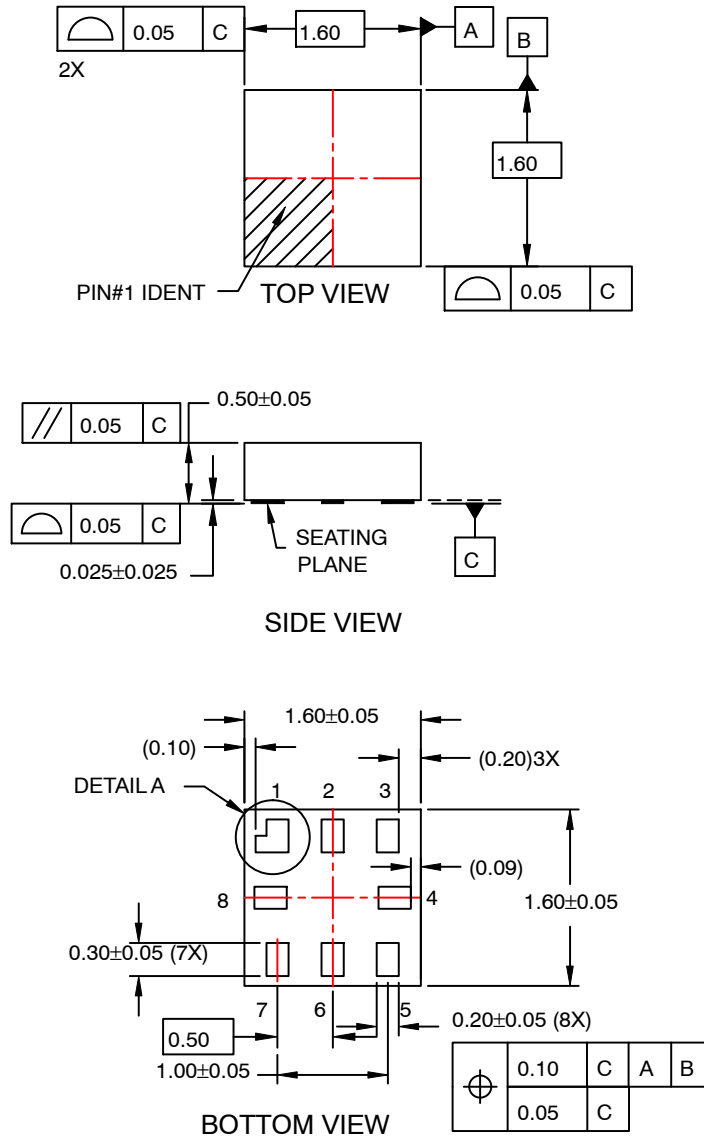
3. All packages are lead free per JEDEC: J-STD-020B standard.

4. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

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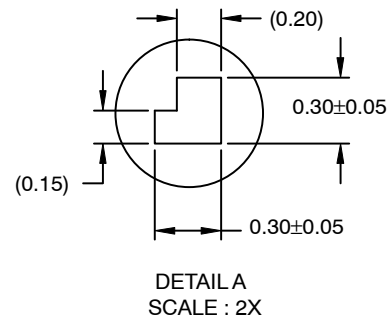
UQFN8 1.6X1.6, 0.5P
CASE 523AY
ISSUE O

DATE 31 AUG 2016



NOTES:

- A. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD.
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- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
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US8
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RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL A

NOTES:

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