SIEMENS

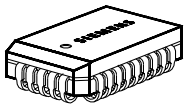
Primary Rate Interface Signaling and Maintenance Controller (PRISM)

PEB 3035

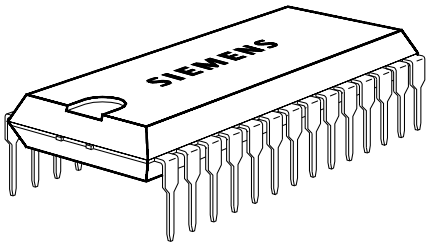
Preliminary Data

CMOS IC

Features



P-LCC-28-R



P-DIP-28

Serial Interface

- Two independent signaling/maintenance channels programmable in a
  - serial mode
  - strobe mode
  - time-slot assignment mode
- Programmable bit inversion
- Zero bit stuffing
- Programmable idle code (Flags, all ones)
- Continuous transmission of up to 32-bytes data
- Data rate up to 4 Mbit/s

Protocol Support

- Support of the ESF-DL protocol according to T1.403-1989 or according to AT & T TR 54016
- Support of HDLC protocol
- Transparent mode for totally transparent data transmission and reception

µP Interface

- 8-bit multiplexed µP-interface (SIEMENS/Intel type of µP interface)
- 64-byte FIFO per channel and direction
- Efficient transfer of data blocks from/to system memory by interrupt request

General

- P-DIP-28 or P-LCC-28-R package
- Advanced CMOS technology
- Low power consumption

Type	Version	Ordering Code	Package
PEB 3035-N	V1.1	Q67100-H6242	P-LCC-28-R (SMD)
PEB 3035-P	V1.1	Q67100-H6243	P-DIP-28

Introduction

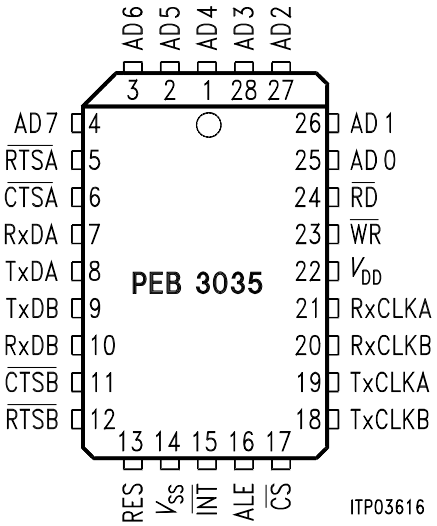
The PEB 3035 PRISM (Primary Rate Interface Signaling and Maintenance controller) is a two channel serial communication controller designed to support signaling and maintenance functions for T1 - Primary Rate Interfaces using the Extended Super Frame format ESF. The device supports the DL-channel protocol for ESF format according to T1.403-1989 ANSI specification or according to AT & T TR 54016, September 1989.

The 8-bit parallel µP interface fits perfectly into every Siemens/Intel 8-bit or 16-bit microcontroller or microprocessor system.

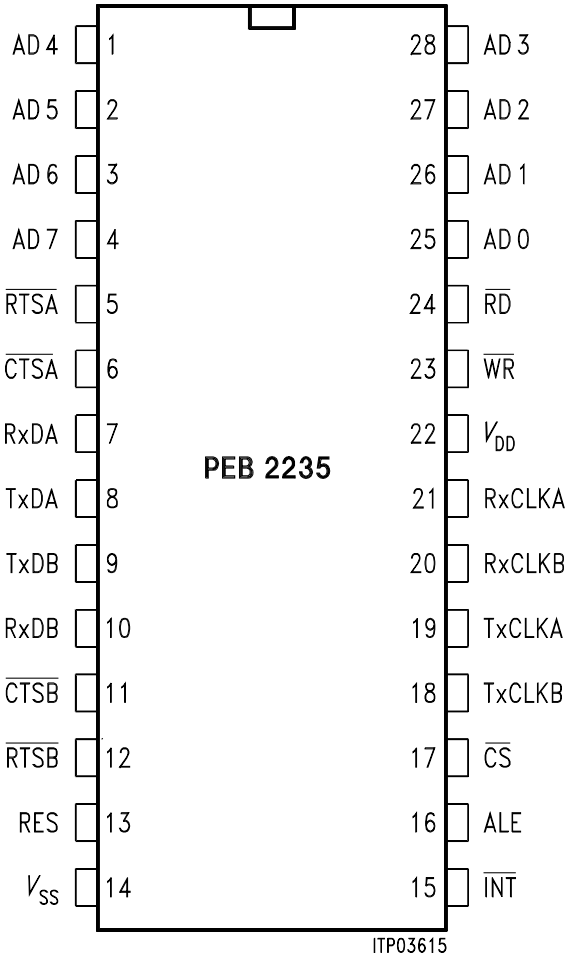
The two serial channels can be programmed in three different clock modes to function in time-slot oriented applications, in a strobe mode or as a serial interface.

Pin Configuration
(top view)

P-LCC-28-R



P-DIP-28

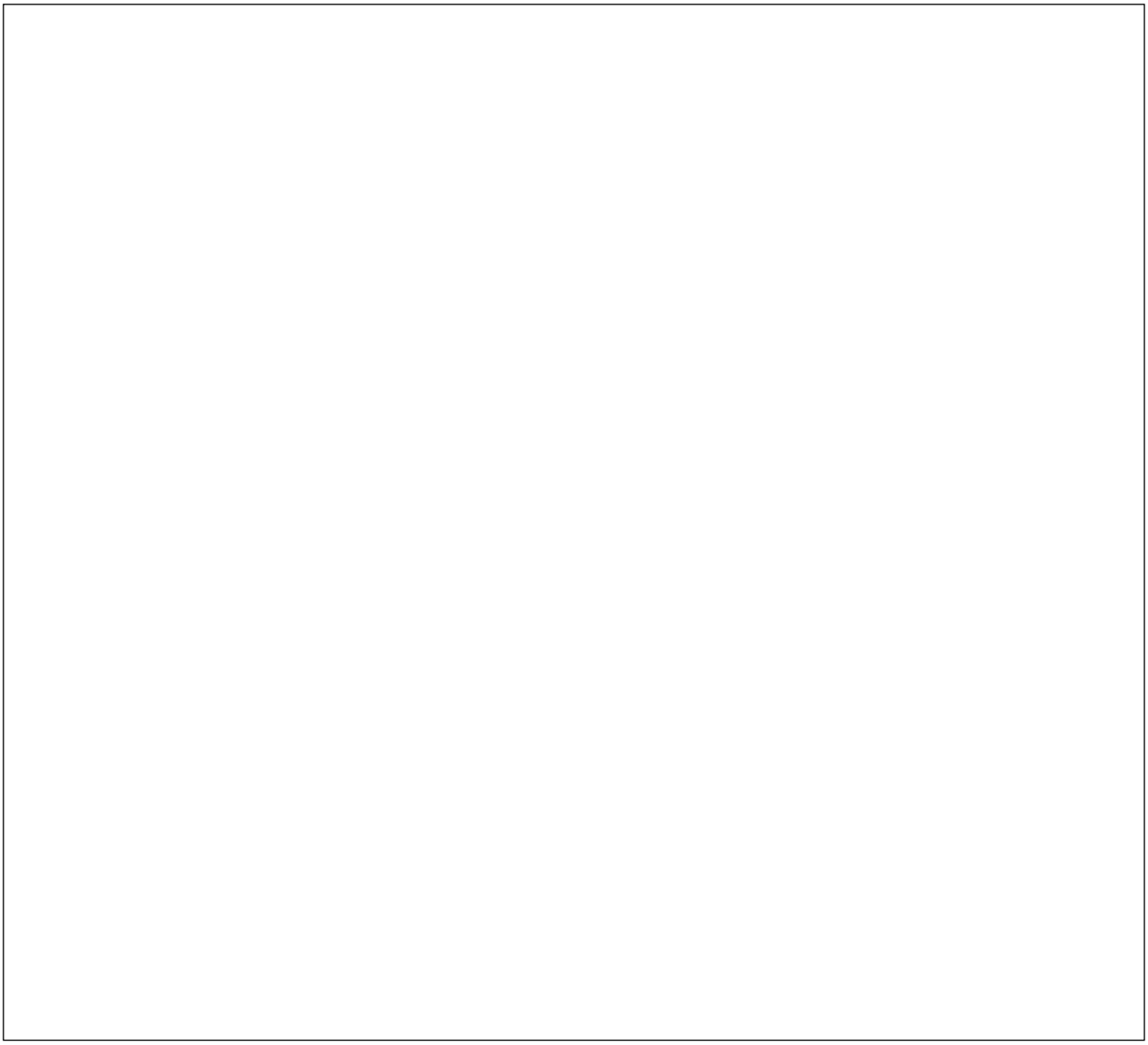


Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
25 26 27 28 1 2 3 4	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O	**Data Bus** The multiplexed address data bus transfers data and commands between the µP interface and the PRISM.
24	$\overline{RD}$	I	**Read** This signal indicates a read operation.
23	$\overline{WR}$	I	**Write** This signal indicates a write operation.
17	$\overline{CS}$	I	**Chip Select** A low on this signal selects the PRISM for a read/ write operation.
7 10	RxDA RxDB	I/O I/O	**Receive Data**, (channel A/channel B) These lines receive serial data at standard TTL or CMOS levels.
5 12	$\overline{RTSA}$ $\overline{RTSB}$	O O	**Request to Send**, (channel A/channel B) When RTS bit in MODE register is set the RTS signal goes low. When the RTS bit is reset, the signal goes high if the transmitter has finished and there is no further request for transmission.
8 9	TxDA TxDB	I/O I/O	**Transmit Data**, (channel A/channel B) These lines transmit serial data at standard TTL or CMOS levels. They can be programmed as push pull or open-drain outputs.
6 11	$\overline{CTSA}$ $\overline{CTSB}$	I I	**Clear to Send**, (channel A/channel B) A change on this input lines leads to an interrupt if enabled (CCR2; CIE, see Register Definitions).
13	RES	I	**Reset** A high on this input forces the PRISM into reset state. The PRISM is in power-up mode during reset and in power down mode after reset. The minimum pulse width is 1.8 µs.

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
16	ALE	I	**Address Latch Enable** A high on this line indicates an address on the external address/data bus.
14	V_{SS}		**Ground** (0 V)
15	$\overline{INT}$	OD	**Interrupt Request** The signal is activated when the PRISM requests an interrupt (active low). $\overline{INT}$ is an open drain output. This pin must be connected to pull-up resistor.
19 18	TxCLKA TxCLKB	I I/O	**Transmit Clock**, (channel A/channel B) These pins can be programmed in several different modes of operation. T×CLK may supply - the transmit clock for the respective channel (clock mode 0) - a transmit strobe signal (clock mode 1) - a frame sync. signal (T×CLKA, clock mode 2) Programmed as output, the T×CLKB pin supplies a tristate control signal, indicating the programmed transmit time slot (clock mode 2).
21 20	RxCLKA RxCLKB	I I	**Receive Clock**, (channel A/channel B) These pins can be programmed in several different operation modes. In each channel the R×CLK pins may supply ● the receive clock (clock mode 0) ● the receive and transmit clock (clock mode 1, 2).
22	V_{DD}	I	**Power** + 5 V power supply



Block Diagram

The PEB 3035 PRISM contains two independent, full duplex serial channels which can be used for HDLC signaling, bit oriented messages according to ANSI specification T1.403 1989 or fully transparent data communication.

The data link controller handles all functions necessary to establish and maintain an HDLC data link, such as

- Flag insertion and detection,
- Bit stuffing,
- CRC generation and checking,
- Address field recognition.

Associated with each serial channel is a set of independent command and status registers (SP-REG) and 64-byte deep FIFO's for transmit and receive direction.

Functional Description

The PEB 3035 PRISM is designed to support signaling and maintenance functions for T1 primary rate systems. The device supports the ESF-DL channel according to ANSI specification T1.403 1989 or according to AT & T TR 54016, September 1989. Two receivers are implemented in each channel which can be switched ON/OFF independently. If both receivers are activated, PRISM automatically switches between HDLC and BOM mode. The two independent channels can be programmed in three different clock modes to function in time-slot oriented applications, in a strobe mode or as serial interface.

64-byte FIFO buffers are used for the temporary storage of data packets transferred between the serial communication interface and the parallel system bus.

Note: To support the ESF-DL protocol according AT & T TR 54016, September 1989, or if the PRISM is used for HDLC format only, the BOM receiver has to be switched off. Transmission of a preamble of 32 flags before starting an HDLC frame is programmable (CCR1, see Register Definitions).

Automatic Format Switching

Characteristics: Automatic switching between message oriented HDLC and bit oriented messaging (BOM) mode, BOM and HDLC receiver switched on (MODE: HRAC, BRAC).

After reset or sw-reset (CMDR: RHR) the PRISM operates in HDLC mode. If eight or more consecutive ones are detected, the BOM mode is entered. Upon detection of a flag in the data stream, the PRISM switches back to HDLC-mode.

Note: Operating in BOM-mode, the PRISM may receive an HDLC frame immediately, i. e. without any preceding flags.

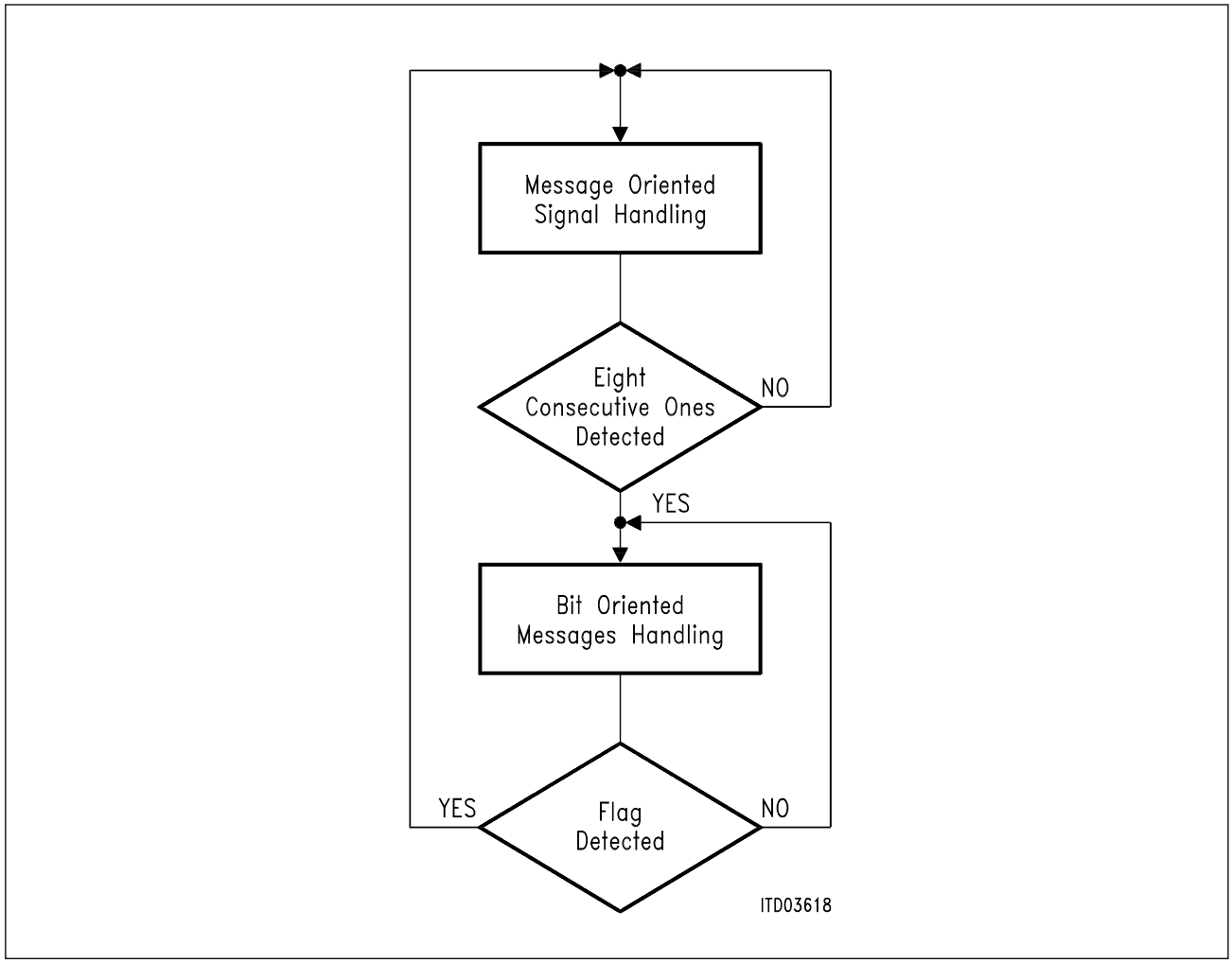


Figure 1
Switching between HDLC and BOM Mode

HDLC Mode

Receive Direction

Depending on the selected address mode, the PRISM can perform a 2-byte, 1-byte or no address recognition (**see Operating Modes**).

Transmit Direction

During HDCL operation Clock Configuration Register 1 (CCR1) can be programmed to HDLC interframe timefill mode. Either flags or idle as interframe timefill may be selected. (CCR1: ITM, IT1, IT0, **see Register Definitions**).

An HDLC frame may now be initiated by the CPU (**see Data Transmission**).

Note: An HDLC frame may be transmitted also if BOM interframe timefill mode is selected.

BOM Mode

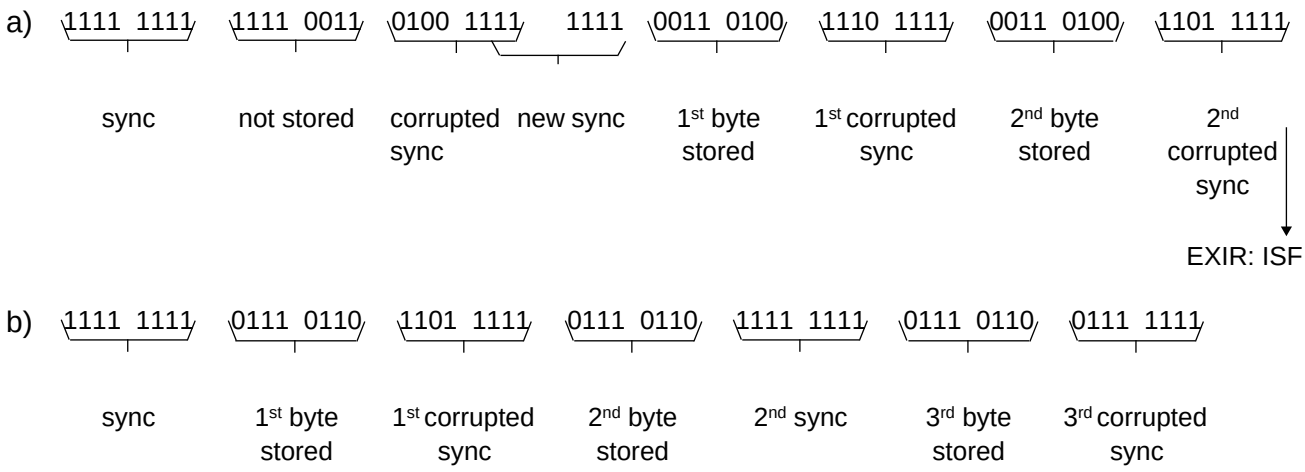
Receive Direction

In BOM mode, the following byte format is assumed (the left most bit is received first).

11111111 0xxxxxx0

The PRISM uses the FF$_H$ byte for synchronization, the next byte is stored in RFIFO (first bit received: lsb) if it starts and ends with a '0'. Bytes starting or ending with a '1' are not stored. If there are no 8 consecutive one's detected within 32 bit, an interrupt is generated (EXIR: ISF, c.f. 4.2). However, byte sampling is not stopped.

Byte Sampling in BOM Mode



Two different BOM reception modes may be programmed (MODE: BRM, see Register Definitions).

10 byte packets: After storing 10 bytes in RFIFO the receive status byte marking a BOM frame (RSTA: HFR, see Register Definitions) is added as the eleventh byte and an interrupt (ISTA: RME) is generated. The sampling of data bytes continues and interrupts are generated every 10 bytes until an HDLC flag is detected.

Continuous reception: Interrupts are generated every 32 bytes (ISTA: RPF). After detecting an HDLC flag, byte sampling is stopped, the receive status byte is stored in RFIFO and an RME interrupt is generated (ISTA: RME).

The user may switch between these modes at any time. Byte sampling may be stopped by deactivating the BOM receiver (MODE: BRAC). In this case the receive status byte is added, an interrupt is generated (ISTA: RME) and HDLC mode is entered. Whether the PRISM operates in HDLC or BOM mode may be checked by reading the Status Register (STAR: BOM, see Register Definitions).

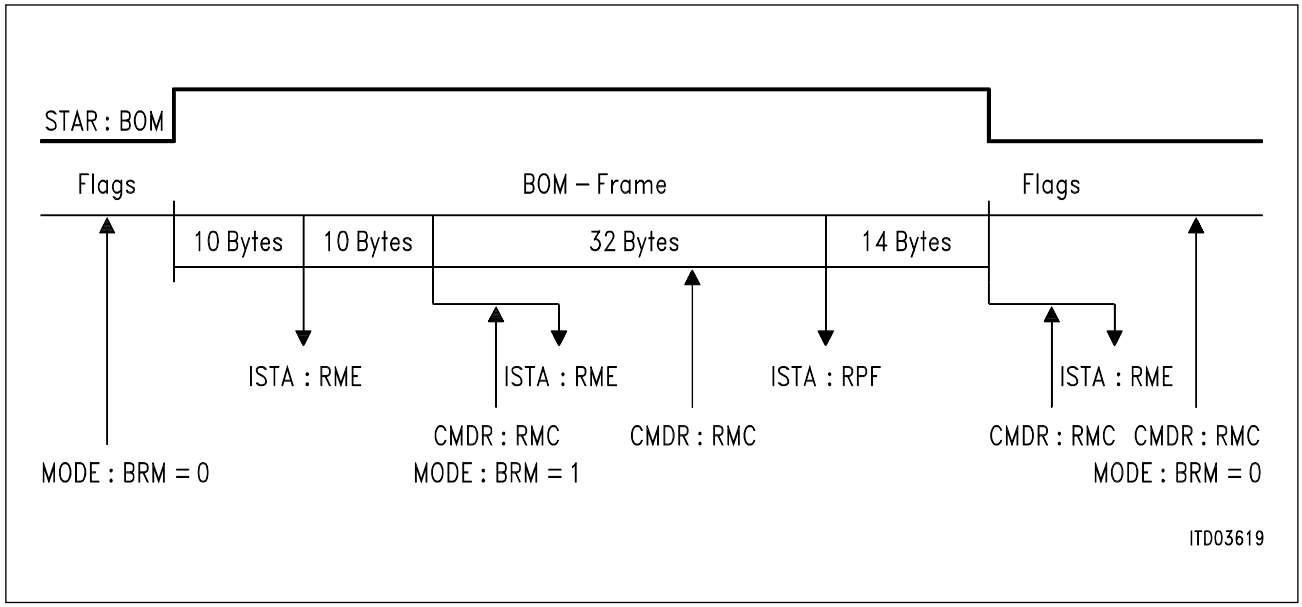


Figure 2
Reception of a BOM Frame, Example

Note: Yellow alarm bytes are also stored in RFIFO. If a BOM byte can not be stored due to a full RFIFO an interrupt is generated (EXIR: RFO, see Register Definitions).

Yellow Alarm Detection

A yellow alarm condition is indicated by the following byte format:

11111111 00000000

Two different algorithms for yellow alarm detection are programmable (YADR: YDM, see Register Definitions)

Two of two: Yellow alarm is switched on if two yellow alarm indications in sequence are detected.

Seven of ten: Yellow alarm is switched on if at least seven yellow alarm indications out of ten are detected. The mechanism starts immediately after BOM mode is entered and checks always the last ten indications received.

Note: The reception of an HDLC flag resets the yellow alarm search.

If the yellow alarm-on condition is detected, the PRISM generates an interrupt (ISTA:RSC, see Register Definitions) and the actual state may be read from Status Register (STAR: YAL). Now the yellow alarm-off detection mechanism is started. Yellow alarm is turned off if no yellow alarm indication is received for a programmable number of times (YADR, see Register Definitions). An interrupt is generated again (ISTA: RSC) and STAR: YAL may be checked. The yellow alarm/on state can also be cleared by writing the Yellow Alarm Detection Register (YADR).

Note: Yellow alarm is not switched off and the yellow alarm-off detection mechanism is not stopped after receiving an HDLC flag, because HDLC flags may be caused by single bit errors on the line.

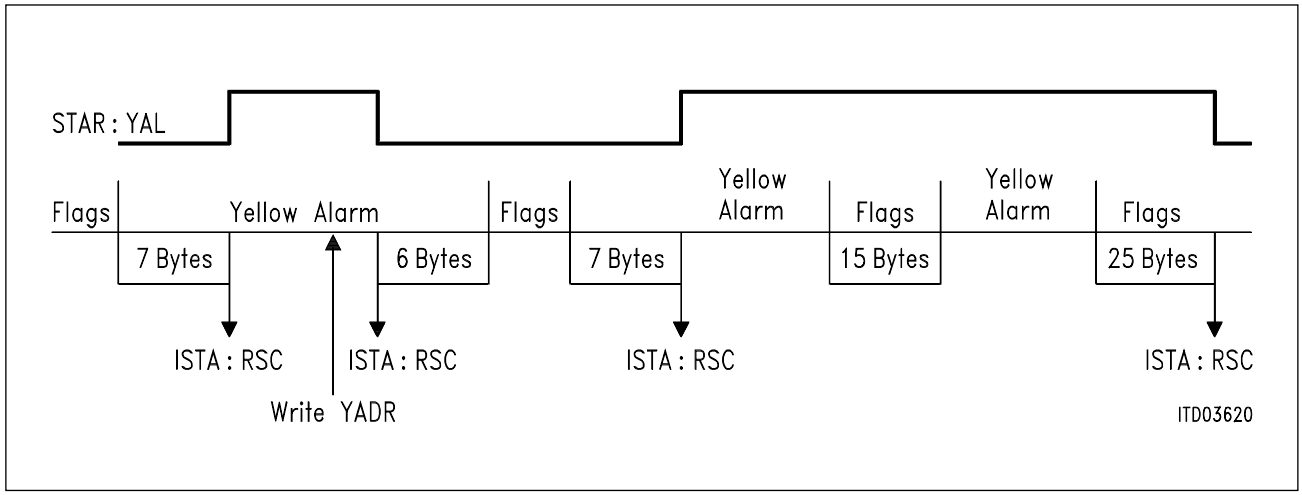


Figure 3
Yellow Alarm Detection, Example

Transmit Direction

Operating in BOM mode, Clock Configuration Register 1 (CCR1) may be programmed to BOM interframe timefill mode where one of four idle codes may be selected (CCR1: ITM, IT1, IT0 see Register Definitions). Therefore yellow alarm can be issued by programming ITM = 1, IT1 = 0, IT2 = 0.

A BOM frame may be initiated by the CPU either as a transparent frame or a cyclic transmission frame.

In a special transparent transmission mode (MODE: TXM, see Register Definitions) the PRISM generates a sync byte (FF$_H$) in front of every data byte. Therefore only data bytes have to be entered into XFIFO, the requested interrupt reaction time is doubled. This mode may also be used with a cyclic transmission frame.

Note: A transparent frame may also be transmitted with ‘idle’ or ‘flags’ as interframe timefill.

Operating Modes

The HDLC controller of each channel can be programmed to operate in various modes, which are different in the treatment of the frames in receive direction. Thus, the receive data flow and the address recognition features can be effected in a very flexible way, which satisfies a whole variety of requirements.

There are 6 different operating modes which can be set via the MODE register.

2-Byte Address Comparison

The high address byte is compared with three individually programmable values in RAH1, RAH2 and RAH3 registers. Bit 1 of the high byte address is excluded from the address comparison of RAH1 (7 bit) and is included with RAH2 and RAH3 (8 bit). The result of the address comparison is stored in the Receive Status Register (RSTA:HAD1,0, see Register Definitions).

Similarly, two compare values can be programmed in special registers (RAL1, RAL2) for the low address byte. A valid address will be recognized when the high and low byte of the address field correspond to one of the compare values. Thus, the PRISM can be called with 8 different address combinations, HDLC frames with address fields not matching one of these address combinations are ignored.

The HDLC control field, data in the I-field and an additional status byte are temporarily stored in the RFIFO. The HDLC control field and additional information can also be read from special registers (RHCR, RSTA).

1-Byte Address Comparison RAL

The first byte after the opening flag is compared with two individually programmable values in RAL1 and RAL2 registers. The result of the address comparison is stored in the Receive Status Register (RSTA: LAD, see Register Definitions). The whole frame except the address byte plus an additional status byte (RSTA) is stored in RFIFO. The HDLC control field and additional information can also be read from special registers (RHCR, RSTA).

1-Byte Address Comparison RAH

The first byte after the opening flag is compared with three individually programmable values in RAH1, RAH2 and RAH3 registers. Bit 1 is excluded from address comparison of RAH1 and is included with RAH2 and RAH3. The result of the address comparison is stored in the Receive Status Register (RSTA:HAD1,0, see Register Definitions). The whole frame except the address byte plus an additional status byte (RSTA) is stored in RFIFO. RAL1 contains a copy of the second an RHCR of the third byte following the opening flag.

No Address Comparison

No address recognition is performed and each frame will be stored in the RFIFO. RAL1 contains a copy of the first and RHCR, the second byte following the opening flag.

No HDLC Framing Modes 0, 1

Fully transparent data reception without HDLC framing is performed, i.e. without FLAG recognition, CRC check, bit-stuffing mechanism. Data is stored in RAL1 register, in mode 1 data is also stored in RFIFO.

Receive Data Flow (Summary)

The following figure provides an overview of the HDLC received-frame management under the various operating modes.

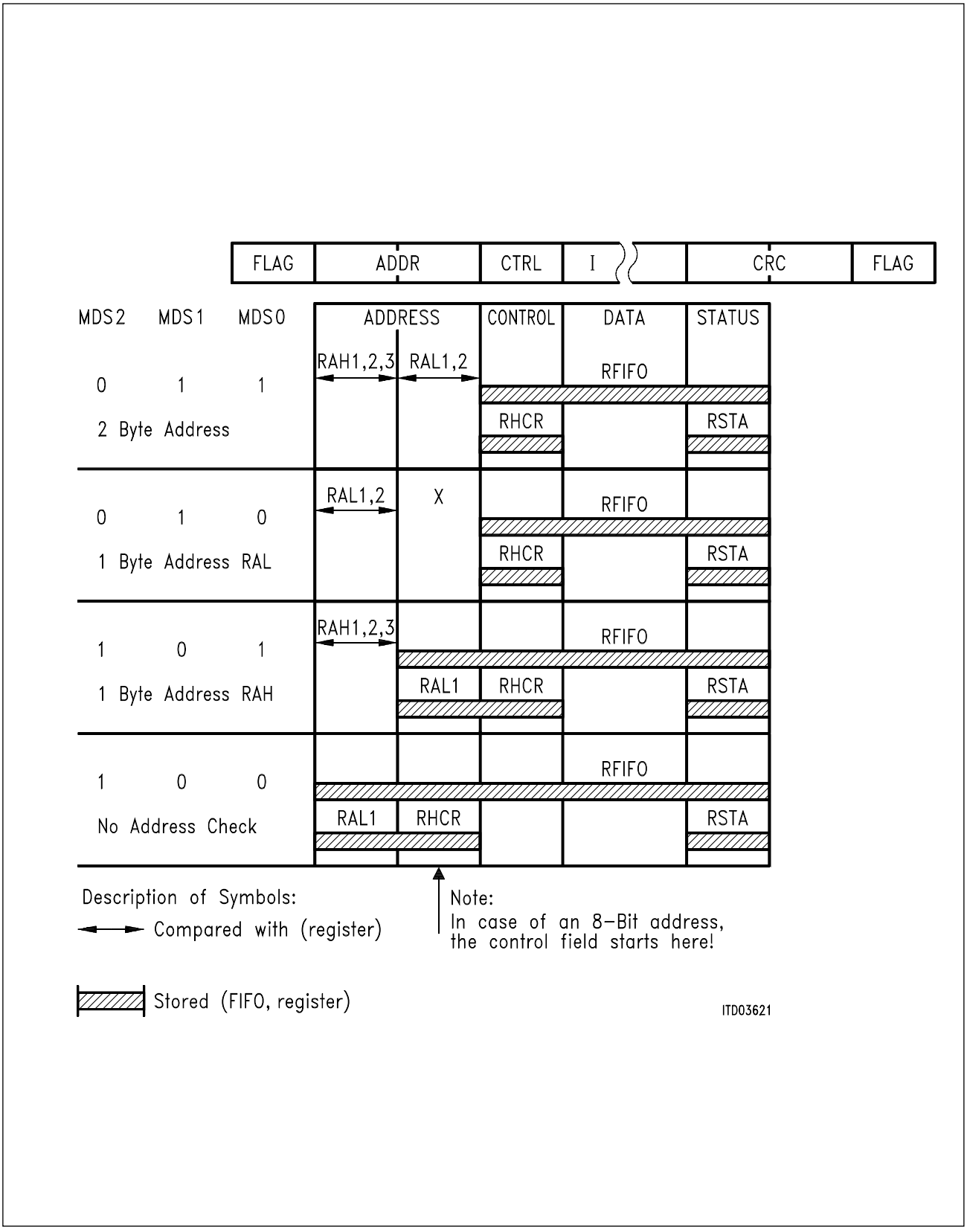


Figure 4
Receive Data Flow of PRISM

Transmit Data Flow

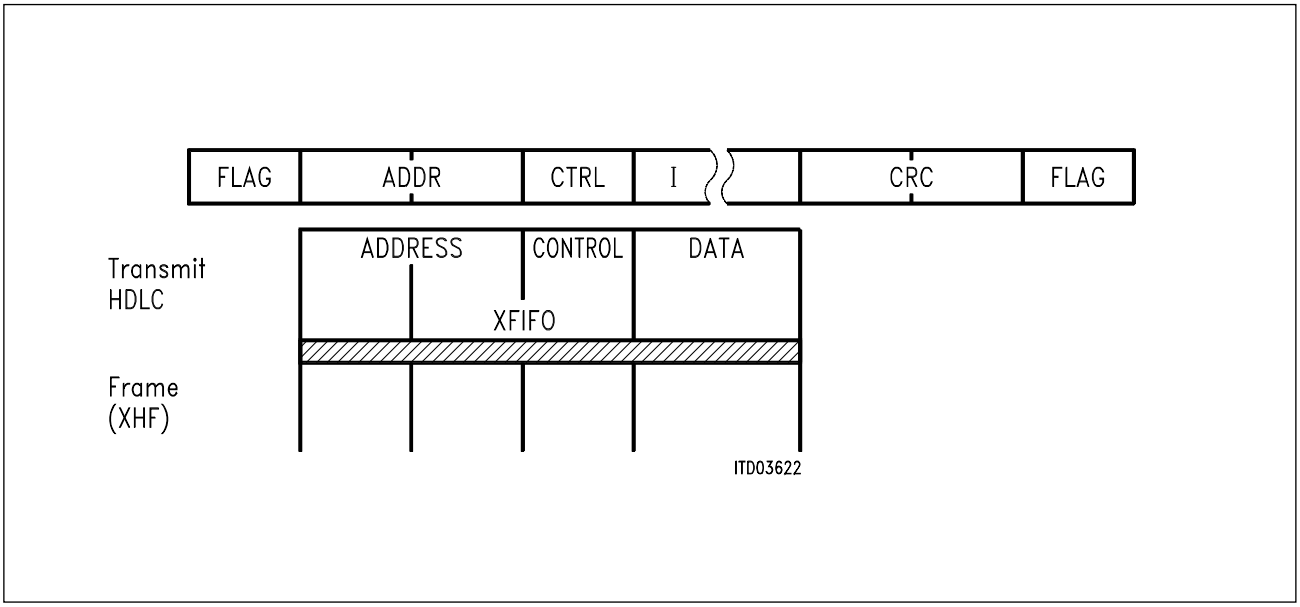


Figure 5
Transmit Data Flow of PRISM

For HDLC frames (command XHF via CMDR register), the address and the control fields have to be entered in the XFIFO as well.

CPU Interface

Register Set

The communication between the CPU and the PRISM is done via a set of directly accessible 8-bit registers. The CPU sets the operating modes, controls function sequences, and gets status information by writing or reading these registers (command/status transfer). Complete information concerning the register functions is provided in chapter Detailed Register Description.

Each of the two serial channels of the PRISM is controlled via an identical, but totally independent register set (channel A and channel B).

Interrupt Interface

Special events in the PRISM are indicated by means of a single interrupt output, which requests the CPU to read status information from the PRISM, or, if interrupt mode is selected, transfer data from/ to PRISM.

Since only one INT request output is provided, the cause of an interrupt must be determined by the CPU reading the PRISM's interrupt status registers (ISTA, EXIR).

The structure of the interrupt status registers is shown in **figure 6.**

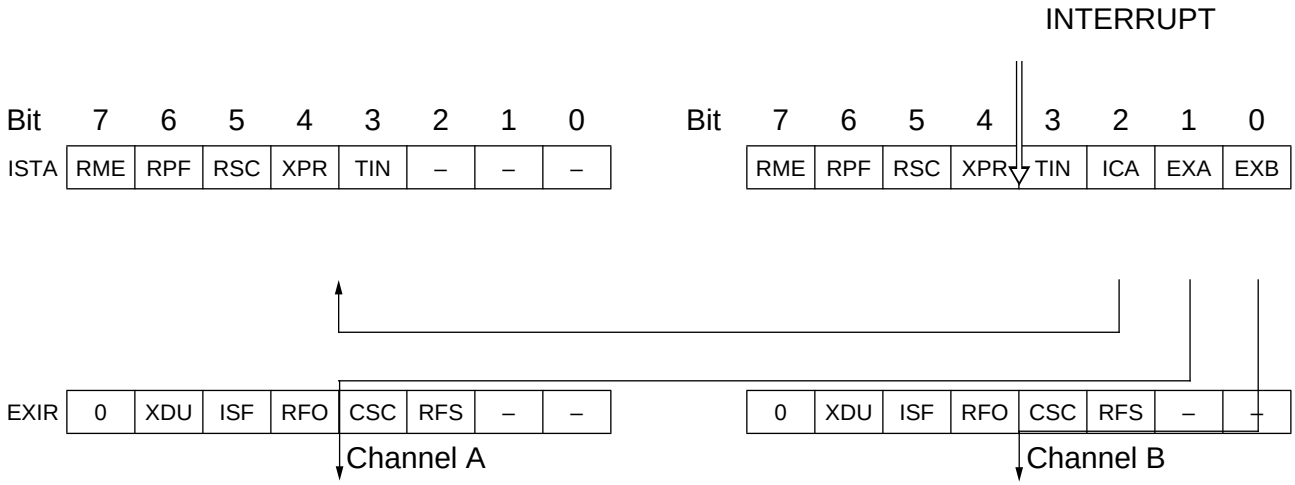


Figure 6
PRISM Interrupt Status Register

Five interrupt indications can be read directly from the ISTA register and another six interrupt indications from the extended interrupt register (EXIR).

After the PRISM has requested an interrupt by setting its INT pin to low, the CPU must first read the interrupt status register of channel B (ISTA-B) in the associated interrupt service routine. The three lowest order bits (bit 2-0) of ISTA-B (ICA, EXA, EXB) point, if set, to those registers in which the actual interrupt source are indicated. It is possible that several interrupt sources are indicated by a single interrupt request (e.g. if the ICA bit is set, at least one interrupt is indicated in the ISTA register of channel A).

An interrupt source from channel B is implicitly indicated by bits 7-3 of ISTA-B; therefore these bits must also always be checked.

The PRISM interrupt sources can be logically grouped into

- receive interrupts,
- transmit interrupts, and
- special condition interrupts.

Each interrupt of the ISTA registers can be selectively masked by setting the respective bit in the MASK register.

The following tables give a complete overview of the individual interrupt indications and the cause of their activation. Specific restrictions are marked with ”*”.

Table 1
Receive Interrupts

RPF	Receive Pool Full (ISTA)	Activated as soon as 32 bytes are stored in the RFIFO but the message is not yet completed.
RME	Receive Message End (ISTA)	Activated if either one message up to 32 bytes or the last part of a message with more than 32 bytes is stored in the RFIFO.
RFO	Receive Frame Overflow (EXIR)	Activated if a complete frame could not be stored due to occupied RFIFO, i.e. the RFIFO is full and the PRISM has detected the start of a new frame.
RFS	Receive Frame Start (EXIR)	* Only activated if enabled by setting the RIE bit in CCR2 register. Activated after the **start** of a valid frame has been detected, i.e. after a valid address check in operation modes providing address recognition, otherwise after the opening flag (transparent mode 0), delayed by two bytes. After an RFS interrupt, the contents of – RHCR – RAL1 – RSTA - bit 3-0 are valid and can be read by the CPU.

Table 2
Transmit Interrupts

XPR	Transmit Pool Ready (ISTA)	Activated whenever a 32-byte FIFO pool is empty and accessible to the CPU, i.e. – following a XRES command via CMDR, – repeatedly during frame transmission started by XHF command, and no end of message indication (XME command) has been issued yet by the CPU, – after the end-of-message indication when frame transmission of a transparent frame or HDLC frame is completed (i.e. CRC and closing flag sequence are shifted out).
XDU	Transmit Data Underrun (EXIR)	Activated if the XFIFO holds no further data, i.e. all data has been shifted out via the serial TxD pin, but no End Of Message (EOM) indication has been detected by the PRISM.

Table 3
Special Condition Interrupts

RSC	Receive Status Change	Activated after a status change of the opposite stations receiver has been detected (yellow alarm ON/OFF).
ISF	Incorrect Sync Format	Activated if no eight consecutive one's within 32 bits can be detected (BOM receiver active).

Internal Timer

TIN	Timer Interrupt (ISTA)	Activated if the internal timer has expired (see description of TIMH, TIML register in chapter Register Description).

External Pin

CSC	CTS Status Change (EXIR)	* Only activated if enabled by setting the CIE bit in the CCR2 register.

FIFO Structure

In both transmit and receive direction 64-byte deep FIFO's are provided for the intermediate storage of data between the serial interface and the CPU interface. The FIFO's are divided into two halves of 32-bytes, where only one half is accessible to the CPU at any time.

The organization of the Receive FIFO (RFIFO) is such, that in the case of a frame up to 64 bytes long, the whole frame may be stored in the RFIFO. After the first 32 bytes have been received, the PRISM prompts to read the 32-byte block by means of interrupt (RPF interrupt). This block remains in the RFIFO until a confirmation is given to the PRISM acknowledging the transfer of the data block. This confirmation is a RMC (Receive Message Complete) command via the CMDR register. As a result, it's possible, to read out the data block any number of times until the RMC command is issued.

The configuration of the RFIFO prior to and after acknowledgement is shown in **figure 7.**

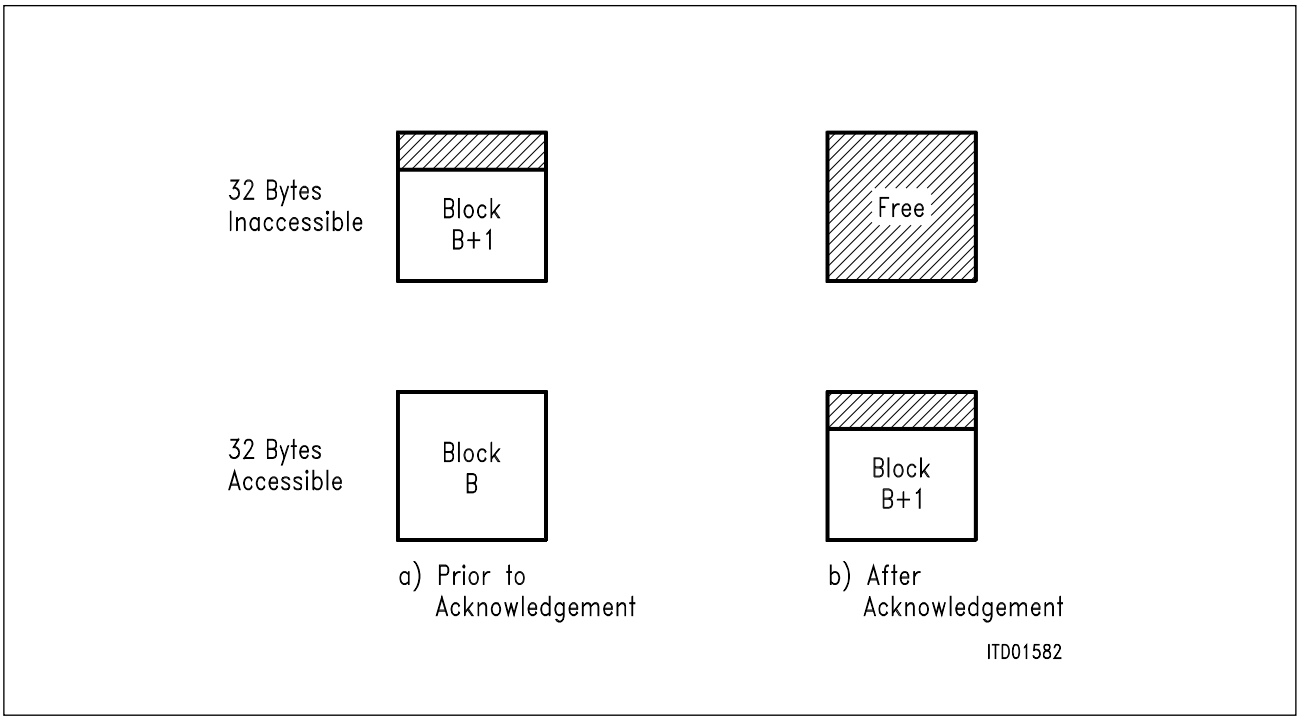


Figure 7
Configuration of RFIFO (Long Frames)

If frames longer than 64 bytes are received, the device will repeatedly prompt to read out 32-byte data blocks via interrupt.

In the case of several shorter frames, up to 17 may be stored in the PRISM.

If the accessible half of the RFIFO contains a frame i (or the last part of frame i), up to 16 short frames may be stored in the other half (i + 1, … , i + n), prior to frame i being fetched from the RFIFO.

This is illustrated in **figure 8**.

For a description of a transmit and receive sequence in both Interrupt or DMA Mode, please refer to chapter Data Transmission and Data Reception.If frames longer than 64 bytes are received, the device will repeatedly prompt to read out 32-byte

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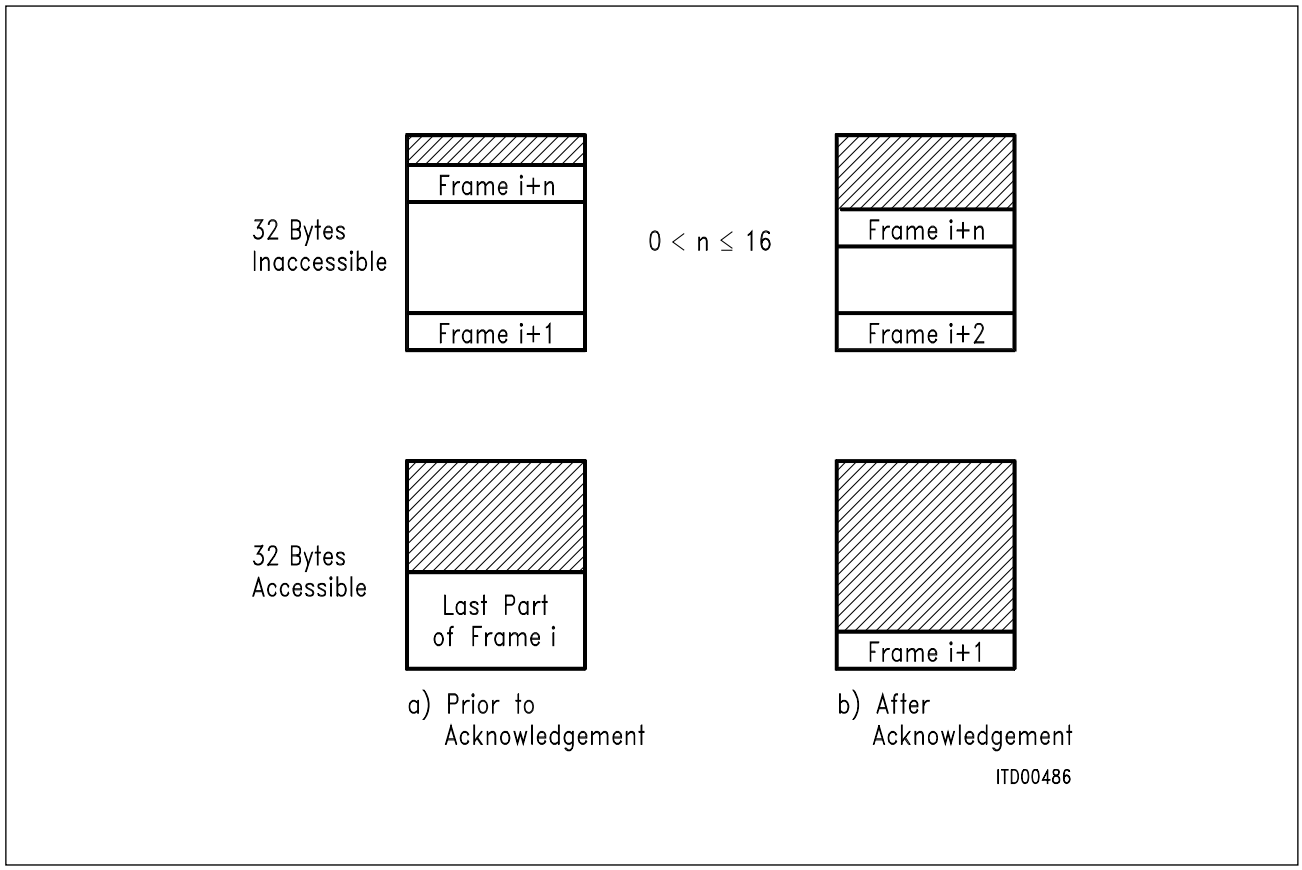

Figure 8
Configuration of RFIFO (Short Frames)

Note: The number of 17 frames applies for the PRISM operating in the auto- or non-auto-mode (address recognition), and short frames containing only the HDLC address and control field are received. Since the address is not stored, the control field is always stored first in the RFIFO, and an additional status byte is always appended at the end of each frame in the RFIFO, these frames will occupy two bytes.

Clock Modes

The PEB 3035 PRISM can be operated in three different clock modes.

- serial mode (clock mode 0)
- strobe mode (clock mode 1)
- time-slot assignment mode (clock mode 2)

Table 4
Overview of Clock Modes

Clock		
Type	**Source**	**Mode**
Receive Clock	RxCLK Pins	0, 1, 2
Transmit Clock	TxCLK Pins RxCLK Pins	0 1, 2
Strobe pulse receive Strobe pulse transmit	TxCLKA Pin TxCLKB Pin	1 1
Frame sync. pulse receive, transmit	TxCLKA Pin	2

Clock Mode 0 (External Clocks)

Separate, externally generated receive and transmit clocks are forwarded to the PRISM via their respective pins.

Clock Mode 1 (Rec./Trm. Strobes)

Externally generated, but identical receive and transmit clocks are forwarded via RxCLK pins. In addition, a receive strobe can be connected via TxCLKA and a transmit strobe via TxCLKB pins. This operating mode can be applied in time division multiplex applications.

Clock Mode 2 (Time Slots)

This operating mode has been designed for application in time-slot oriented PCM systems.

The receive and transmit clock is identical for each channel and must be supplied externally via RxCLK pins. The PRISM receives and transmits only during certain time slots of programmable width (1 … 256 bit, via RCCR and XCCR registers) and location with respect to a frame synchronization signal, which must be delivered to the PRISM via the TxCLKA pin. One of up to 64-time slots can be programmed independently for receive and transmit direction via TSAR and TSAX registers, and an additional clock shift of 0 … 7 bits via TSAR, TSAX, and CCR2 registers. Together with bits XCS0 and RCS0 (LSB of clock shift), located in the CCR2 register, there are 9 bits to determine the location of a time slot.

According to the value programmed via those bits, the receive/transmit window (time slot) starts with a delay of 1 (minimum delay) up to 512-clock periods following the frame synchronization signal and is active during the number of clock periods programmed via RCCR, XCCR (number of bits to be received/transmitted within a time slot) as shown in **figure 9**.

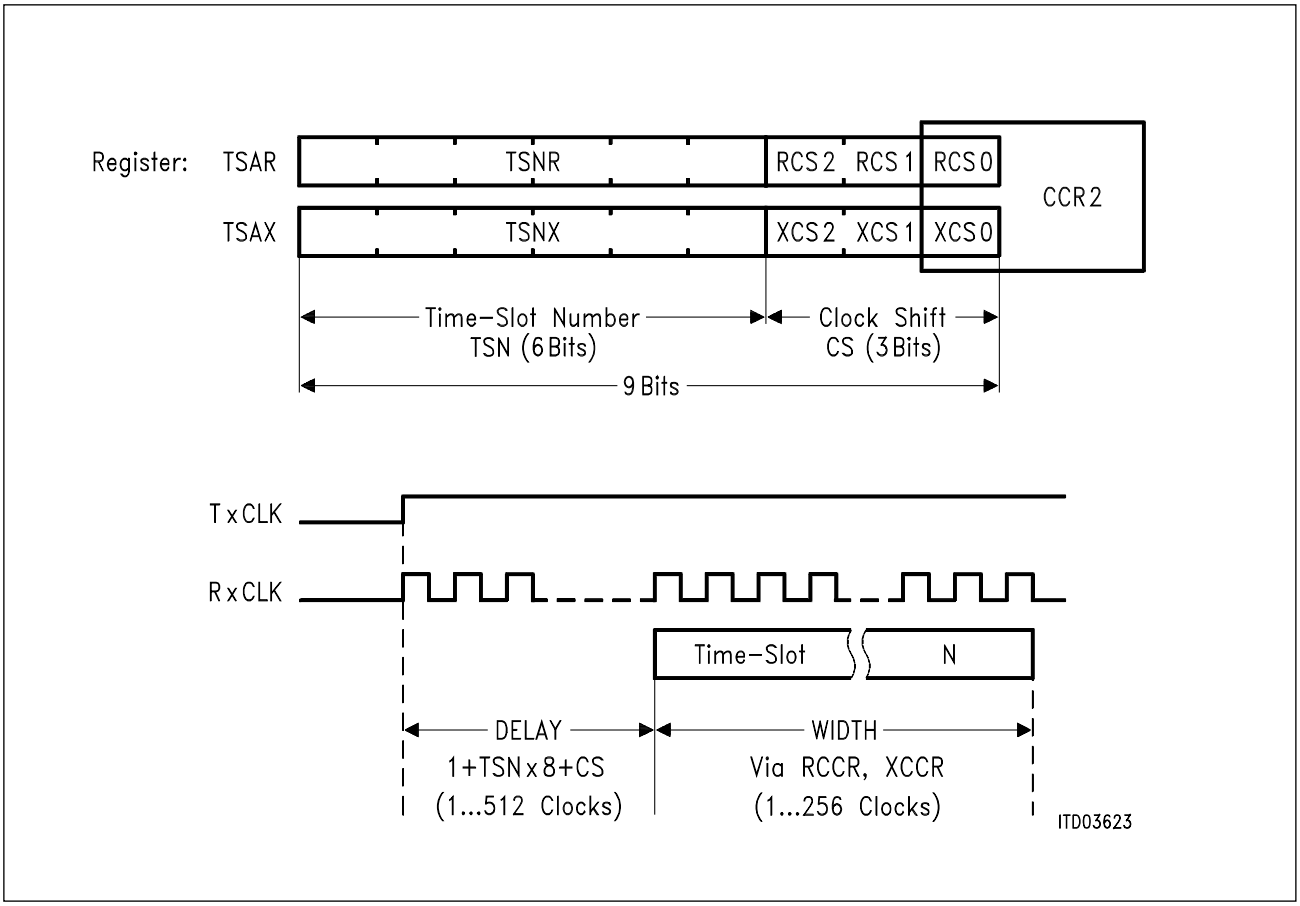

Figure 9
Location of Time Slots

The transmit time slot is additionally indicated by a control signal via TxCLKB if enabled via CCR2:TIO (active low).

Special Functions

Fully Transparent Transmission

The PRISM supports fully transparent data transmission without HDLC framing overhead, i.e. without

- FLAG insertion and deletion
- CRC generation and checking
- Bit-stuffing mechanism

Data transmission is always performed out of the transmit FIFO by directly shifting the contents of the XFIFO via the serial transmit data pin (T×D). Transmission is initiated by setting CMDR:XTF or CMDR: XTF.XME (04H or 06H); end of transmission is indicated by ISTA:XPR.

This feature can be profitably used e.g. for:

- user specific protocol variations
- transmission of a BOM frame
- test purposes, intentional violations of HDLC protocol rules (e.g. wrong CRC)

Cyclic Transmission (Fully Transparent)

The PRISM supports the continuous transmission of the transmit FIFO's contents.

After having written 1 to 64 bytes to the XFIFO, the command

XREP.XTF.XME

via the CMDR register (bit 7 … 0 = 26H) forces the PRISM to repeatedly transmit the data stored in the XFIFO via the T×D pin. A cyclic transmission is indicated in the STAR register.
A cyclic transmission frame may immediately be added to an other cyclic transmission or transparent frame.

Transparent frame followed by cyclic transmission: write exactly 32 bytes to XFIFO and initiate transmission by setting CMDR:XTF (04H). After transmission is started the PRISM generates an XPR interrupt (ISTA:XPR). Now write 1-32 bytes to XFIFO and start cyclic transmission by setting CMDR: XREP.XTF.XME (26H). The PRISM will transmit the first 32 bytes and then will start a cyclic transmission of the second data pool.

Note: It is also possible to transmit n × 32 bytes before starting cyclic transmission.

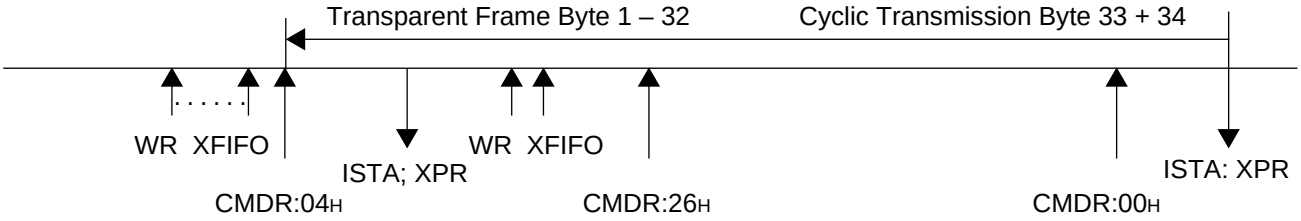

Figure 10
Transparent Frame Plus Cyclic Transmission

Cyclic transmission sequences: write exactly 32 bytes to XFIFO and write CMDR: XREP.XTF (24H). The PRISM starts cyclic transmission and generates an XPR-interrupt (ISTA: XPR). Again 32 bytes may be entered into XFIFO. Now setting CMDR:XREP.XTF causes the PRISM to use the second data pool for cyclic transmission and generate an XPR interrupt. This sequence may be repeated.

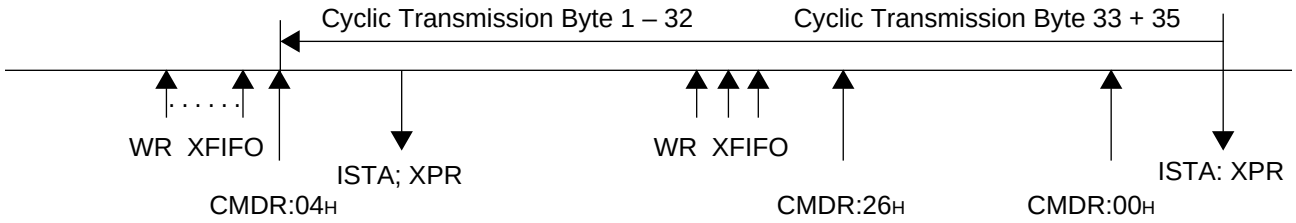

Figure 11
Cyclic Transmission Sequences

If CMDR:XREP is released, the cyclic transmission is stopped after the last byte in XFIFO, after a reset command (CMDR:XRES) it is stopped immediately.

Note: During cyclic transmission the XREP-bit has to be set with every write operation to CMDR.

Receive Length Check Feature

The PRISM offers the possibility to supervise the maximum length of received frames and to terminate data reception in case this length is exceeded.

This feature is controlled via the special Receive Length Check Register (RLCR).

The function is enabled by setting the RC (Receive Check) bit in RLCR and programming the maximum frame length via bits RL6 … RL0.

According to the value written to RL6 … RL0, the maximum receive length can be adjusted in multiples of 32-byte blocks as follows:

$$\text{MAX.LENGTH} = (\text{RL} + 1) \times 32.$$

All frames exceeding this length are treated as if they have been aborted from the opposite station, i.e. the CPU is informed via a

- RME interrupt, and the
- RAB bit in RSTA register is set!

To distinguish between frames really aborted from the opposite station, the receive byte count (readable from RBCH, RBCL registers) exceeds the maximum receive length (via RL6 … RL0) by one or two bytes in this case.

Data Inversion

When NRZ data encoding has been selected, the PRISM may transmit and receive data inverted, i.e. a “one” bit is transmitted as phys.zero (0 V) and a “zero” bit as phys.one (+ 5 V) via the TxD line.

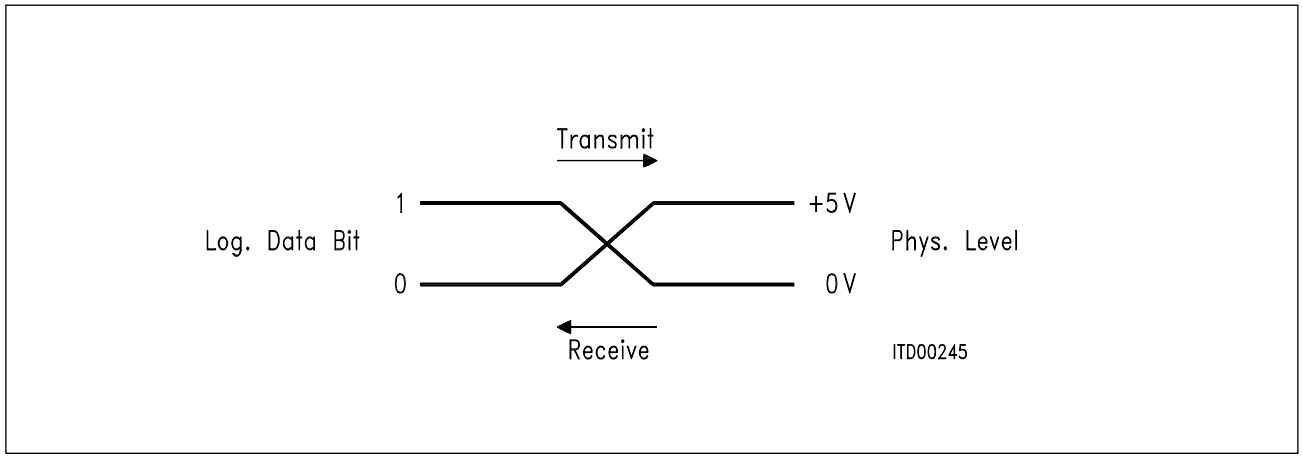

Figure 12

This feature is selected by setting the DIV bit in the CCR2 register.

Test Mode

To provide for fast and efficient testing, the PRISM can be operated in the test mode by setting the TLP bit in the MODE register.

The on-chip serial input and output (TxDA – RxDA, TxDB – RxDB) are connected generating a local loopback. In clock mode 0 the transmit clock is used for reception also.

As a result, the user can perform a self-test of the serial channels of the PRISM.

Operational Description

Reset

The PRISM is forced into the reset state if a high signal is input to the RES pin for a minimum period of 1.8 µs. During the RESET period, the PRISM is temporarily in the power-up mode, and a subset of the registers is initialized with defined values.

After RESET, the PRISM is in power-down mode, and the following registers contain defined values:

Table 5
Reset Values

Register	Reset Value	Meaning
CCR1	00H	– power down mode – transmit data pins are open drain outputs – clock mode 0
CCR2	00H	– CTS and RFS interrupts disabled no data inversion
MODE	00H	1 byte address check – receivers inactive RTS output controlled by PRISM, no testloop
STAR	48H	XFIFO write enable receive line inactive no commands executing
ISTA EXIR	00H	– no interrupts masked
CMDR	00H	no commands
XCCR RCCR	00H	1-bit time slots

Initialization

After reset the CPU has to write a minimum set of registers and an optional set depending on the required features and operating modes.

First, the configuration of the serial port and the clock mode have to be defined via the CCR1 register. The clock mode must be set before power-up, or in the same step with power-up.

The CPU may switch the PRISM between power-up and power-down mode, which has no influence upon the contents of the registers, i.e. the internal state remains stored.

In power-down mode however, all internal clocks are disabled, no interrupts are forwarded to the CPU.

This state can be used as standby mode, when the PRISM is temporarily not used, thus considerably reducing the power consumption.

The individual operating mode must be defined by writing to the MODE register.

The need for programming further registers depends on the selected features (clock mode, operating mode, user demands) according to the following tables:

Clock Mode	Register
0, 1	–
2	CCR2, TSAR, TSAX, XCCR, RCCR

Table 6
Required Register Address Programming for HDLC and BOM Data Reception

Address Mode / Data Format	2 Byte Address Field	1 Byte Address Field
HDLC	RAH1, RAH2, RAH3 RAL1, RAL2	RAH1, RAH2, RAH3 (Mode 101) RAL, RAL2 (Mode 011)
BOM	 YADR	– YADR
Transparent	–	–

Table 7
User Demand Registers

User Demand	Register
CTS/RFS Interrupt Provided	CCR2
Selective Interrupts Should be Masked	MASK
Timer will be used by CPU	TIML TIMH
Receive Length Check Feature	RLCR

Operational Phase

After having performed the initialization, the CPU switches each individual channel of the PRISM into operational phase by setting the PU bit in the CCR1 register (power-up, if not already done during initialization).

Initially, the CPU should bring the transmitter and receiver to a defined state by issuing a XRES (transmitter reset) and RHR (receiver reset) command via the CMDR register.

If data reception should be performed, the receivers must be activated by setting the HRAC/BRAC bits in MODE to 1.

Now the PRISM is ready to transmit and receive data. The control of the data transfer phase is mainly done by commands from CPU to PRISM via the CMDR register, and by interrupt indications from PRISM to CPU.

Additional status information, which does not trigger an interrupt, is available in the STAR register.

Data Transmission

In transmit direction 2×32 byte FIFO buffers (transmit pools) are provided for each channel.

After checking the XFIFO status by polling the Transmit FIFO Write enable bit (XFW in STAR register) or after a Transmit Pool Ready (XPR) interrupt, up to 32 bytes may be entered by the CPU into the XFIFO.

The transmission of a HDLC frame can then be started by issuing an XHF command via the CMDR register. If the transmit command does not include an end of message indication (CMDR: XME), the PRISM will repeatedly request for the next data block by means of an XPR interrupt as soon as a 32-byte pool is accessible to the CPU.

This process will be repeated until the CPU generates the end of message command (CMDR.XME), after which frame transmission is finished correctly by appending the CRC and closing flag sequence.

In the case of no more data being available in the XFIFO prior to the arrival of XME, the transmission of the frame is terminated with an abort sequence and the CPU is notified per interrupt (EXIR: XDU). The frame may also be aborted via software (CMDR: XRES).

The data transmission sequence, from the CPU's point of view, is outlined in **figure 13**.

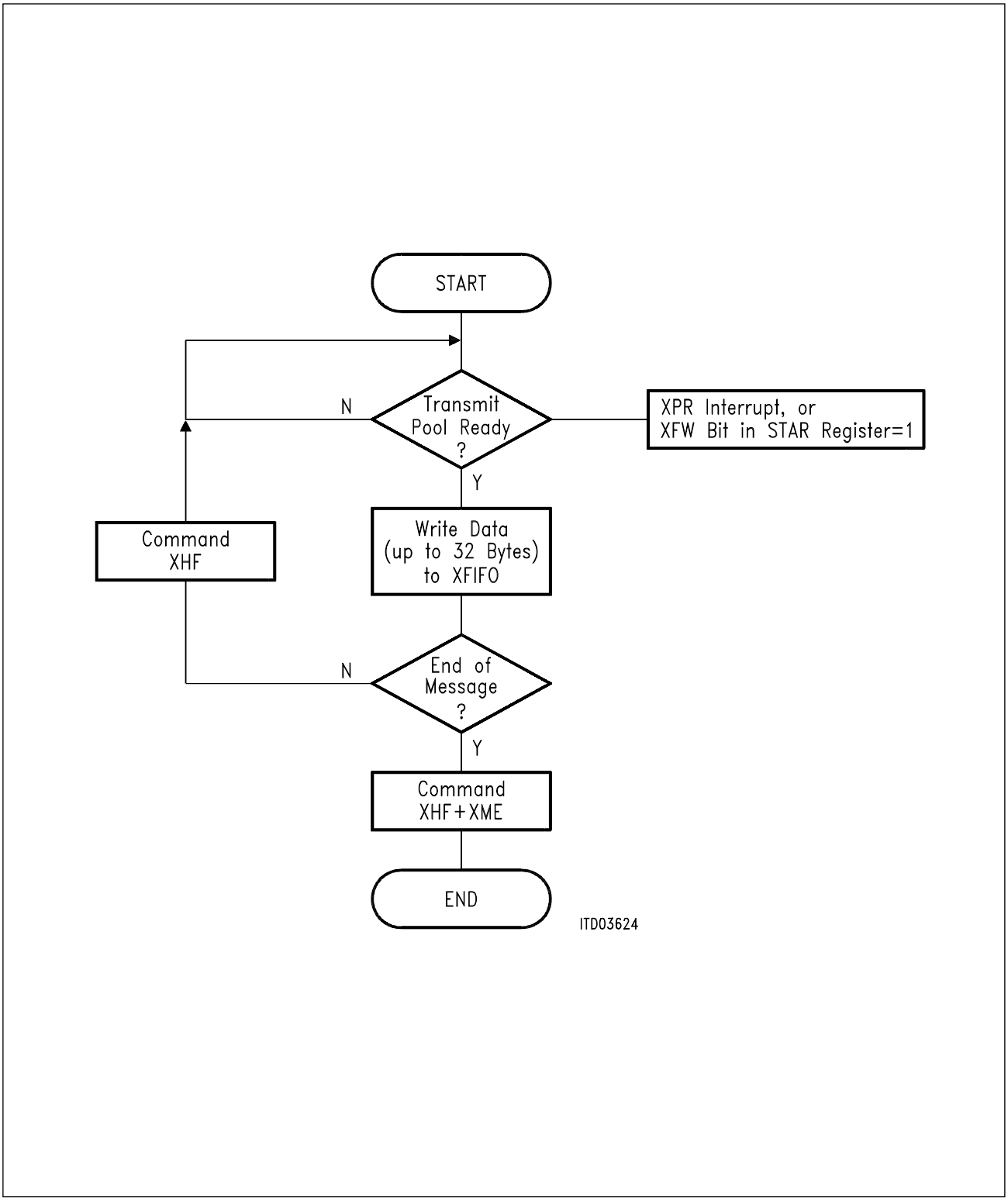

Figure 13
Data Transmission (Flow Diagram)

The activities at both serial and CPU interface during frame transmission (example: frame length = 70 bytes) is shown in **figure 14**.

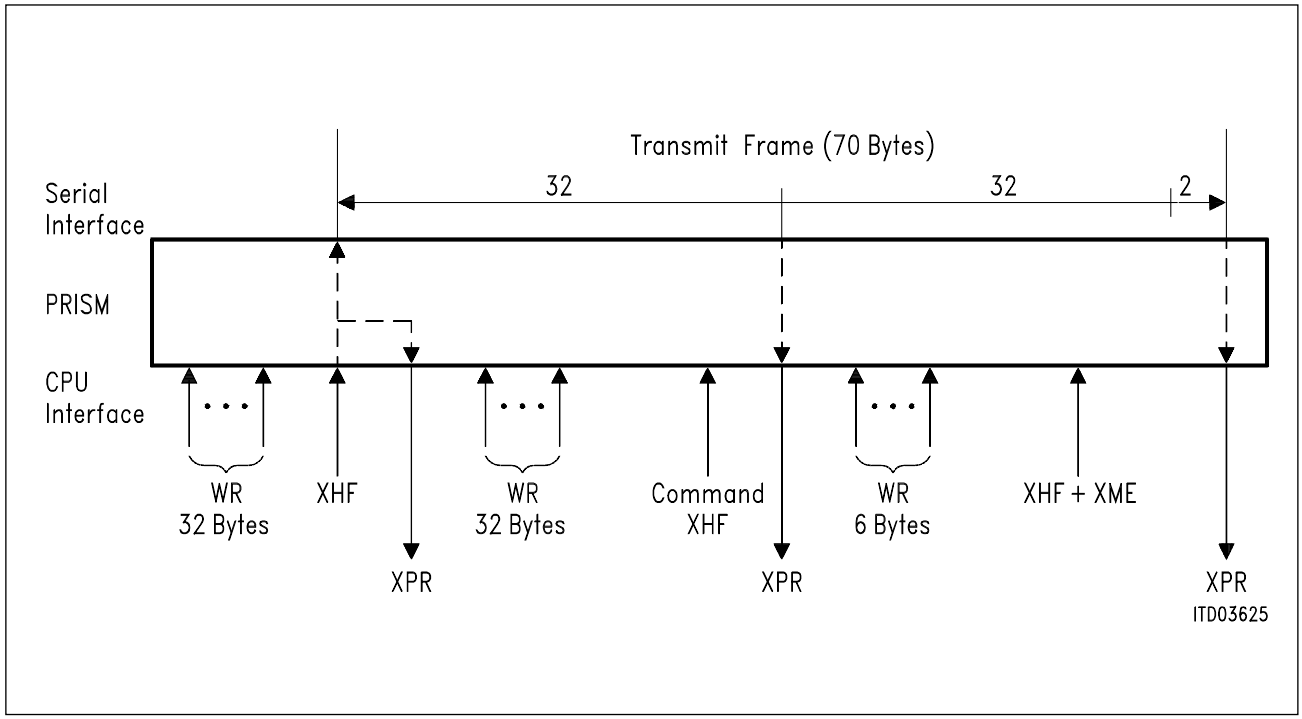

Figure 14
Transmission Sequence Example

Data Reception

Two 32-byte FIFO buffers (receive pools) are also provided for each channel in the receive direction.

There are two different interrupt indications concerned with the reception of data:

- RPF (Receive Pool Full) interrupt, indicating that a 32-byte block of data can be read from the RFIFO and the received message is not yet complete.
- RME (Receive Message End) interrupt, indicating that the reception of one message is completed, i.e. either
  - one message with less than 32 bytes, or the
  - last part of a message with more than 32 bytes

is stored in the RFIFO.

After an interrupt has been processed, i.e. the received data has been read from the RFIFO, this must be explicitly acknowledged by the CPU issuing an RMC (Receive Message Complete) command.

The CPU has to handle the RPF interrupt before additional 32 bytes are received via the serial interface otherwise a “Receive Data Overflow“ condition would occur.

In addition to the message end (RME) interrupt, the following information about the received frame is stored by the PRISM in special registers and/or RFIFO:

Table 8
Status Information after RME Interrupt

Length of Message (Bytes)	RBCH,RBCL	Register
Address Combination AND/OR	RSTA	Register
Address Field	RAL1	Register
Control Field	RHCR	Register
Type of Frame (COMMAND/RESPONSE)	RSTA	Register
CRC Result (Good/Bad)	RSTA	Register
Valid Frame (YES/NO)	RSTA	Register
ABORT Sequence Recognized (YES/NO)	RSTA	Register
Data Overflow	RSTA	Register

The following figure gives an example of an interrupt controlled reception sequence in which a long frame (66 bytes) followed by two short frames (6 bytes each) are received.

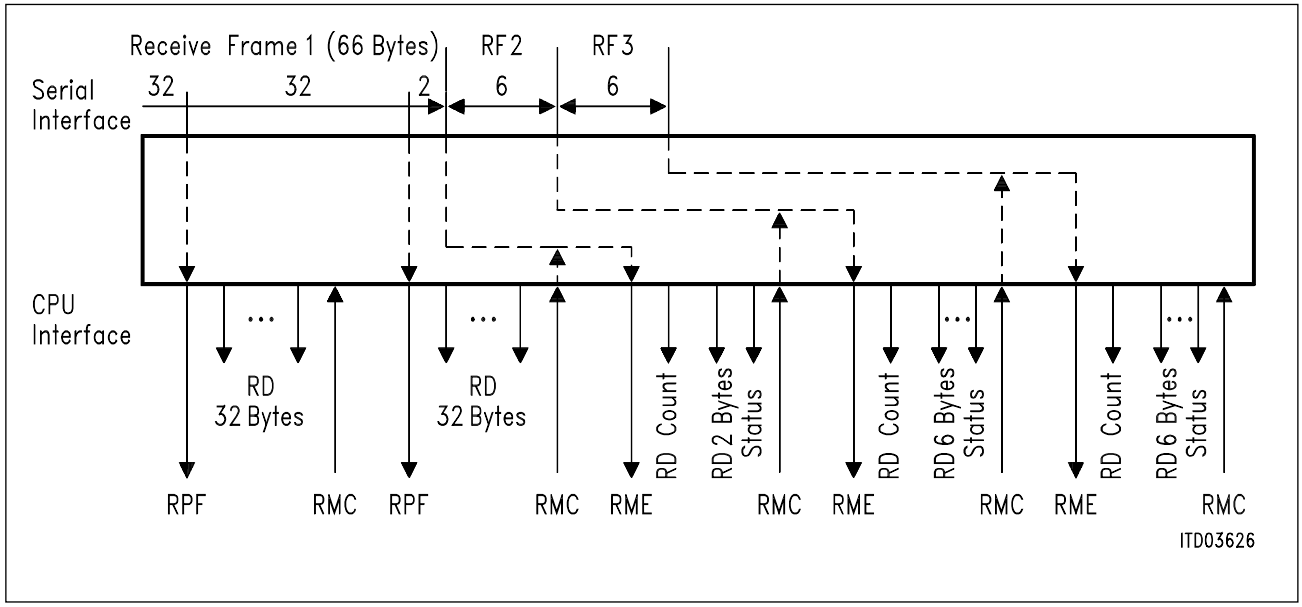

Figure 15
Interrupt Driven Reception Sequence Example

Detailed Register Description

Register Address Arrangement

Table 9
Layout of Register Addresses

Address		Register		Comment Meaning
Channel		Read	Write	
A	B			
00 . . . 1F	40 . . . 5F	RFIFO	XFIFO	Receive/Transmit FIFO
20	60	ISTA	MASK	Interrupt STAtus/MASK
21	61	STAR	CMDR	STAtus/CoMmanD
22	62	MODE		MODE
23	63	TIML		TIMer Low
24	64	EXIR	TIMH	EXtended Interrupt/TIMer High
25	65	RBCL	RAH1	Receive Byte Count Low/ Receive Address High 1
26	66	–	RAH2	Receive Address High 2
27	67	RSTA	RAH3	Receive STAtus/Rec. Addr. High 3
28	68	RAL1		Receive Address Low 1
29	69	RHCR	RAL2	Rec. HDLC Control/Rec. Addr. Low 2
2A	6A	–	–	–
2B	6B	–	YADR	Yellow Alarm Detection Register
2C	6C	CCR2		Channel Configuration Register 2
2D	6D	RBCH	–	Receive Byte Count High
2E	6E	VSTR	RLCR	Version STatus/Rec. frame Length Check
2F	6F	CCR1		Channel Configuration Register 1
30	70	–	TSAX	Time-Slot Assignment Transmit
31	71	–	TSAR	Time-Slot Assignment Receive
32	72	–	XCCR	Transmit Channel Capacity
33	73	–	RCCR	Receive Channel Capacity

Register Definitions

Receive FIFO (READ) RFIFO (00 … 1F/40 … 5F)

Up to 32 bytes of receive data can be read from the RFIFO following an RPF or an RME interrupt.

RPF Interrupt: Exactly 32 bytes to be read

RME Interrupt: Number of bytes to be determined by reading the RBCL, RBCH registers.

The register set of the PEB 3035 PRISM is based on the SAB 82525 HSCX.

Transmit FIFO (WRITE) XFIFO (00 … 1F/40 … 5F)

Up to 32 bytes of transmit data can be written to the XFIFO following an XPR interrupt or STAR.XFW = 1.

Note: Addresses within the address space of the FIFO's are interpreted equally, i.e. the actual data byte can be accessed with any address within the valid range.

Interrupt Status Register (READ)

Value after Reset: 00H

	7							0	
ISTA	RME	RPF	RSC	XPR	TIN	ICA	EXA	EXB	(20/60)

RME … Receive Message End

One message of up to 32 bytes or the last part of a message greater then 32 bytes has been received and is now available in the RFIFO. The message is complete!

The actual message length can be determined by reading the RBCH, RBCL registers.

Additional information is available in the RSTA register.

RPF … Receive Pool Full

A block of 32 bytes of a message is stored in the RFIFO. The message is not yet completed!

RSC … Receive Status Change (significant in auto-mode only!)

A status change (yellow alarm on/off status of the receiver) has been detected in auto-mode. The current status can be read from the STAR register (YAL bit, BOM bit).

XPR … Transmit Pool Ready

A data block of up to 32 bytes can be written to the transmit FIFO.

TIN … Timer Interrupt

The internal timer has expired. (See also description of TIMH/TIML registers!)

ICA … Interrupt of Channel A (Channel B only)

Indicates, that an interrupt has been caused by channel A and the interrupt source(s) is (are) indicated in the ISTA register of channel A (i.e. at least one bit of the ISTA register of channel A is set).

EXA … Extended Interrupt of Channel A (Channel B only)

An interrupt has been caused by channel A an the source(s) is (are) indicated in the EXIR register of channel A.

EXB … Extended Interrupt of Channel B (Channel B only)

An interrupt has been caused by channel B and the source(s) is (are) indicated in the EXIR register of channel B.

Note: The ICA, EXA and EXB bits are present in channel B only and point to the ISTA (chA), EXIR (chA), and EXIR (chB) registers.
After the PRISM has requested an interrupt by turning its INT pin to low, the CPU must first read the ISTA register of channel B and check the state of these bits in order to determine which interrupt source(s) of which channel(s) has caused the interrupt. More than one interrupt source may be indicated by a single interrupt request.

After the respective register has been read, EXA, and EXB are reset. All other bits will be reset after reading ISTA. To prevent malfunctions, each bit is individually monitored and reset.

MASK Register (WRITE)

	7							0	
MASK	RME	RPF	RSC	XPR	TIN	GIM	EXA	EXB	(20/60)

Value after RESET: 00H (all interrupts enabled)

Each interrupt source can be selectively masked by setting the respective bit in the MASK register (bit positions correspond to ISTA register). Masked interrupts are indicated when reading ISTA. They remain internally stored and will be indicated after the respective MASK bit is reset.

GIM … General Interrupt Mask

Channel A: If GIM is set, all active interrupts of ISTA chA are indicated but ICA is not set in the ISTA chB.

Channel B: If GIM is set, all active not-masked interrupts of both channels are indicated but the INT pin is not turned low. This feature may be used for polling procedures.

Note: In the event of an extended interrupt, no interrupt request will be generated with a masked EXA, EXB bit, although this bit is set in ISTA.

Extended Interrupt Register (READ)

	7							0	
EXIR	0	XDU	ISF	RFO	CSC	RFS	0	0	(24/64)

Value after RESET: 00H

XDU … Transmit Data Underrun

The actual frame has been aborted with IDLE, because the XFIFO holds no further data, but the frame is not yet complete!

Note: It is not possible to send frames when an XDU interrupt is indicated.

ISF … Incorrect Sync Format (significant in auto-mode only!)

The PRISM could not detect eight consecutive one's within 32 bits in BOM mode.

RFO … Receive Frame Overflow

One frame (HDCL mode) or one byte (BOM mode) could not be stored due to occupied RFIFO (i.e. a whole frame has been lost). This interrupt can be used for statistical purposes and indicates, that the CPU does not respond quickly enough to an incoming RPF or RME interrupt.

CSC … Clear To Send Status Change

Indicates, that a state transition has occured at the CTS pin. The actual state can be read from STAR register (CTS bit).

This interrupt must be enabled by setting the CIE bit in CCR2.

RFS … Receive Frame Start

This is an early receiver interrupt activated after the start of a valid frame has been detected, i.e. after a valid address check in operation modes providing address recognition, otherwise after the opening flag (transparent mode 0), delayed by two bytes.
After an RFS interrupt, the contents of

– RHCR
– RAL1
– RSTA - bit 3-0

are valid and can be read by the CPU.
This interrupt must be enabled by setting the RIE bit in CCR2.

Status Register (READ)

	7							0	
STAR	XDOV	XFW	XREP	YAL	RLI	CEC	CTS	BOM	(21/61)

Value after RESET: 48H

XDOV … Transmit Data Overflow

More than 32 bytes have been written to the XFIFO.

XFW … Transmit FIFO Write Enable

Data can be written to the XFIFO.

XREP … Transmission Repeat

Status indication of CMDR: XREP.

YAL … Yellow Alarm (significant in auto-mode only!)

Indicates the yellow alarm status.

0 ... yellow alarm off

1 ... yellow alarm on

RLI … Receive Line Inactive

Neither FLAGs as interframe time fill nor frames are received via the receive line.

Note: Significant only in point-to-point configurations!

CEC … Command Executing

0 ... No command is currently being executed, the CMDR register can be written to.

1 ... A command (written previously to CMDR) is currently being executed, no further command can be temporarily written via CMDR register.

Note: CEC will be active at most 2.5-transmit clock periods. If the PRISM is in power down mode CEC will stay active.

CTS … Clear To Send State

If the CIE bit in CCR2 is set, this bit indicates the state of the CTS pin.

0 ... CTS is inactive (high signal at CTS)

1 ... CTS is active (low signal at CTS)

BOM … Bit Oriented Message (significant in auto-mode only!)

Indicates the status of the receiver.

0 ... HDLC mode

1 ... BOM mode

Command Register (WRITE)

Value after RESET: 00H

	7							0	
CMDR	RMC	RHR	XREP	STI	XHF	XTF	XME	XRES	(21/61)

RMC … Receive Message Complete

Confirmation from CPU to PRISM, that the actual frame or data block has been fetched following an RPF or RME interrupt, thus the occupied space in the RFIFO can be released.

RHR … Reset Receiver

All data in the RFIFO and the receiver is deleted.

XREP … Transmission Repeat

Together with XTF set (write 24H or 26H to CMDR), the PRISM repeatedly transmits the contents of the XFIFO (1 ... 32 bytes) without HDLC framing fully transparent, i.e. without FLAG, CRC insertion, bit stuffing.

The cyclic transmission is stopped with an XRES command or by resetting XREP.

STI … Start Timer

The internal timer is started.

Note: The timer is stopped by rewriting the TIML register after start.

XHF … Transmit HDLC Transparent Frame

After having written up to 32 bytes to the XFIFO, this command initiates the transmission of an HDLC frame.

XTF … Transmit Transparent Frame

Initiates the transmission of a transparent frame without HDLC framing.

XME … Transmit Message End

Indicates, that the data block written last to the transmit FIFO completes the actual frame. The PRISM can terminate the transmission operation properly.

XRES … Transmit Reset

The contents of the XFIFO is deleted and IDLE is transmitted. This command can be used by the CPU to abort a frame currently in transmission. After setting XRES an XPR interrupt is generated in every case.

Note: The maximum time between writing to the CMDR register and the execution of the command is 2.5-clock cycles. Therefore, if the CPU operates with a very high clock in comparison with the PRISM's clock, it's recommended that the CEC bit of the STAR register is checked before writing to the CMDR register to avoid any loss of commands.

Mode Register (READ/WRITE)

Value after RESET: 00H

	7							0	
MODE	MDS2	MDS1	MDS0	BRM	HRAC	BRAC	TXM	TLP	(22/62)

MDS2-0 … Mode Select

The operating mode of the HDLC receiver is selected.

000 ... Reserved

001 ... Reserved

010 ... 1 byte address comparison RAL (RAL1, 2)

011 ... 2 byte address comparison (RAH1, 2, 3 and RAL1, 2)

100 ... No address comparison

101 ... 1 byte address comparison RAH (RAH1, 2, 3)
The byte following the address byte is stored in RAL1, the third byte is stored in RHCR

110 ... No HDLC framing mode 0

111 ... No HDLC framing mode 1

Note: In modes 6 and 7, the HRAC and BRAC bits must be reset to enable fully transparent reception.

BRM … BOM Receive Mode (significant in BOM mode only)

0 … 10 byte packets

1 … Continuous reception

HRAC … HDLC Receiver Active

Switches the HDCL receiver to operational or inoperational state.

0 … Receiver inactive

1 … Receiver active

In modes 6 and 7 this bit must be reset to enable fully transparent reception!

Mode Register (READ/WRITE)

Value after RESET: 00H

	7							0	
MODE	MDS2	MDS1	MDS0	BRM	HRAC	BRAC	TXM	TLP	(22/62)

MDS2-0 … Mode Select

The operating mode of the HDLC receiver is selected.

000 … Reserved

001 … Reserved

010 … 2-byte address comparison (RAH1, 2, 3 and RAL1, 2)

011 … 1-byte address comparison RAL (RAL1, 2)

100 … No address comparison

101 … 1-byte address comparison RAH (RAH1, 2, 3)

110 … No HDLC framing mode 0

111 … No HDLC framing mode 1

Note: In modes 6 and 7, the HRAC and BRAC bits must be reset to enable fully transparent reception.

BRM … BOM Receive Mode (significant in BOM mode only)

0 … 10-byte packets

1 … Continuous reception

HRAC … HDLC Receiver Active

Switches the HDCL receiver to operational or inoperational state.

0 … Receiver inactive

1 … Receiver active

In modes 6 and 7 this bit must be reset to enable fully transparent reception!

BRAC … BOM Receiver Active

Switches the BOM receiver and the yellow alarm detection mechanism to operational or inoperational state.

0 … Receiver inactive

1 … Receiver active

TXM … Transparent Transmission Mode

0 … Full transparent mode; the PRISM generates one sync-byte (FF_H) and then transmits the content of XFIFO.

1 … BOM transmission mode; a sync byte (FF_H) is generated automatically in front of every data byte.

TLP … Testloop

Input and output of the HDLC channels are internally connected. In clock mode 0 the transmit clock is used for transmission and reception.

(transmitter channel A - receiver channel A/

transmitter channel B - receiver channel B)

Timer Register Low (READ/WRITE)

	7						0	
TIML	TV7						TV0	(23/63)

TV7-0 … Timer Value, Bit 7-0

Together with bits TV11-8 of TIMH the time period t_1 is set as follows

$t_1 = 4 \times (\text{VALUE} + 1) \times \text{TCP}$

Where TCP is the period of

- transmit clock (clock mode 0)
- receive strobe (clock mode 1)
- synchronization signal (clock mode 2)

t_1 indicates the time period after which a timer interrupt will be generated.

Timer Register High (WRITE)

	7						0	
TIMH	0	0	0	TMD	TV11		TV8	(24/64)

TMD … Timer Mode

A timer interrupt is generated once after the expiration of t_1 (TMD = 0) or periodically (TMD = 1).

TV11-8 … Timer Value, bit 11-8 (higher significant bits, refer to description of TIML)

Receive Byte Count Low (READ)

	7							0	
RBCL	RBC7							RBC0	(25/65)

Together with RBCH (bits RBC11 - RBC8), the length of the actual received frame (1 … 4095 bytes) can be determined. These registers must be read by the CPU following a RME interrupt.

Receive Address Byte High Register 1 (WRITE)

	7						1	0	
RAH1	RAH1						0		(25/65)

RAH1 … Value of First Individual Programmable High Address Byte. (7 bits compared)

Bit 1 (C/R-bit) is excluded from address comparison.

Receive Address Byte High Register 2 (WRITE)

	7							0	
RAH2	RAH2								(26/66)

RAH2 … Value of Second Individual Programmable High Address Byte. (8 bits compared)

Receive Address Byte High Register 3 (WRITE)

RAH3	RAH3	(27/67)

RAH3 … Value of Third Individual Programmable High Address Byte. (8 bits compared)

Receive Status Register (READ)

	7							0	
RSTA	VFR	RDO	CRC	RAB	HAD1	HAD0	LAD	HFR	(27/67)

VFR … Valid Frame

Determines whether a valid frame has been received.

1 … Valid

0 … Invalid

An invalid frame is either

– a frame which is not an integer number of 8 bits (n × 8 bits) in length (e.g. 25 bit), or
– a frame which is too short depending on the selected operation mode via MODE (MDS2, MDS1, MDS0) as follows:

- 16-bit address check: 4 bytes
- 8-bit address check: 3 bytes
- no address check: 2 bytes

Note: Shorter frames are not reported.

RDO … Receive Data Overflow

A data overflow has occured within the actual frame.

CRC … CRC Compare/Check

0 … CRC check failed; received frame contains errors.

1 … CRC check o.k.; received frame is error-free.

RAB … Receive Message Aborted

The received frame was aborted from the transmitting station.

According to the HDLC protocol, this frame must be discarded by the CPU.

HAD1, 0 … High Byte Address Compare; significant only if 2-byte address mode has been selected.

In operating modes which provide high byte address recognition, the PRISM compares the high byte of a 2-bytes address with the contents of three individual programmable registers (RAH1, RAH2, RAH3).

00 … RAH3 recognized

10 … RAH2 recognized

01 … RAH1, C/R = 0 (bit 1)

11 … RAH1, C/R = 1 (bit 1)

LAD … Low Byte Address Compare; significant only if 2-byte or 1-byte address mode RAL has been selected.

The low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared with two individual programmable registers (RAL1, RAL2).

0 … RAL2 has been recognized

1 … RAL1 has been recognized

HFR … HDLC Frame Format

A HDLC-frame (HFR = 1) or a BOM-frame (HFR = 0) was received.

Note: RSTA7-1 is not valid with a BOM-frame (HFR = 0)

Note: RSTA corresponds to the last received HDLC frame; it is duplicated into RFIFO for every frame (last byte of frame)

Receive Address Byte Low Register 1 (READ/WRITE)

	7						0	
RAL1	RAL1							(28/68)

The general function (READ/WRITE) and the meaning or contents of this register depends on the selected operating mode:

– 2-byte/1-byte address comparison - WRITE:
  RAL1 can be programmed with the value of the first individual low address byte.

– 1-byte address comparison RAH - READ:
  RAL1 contains the byte following the high byte of the address in the receive frame (i.e. the second byte after the opening flag).

– No address comparison - READ:
  RAL1 contains the first byte after the opening flag (first byte of received frame).

– No HDLC framing - READ:
  RAL1 contains the actual data byte currently assembled at the RxD pin, by passing the HDLC receiver (fully transparent reception without HDLC framing).

Receive Address Byte Low Register 2 (WRITE)

	7						0	
RAL2	RAL2							(29/69)

Value of the second individual programmable low address byte.

Receive HDLC Control Register (READ)

	7							0	
RHCR	RHCR								(29/69)

Value of the HDLC control field of the last received frame.

Note: RHCR is duplicated into RFIFO for every frame.

Yellow Alarm Detection Register (WRITE)

Value after RESET: XXH

	7							0	
YADR	0	YDM	YV5	YV4	YV3	YV2	YV1	YV0	(2B/6B)

YDM … Yellow Alarm Detection Mode

0 … Seven out of ten

1 … Two out of two

YV5-0 … Yellow Alarm OFF-Value, Bit 5-0

The number of not-yellow-alarm indications in sequence to declare yellow alarm off are indicated.

Number = value + 1

Note: Yellow alarm is turned off by writing YADR

Channel Configuration Register 2 (READ/WRITE)

Value after RESET: 00H

The meaning of the individual bits in CCR2 depends on the selected clock mode via CCR1 as follows:

	7							0	
CCR2 clock mode 0, 1	SOC	RTS	0	0	0	CIE	RIE	DIV	(2C/6C)

CCR2 clock mode 2	SOC	RTS	XCS0	RCS0	TIO	CIE	RIE	DIV

SOC … Special Output Control

0 … Data is transmitted on TxD, received on RxD pin (normal case)

1 … Data is transmitted on RxD, received on TxD pin.

RTS … Request To Send

Defines the state and control of RTS pin.

0 … The RTS pin is controlled by the PRISM autonomously.

RTS is activated when a frame transmission starts and deactivated after the transmission operation is completed.

1 … The RTS pin is controlled by the CPU.

If this bit is set, the RTS pin is activated immediately and remains active till this bit is reset.

TIO … Transmit Clock Input Output Switch

0 … TxCLKB pin used as input

1 … TxCLKB pin used as output; in this case the transmit window of channel B is output.

Note: TIO may only be set in CCR2 of channel B

CIE … Clear To Send Interrupt Enable

Any state transition at the CTS input pin may cause an interrupt which is indicated in the EXIR register (CSC bit). The actual state at the CTS pin can be determined reading the CTS bit of the STAR register.

0 … Disable

1 … Enable

RIE … Receive Frame Start Interrupt Enable

When set, the RFS interrupt (via EXIR) is enabled!

DIV … Data Inversion

Data is transmitted and received inverted.

XCS0, RCS0 … Transmit/Receive Clock Shift, Bit 0

Together with bits XCS2, XCS1 (RCS2, RCS1) in TSAX (TSAR) the clock shift relative to the frame synchronization signal of the Transmit (Receive) Time Slot can be adjusted.

A clock shift of 0 … 7 bits is programmable (clock mode 2 only!)

Received Byte Count High (READ)

	7				3	0	
RBCH	0	0	0	OV	RBC11	RBC8	(2D/6D)

OV … Counter Overflow

More than 4095 bytes received!

The received frame exceeded the byte count in RBC11 … RBC0.

RBC11 … RBC8 … Receive Byte Count (most significant bits)

Together with RBCL (bits RBC7 … RBC0) the length of the received frame can be determined.

Version Status Register (READ)

	7				3	0	
VSTR	0	0	0	0	VN3	VN0	(2E/6E)

VN3 … VN0 … Version Number of Chip

0 … SAB 82520 HSCC

2 … PEB 3035 PRISM, Version 1.1

Receive Length Check Register (WRITE)

Value after RESET: 00H

	7		3	0	
RLCR	RC	RL6		RL0	(2E/6E)

RC … Receive Check (ON/OFF)

0 … Receive length check feature disabled

1 … Receive length check feature enabled

RL … Receive Length

The maximum receive length after which data reception is suspended can be programmed here. Depending on the value RL programmed via RL6 … RL0, the receive length is (RL + 1) $\times$ 32 bytes! A frame exceeding this length is treated as if it was aborted by the opposite station (RME Interrupt, RAB bit set).

In this case, the Receive Byte Count (RBCH, RBCL) is greater than the programmed receive length.

Channel Configuration Register 1 (READ/WRITE)

Value after RESET: 00H

	7							0	
CCR1	PU	0	ITM	ODS	IT1	IT0	CM1	CM0	(2F/6F)

PU … Switches between Power Up and Power Down Mode

0 … Power down (standby)

1 … Power up (active)

ITM … Interframe Timefill Mode

Interframe timefill according HDLC (ITM = 0) or BOM format (ITM = 1).

ODS … Output Driver Select

Defines the function of the transmit data pins (TxDA, TxDB)

0 … TxD pins are open drain outputs

1 … TxD pins are push-pull outputs

IT1/IT0 … Interframe Timefill

Depending on the selected interframe timefill mode, the following interframe timefill sequences may be selected:

- HDLC-mode (ITM = 0)
  00 … continuous idle sequences (TxD pin remains in the '1' state)
  10 … continuous flag sequences (0111 1110 bit patterns)
  01 … idle sequences, every frame is started with a preamble of 32 flags
  11 … flag sequences, at least 32 flags are transmitted between two frames
  Note: RTS-pin goes low (active) during transmission of a preamble.

- BOM mode (ITM = 1) (leftmost bit transmitted first)
  00 … 11111111 00000000 bit patterns (yellow alarm)
  01 … 11111111 00111000 bit patterns
  10 … 11111111 00110100 bit patterns
  11 … 11111111 00101100 bit patterns

CM1, CM0 … Clock Mode

Selects one of the 3 different clock modes

00 … Clock mode 0

01 … Clock mode 1

10 … Clock mode 2

Time-Slot Assignment Register Transmit (WRITE)

This register is only used in clock mode 2!

	7	2	1	0	
TSAX	TSNX		XCS2	XCS1	(30/70)

TSNX … Time-Slot Number Transmit

Selects one of up to 64 possible time slots (00H-3FH) in which data is transmitted. The number of bits per time slot can be programmed via XCCR.

XCS2, XCS1 … Transmit Clock Shift, Bit 2-1

Together with bit XCS0 in CCR2, the transmit clock shift can be adjusted.

Time-Slot Assignment Register Receive (WRITE)

This register is only used in clock mode 2!

	7	0		
TSAR	TSNR	RCS2	RCS1	(31/71)

TSNR … Time-Slot Number Receive

Defines one of up to 64 possible time slots (00H-3FH) in which data is received. The number of bits per time slot can be programmed via RCCR.

RCS2, RCS1 … Receive Clock Shift, Bit 2-1

Together with bit RCS0 in CCR2, the receive clock shift can be adjusted.

Transmit Channel Capacity Register (WRITE)

Value after RESET: 00H

This register is only used in clock mode 2!

	7		0	
XCCR	XBC7		XBC0	(32/72)

XBC7 … XBC0 … Transmit Bit Count, Bit 7-0

Defines the number of bits to be transmitted with a time slot:

Number of bits = XBC + 1. (1 … 256 bits/time slot).

Receive Channel Capacity Register (WRITE)

Value after RESET: 00H

This register is only used in clock mode 2!

	7		0	
RCCR	RBC7		RBC0	(33/73)

RBC7 … RBC0 … Receive Bit Count, Bit 7-0

Defines the number of bits to be received within a time slot:

Number of bits = RBC + 1. (1 … 256 bits/time slot).

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	0 to 85	˚C
Storage temperature	T_{stg}	– 65 to 125	˚C
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V
Maximum voltage on any pin	V_S	6	V

DC Characteristics

T_A = 0 to 85 ˚C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V

Parameter		Symbol	Limit Values		Unit	Test Condition
			min.	max.		
Input low voltage		V_{IL}	– 0.4	0.8	V	
Input high voltage		V_{IH}	2.0	V_{DD} + 0.4	V	
Output low voltage		V_{OL}		0.45	V	I_{OL} = 7 mA (pins TxD, RxD) I_{OL} = 2 mA (all other)
Output high voltage		V_{OH}	2.4		V	I_{OH} = – 400 µA
Output high voltage		V_{OH}	V_{DD} – 0.5		V	I_{OH} = – 100 µA
Power supply current	operational	I_{CC}		8	mA	V_{DD} = 5 V Inputs at 0 V/V_{DD} no output loads
	power down			1.5	mA	
Input leakage current		I_{LI}		10 µA		0 V < V_{IN} < V_{DD} to 0 V
Output leakage current		I_{LO}				0 V < V_{OUT} < V_{DD} to 0 V

Capacitance

T_A = 25 ˚C, V_{DD} = 5 V ± 5 %, V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		typ.	max.		
Input capacitance	C_{IN}	5	10	pF	
Output capacitance	C_{OUT}	8	15	pF	
I/O	C_{IO}	10	20	pF	

AC Characteristics

T_A = 0 to 85 ˚C, V_{DD} = 5 V ± 5 %

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and at 0.8 V for a logical "0".

The AC testing input/output waveforms are shown below.

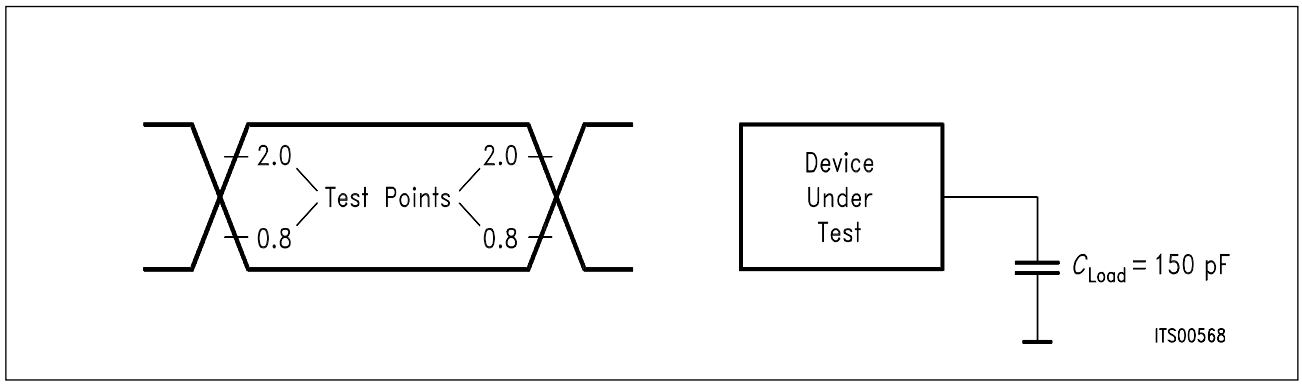

Figure 16
Input/Output Waveform for AC Tests

Microcontroller Interface Timing

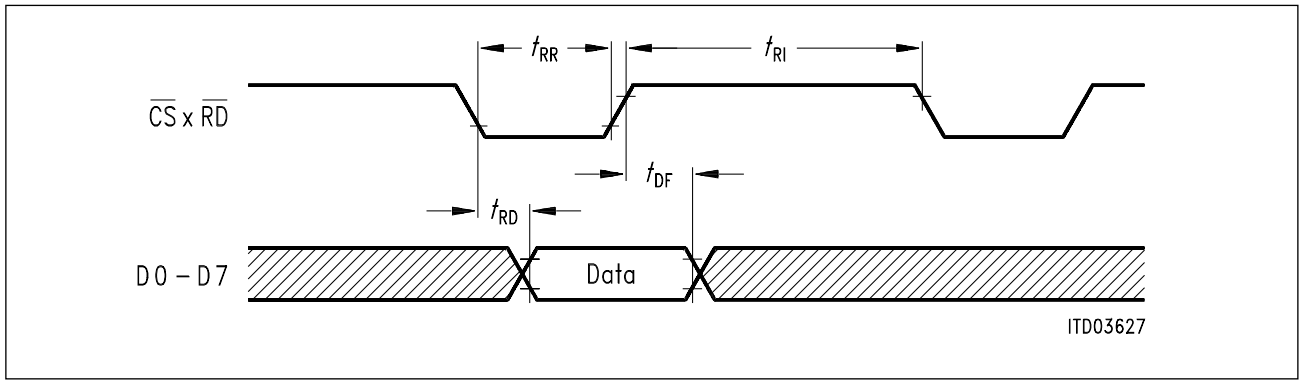

Figure 17
µP Read Cycle

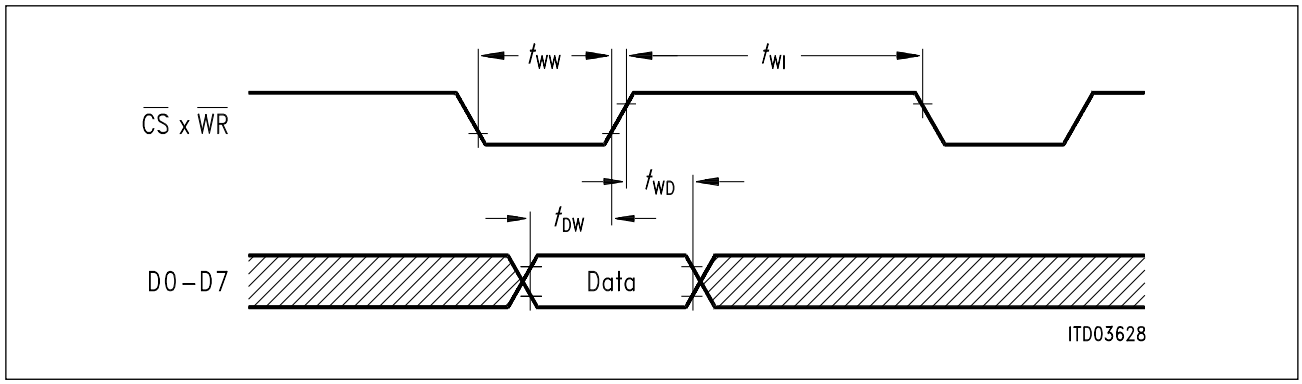

Figure 18
µP Write Cycle

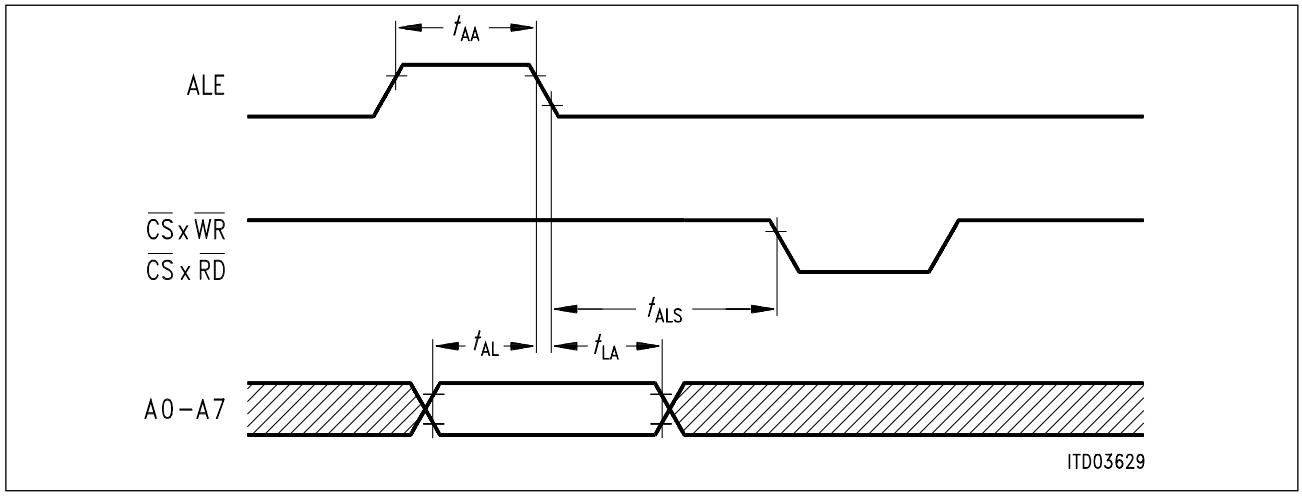

Figure 19
Multiplexed Address Timing

Parameter and Values of the Bus Modes

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{AA}	45		ns
Address set-up time to ALE	t_{AL}	11		ns
Address hold time from ALE	t_{LA}	11		ns
Address latch set-up time WR, RD	t_{ALS}	0		ns
$\overline{RD}$ pulse width	t_{RR}	120		ns
Data output delay from $\overline{RD}$	t_{RD}		120	ns
Data float delay from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	60		ns
$\overline{WR}$ pulse width	t_{WW}	60		ns
Data set-up time to $\overline{WR}$ + $\overline{CS}$	t_{DW}	30		ns
Data hold time from $\overline{WR}$ + $\overline{CS}$	t_{WD}	10		ns
$\overline{WR}$ control interval	t_{WI}	60		ns

Serial Interface Timing

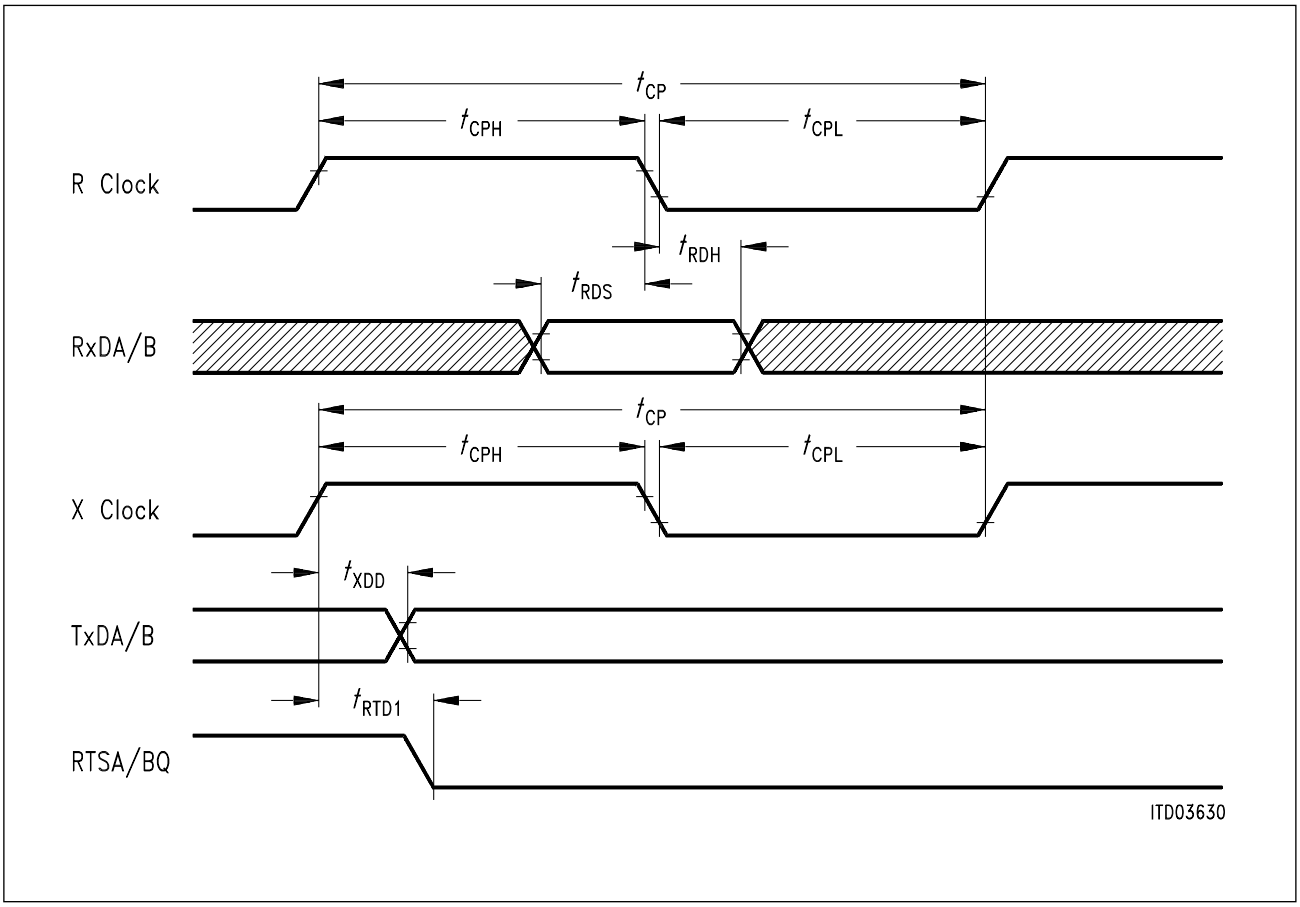

Figure 20
Serial Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Receive data set-up	t_{RDS}	20		ns
Receive data hold	t_{RDH}	5		ns
Transmit data delay	t_{XDD}	20	85	ns
Request to send delay 1	t_{RTD1}	30	120	ns
Clock period	t_{CP}	240		ns
Clock period Low	t_{CPL}	90		ns
Clock period High	t_{CPH}	90		ns

Clock Mode 1

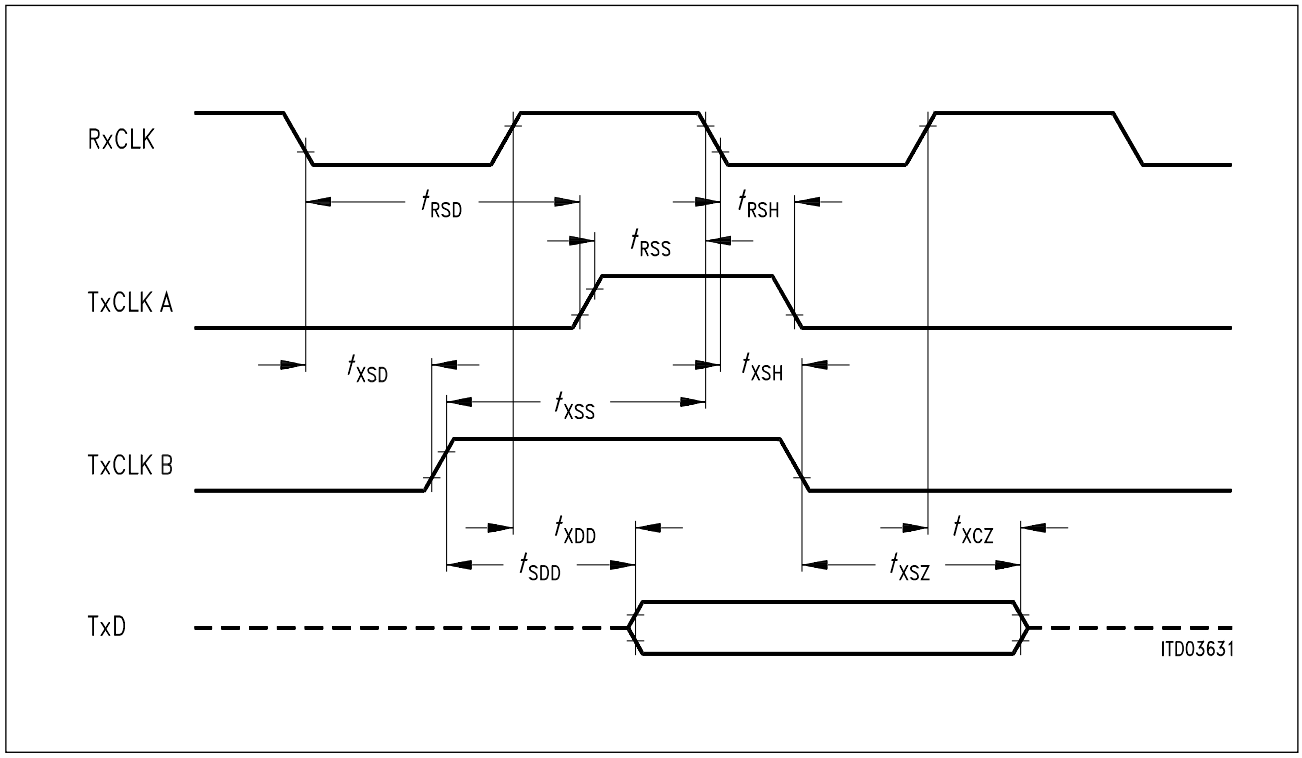

Figure 21
Strobe Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Receive strobe delay	t_{RSD}	30		ns
Receive strobe set-up	t_{RSS}	60		ns
Receive strobe hold	t_{RSH}	30		ns
Transmit strobe delay	t_{XSD}	30		ns
Transmit strobe set-up	t_{XSS}	60		ns
Transmit strobe hold	t_{XSH}	30		ns
Transmit data delay	t_{XDD}		85	ns
Strobe data delay	t_{SDD}		90	ns
High impedance from clock	t_{XCZ}		50	ns
High impedance from strobe	t_{XSZ}		50	ns

Clock Mode 2

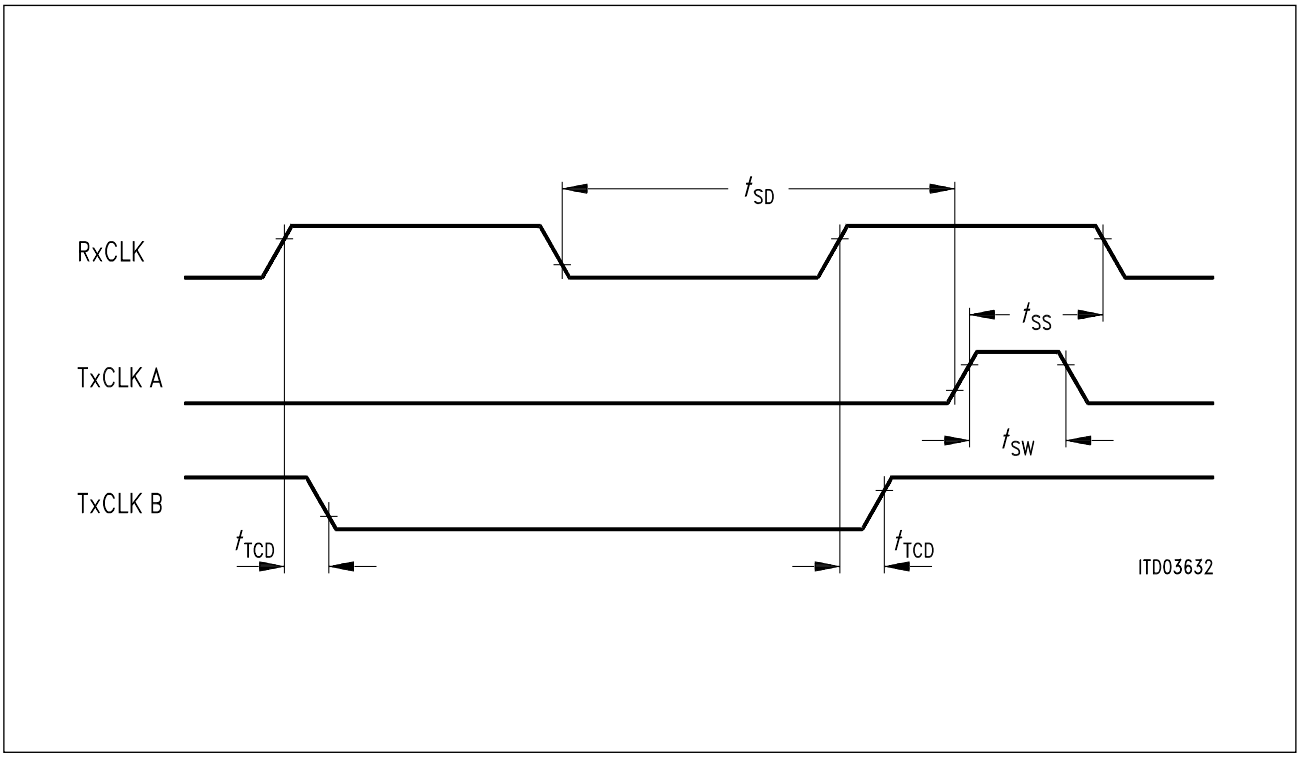

Figure 22
Synchronization Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Sync pulse delay	t_{SD}	30		ns
Sync pulse set-up	t_{SS}	30		ns
Sync pulse width	t_{SW}	40		ns
Time slot control delay	t_{TCD}	20	85	ns

Reset Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
RES high	t_{RWH}	1800		ns