FAIRCHILD

SEMICONDUCTOR™

MM74HC4316
Quad Analog Switch with Level Translator

General Description

The MM74HC4316 devices are digitally controlled analog switches implemented in advanced silicon-gate CMOS technology. These switches have low "ON" resistance and low "OFF" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Three supply pins are provided on the MM74HC4316 to implement a level translator which enables this circuit to operate with 0–6V logic levels and up to ±6V analog switch levels. The MM74HC4316 also has a common enable input in addition to each switch's control which when HIGH will disable all switches to their OFF state. All analog inputs and outputs and digital inputs are protected from electro-static damage by diodes to V_{CC} and ground.

Features

- Typical switch enable time: 20 ns
- Wide analog input voltage range: ±6V
- Low "ON" resistance:
  50 typ. ($V_{CC}-V_{EE} = 4.5V$) 30 typ. ($V_{CC}-V_{EE} = 9V$)
- Low quiescent current: 80 μA maximum (74HC)
- Matched switch characteristics
- Individual switch controls plus a common enable

Ordering Code:

| Order Number	Package Number	Package Description
MM74HC4316M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
MM74HC4316SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4316MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC4316N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram
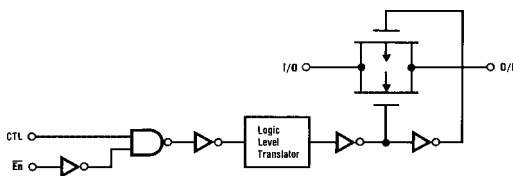
Connection Diagram

Top View
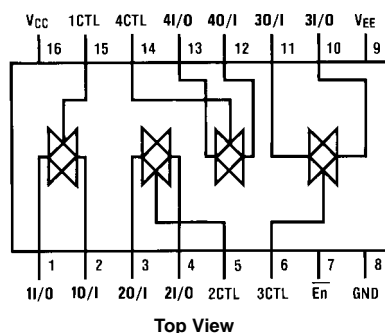
Truth Table

Inputs		Switch
$\overline{En}$	CTL	I/O–O/I
H	X	"OFF"
L	L	"OFF"
L	H	"ON"

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Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.5V
Supply Voltage (V_{EE})	+0.5 to −7.5V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Switch I/O Voltage (V_{IO})	V_{EE}−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
Supply Voltage (V_{EE})	0	−6	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns
V_{CC} = 12.0V		250	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: − 12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A = 25°C		T_A = −40 to 85°C	T_A = −55 to 125°C	Units
					Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level			2.0V		1.5	1.5	1.5	V
	Input Voltage			4.5V		3.15	3.15	3.15	V
				6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum LOW Level			2.0V		0.5	0.5	0.5	V
	Input Voltage			4.5V		1.35	1.35	1.35	V
				6.0V		1.8	1.8	1.8	V
R_{ON}	Minimum "ON" Resistance	V_{CTL} = V_{IH}, I_S = 2.0 mA	GND	4.5V	100	170	200	220	Ω
	(Note 5)	V_{IS} = V_{CC} to V_{EE}	−4.5V	4.5V	40	85	105	110	Ω
		(Figure 1)	−6.0V	6.0V	30	70	85	90	Ω
			GND	2.0V	100	180	215	240	Ω
		V_{CTL} = V_{IH}, I_S = 2.0 mA	GND	4.5V	40	80	100	120	Ω
		V_{IS} = V_{CC} or V_{EE}	−4.5V	4.5V	50	60	75	80	Ω
		(Figure 1)	−6.0V	6.0V	20	40	60	70	Ω
R_{ON}	Maximum "ON" Resistance	V_{CTL} = V_{IH}	GND	4.5V	10	15	20	20	Ω
	Matching	V_{IS} = V_{CC} to V_{EE}	−4.5V	4.5V	5	10	15	15	Ω
			−6.0V	6.0V	5	10	15	15	Ω
I_{IN}	Maximum Control	V_{IN} = V_{CC} or GND	GND	6.0V		±0.1	±1.0	±1.0	μA
	Input Current								
I_{IZ}	Maximum Switch "OFF"	V_{OS} = V_{CC} or V_{EE}	GND	6.0V		±60	±600	±600	nA
	Leakage Current	V_{IS} = V_{EE} or V_{CC}	−6.0V	6.0V		±100	±1000	±1000	nA
		V_{CTL} = V_{IL} (Figure 2)							
I_{IZ}	Maximum Switch "ON"	V_{IS} = V_{CC} to V_{EE}	GND	6.0V		±40	±150	±150	nA
	Leakage Current	V_{CTL} = V_{IH}, V_{OS} = OPEN	−6.0V	6.0V		±60	±300	±300	nA
		(Figure 3)							
I_{CC}	Maximum Quiescent	V_{IN} = V_{CC} or GND	GND	6.0V		2.0	20	40	μA
	Supply Current	I_{OUT} = 0 μA	−6.0V	6.0V		8.0	80	160	μA

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages (V_{CC}–V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

$V_{CC} = 2.0V–6.0V$, $V_{EE} = 0V–6V$, $C_L = 50$ pF (unless otherwise specified)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	$T_A = +25°C$ Typ	$T_A = +25°C$	$T_A = -40°C$ to $+85°C$	$T_A = -55°C$ to $+125°C$	Units
						Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		GND	2.0V	25	50	63	75	ns
			GND	4.5V	5	10	13	15	ns
			−4.5V	4.5V	4	8	12	14	ns
			−6.0V	6.0V	3	7	11	13	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay (Control)	$R_L = 1$ kΩ	GND	2.0V	30	165	206	250	ns
			GND	4.5V	20	35	43	53	ns
			−4.5V	4.5V	15	32	39	48	ns
			−6.0V	6.0V	14	30	37	45	ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay (Control)	$R_L = 1$ kΩ	GND	2.0V	45	250	312	375	ns
			GND	4.5V	25	50	63	75	ns
			−4.5V	4.5V	20	44	55	66	ns
			−6.0V	6.0V	20	44	55	66	
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay (Enable)		GND	2.0V	35	205	256	308	ns
			GND	4.5V	20	41	52	62	ns
			−4.5V	4.5V	19	38	48	57	ns
			−6.0V	6.0V	18	36	45	54	ns
t_{PLZ}, t_{PHZ}	Maximum Switch Turn "OFF" Delay (Enable)		GND	2.0V	58	265	330	400	ns
			GND	4.5V	28	53	67	79	ns
			−4.5V	4.5V	23	47	59	70	ns
			−6.0V	6.0V	21	47	59	70	ns
f_{MAX}	Minimum Frequency Response (Figure 7) 20 log $(V_{OS}/V_{IS})= -3$ dB	$R_L = 600\Omega$, $V_{IS} = 2V_{PP}$ at $(V_{CC}-V_{EE}/2)$ (Note 6) (Note 7)	0V	4.5	40				MHz
			−4.5V	4.5V	100				MHz
	Control to Switch Feedthrough Noise (Figure 8)	$R_L = 600\Omega$, F = 1 MHz $C_L = 50$ pF (Note 7) (Note 8)	0V	4.5V	100				mV
			−4.5V	4.5V	250				mV
	Crosstalk Between any Two Switches (Figure 9)	$R_L = 600\Omega$, F = 1 MHz	0V	4.5V	−52				dB
			−4.5V	4.5V	−50				dB
	Switch OFF Signal Feedthrough Isolation (Figure 10)	$R_L = 600\Omega$, F = 1 MHz $V_{CTL} = V_{IL}$, (Note 7) (Note 8)	0V	4.5V	−42				dB
			−4.5V	4.5V	−44				dB
THD	Sinewave Harmonic Distortion (Figure 11)	$R_L = 10$ KΩ, $C_L = 50$ pF, F = 1 KHz							
		$V_{IS} = 4V_{PP}$	0V	4.5V	0.013				%
		$V_{IS} = 8V_{PP}$	−4.5V	4.5V	0.008				%
C_{IN}	Maximum Control Input Capacitance				5				pF
C_{IN}	Maximum Switch Input Capacitance				35				pF
C_{IN}	Maximum Feedthrough Capacitance	$V_{CTL} = $ GND			0.5				pF
C_{PD}	Power Dissipation Capacitance				15				pF

Note 6: Adjust 0 dBm for F = 1 KHz (Null R_L/Ron Attenuation).

Note 7: V_{IS} is centered at $V_{CC}-V_{EE}/2$.

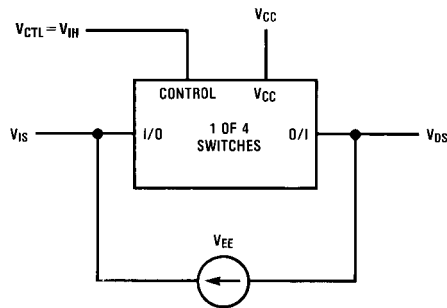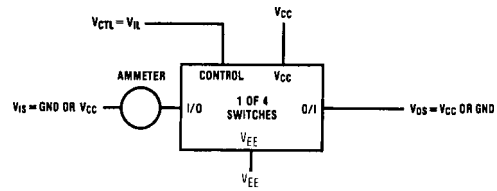**Note 8:** Adjust for 0 dBm.

AC Test Circuits and Switching Time Waveforms

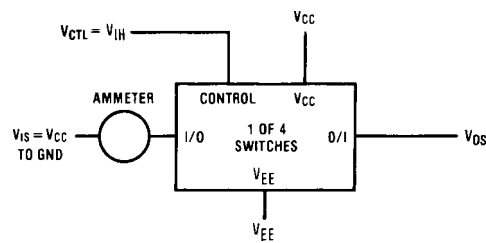FIGURE 1. "ON" Resistance
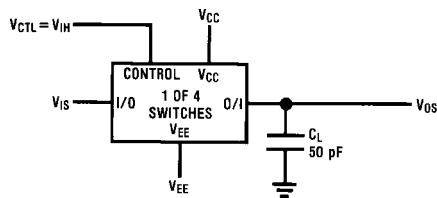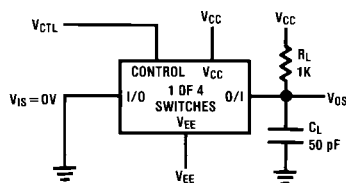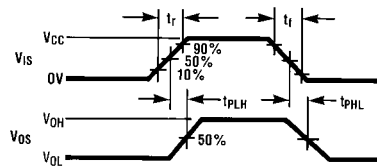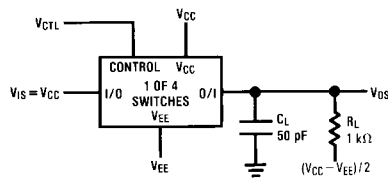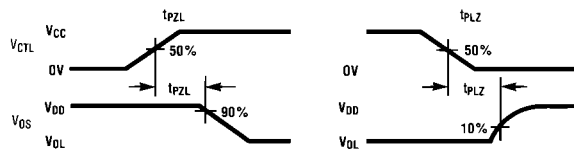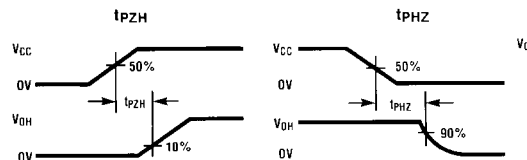
FIGURE 2. "OFF" Channel Leakage Current

FIGURE 3. "ON" Channel Leakage Current

FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

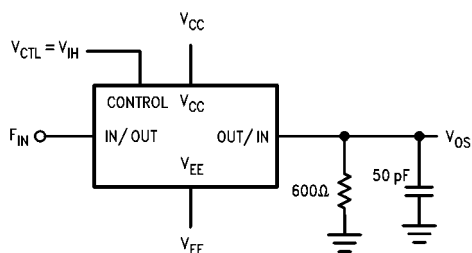# AC Test Circuits and Switching Time Waveforms (Continued)
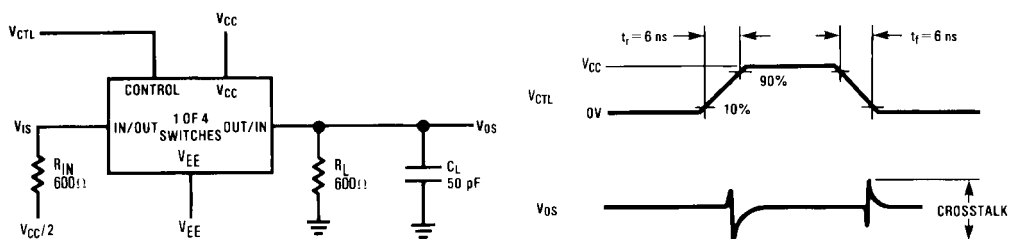

FIGURE 7. Frequency Response
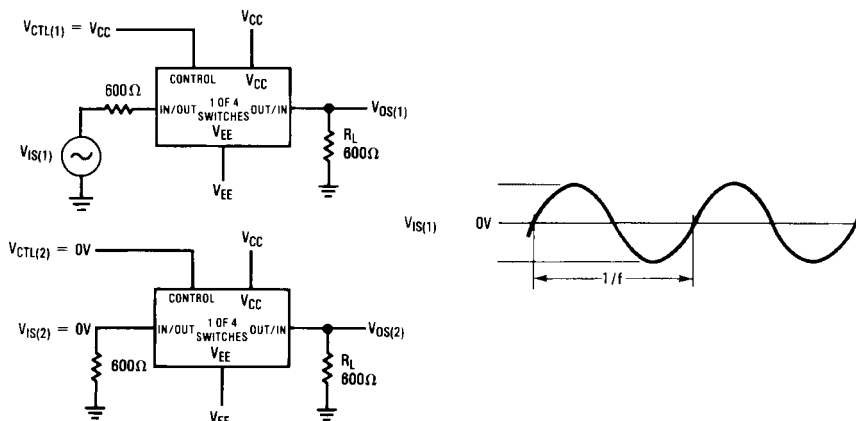

FIGURE 8. Crosstalk: Control Input to Signal Output

FIGURE 9. : Crosstalk Between Any Two Switches

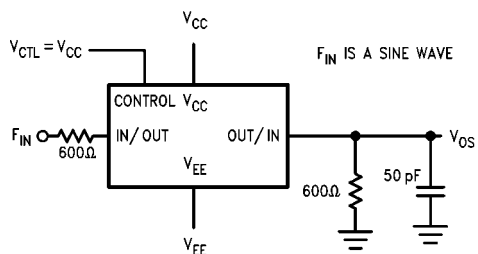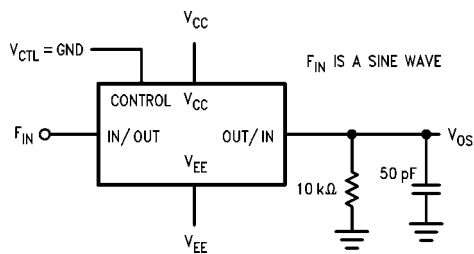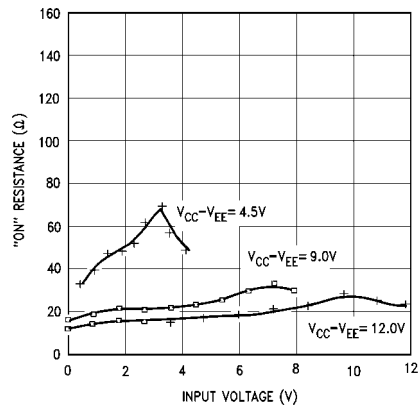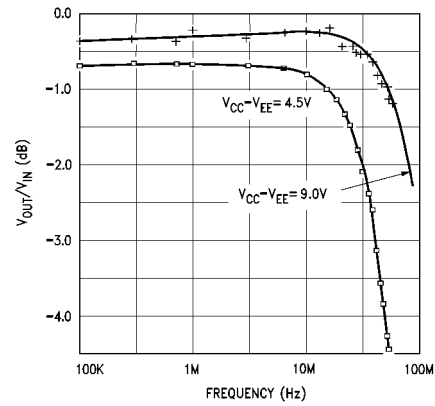FIGURE 10. Switch OFF Signal Feedthrough Isolation

FIGURE 11. Sinewave Distortion

Typical Performance Characteristics

Typical "ON" Resistance

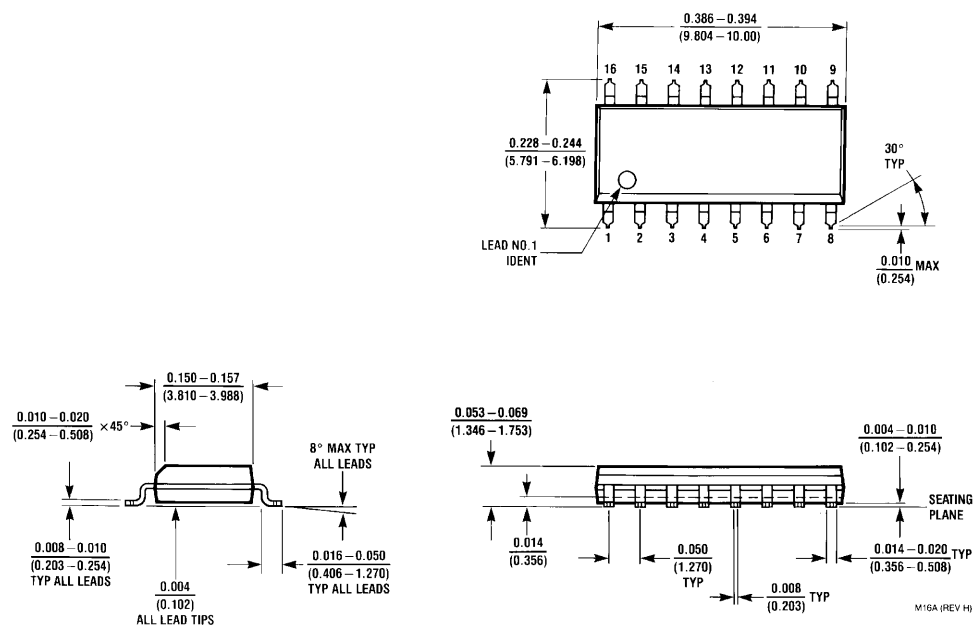**Typical Crosstalk Between Any Two Switches**
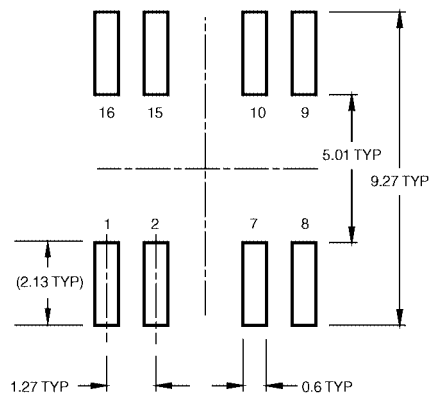

Typical Frequency Response
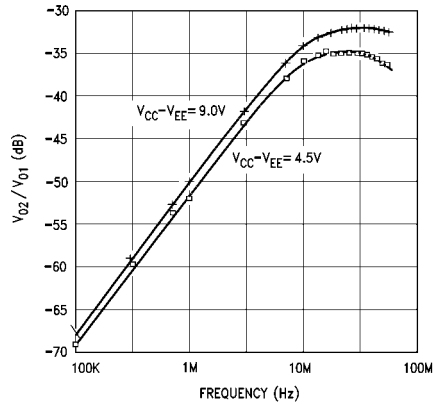
Special Considerations

In certain applications the external load-resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the analog switch input pins, the voltage drop across the switch must not exceed 0.6V (calculated from the On Resistance).

Physical Dimensions inches (millimeters) unless otherwise noted

0.386 − 0.394
(9.804 − 10.00)

16 15 14 13 12 11 10 9

0.228 − 0.244
(5.791 − 6.198)

30°
TYP

LEAD NO.1
IDENT

1   2   3   4   5   6   7   8

0.010 MAX
(0.254)

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) ×45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP

0.014 − 0.020
(0.356 − 0.508) TYP

M16A (REV H)

16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

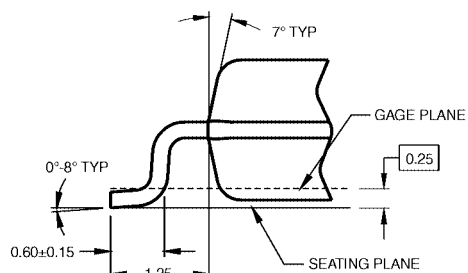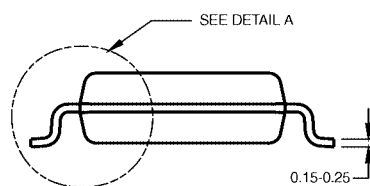## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

10.2±0.1
-A-

0.47 TYP

16   9

7.8

3.9

5.3±0.1
-B-

⌒ 0.2 C B A
ALL LEAD TIPS

PIN #1 IDENT.

1   8

16   15   10   9

5.01 TYP

9.27 TYP

(2.13 TYP)

1   2   7   8

1.27 TYP   0.6 TYP

LAND PATTERN RECOMMENDATION

ALL LEAD TIPS
⌒ 0.1 C

2.1 MAX.

1.8±0.1

-C-

1.27 TYP

0.15±0.05

0.35-0.51
⊕ 0.12 Ⓜ C A

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.15-0.25

7° TYP

GAGE PLANE
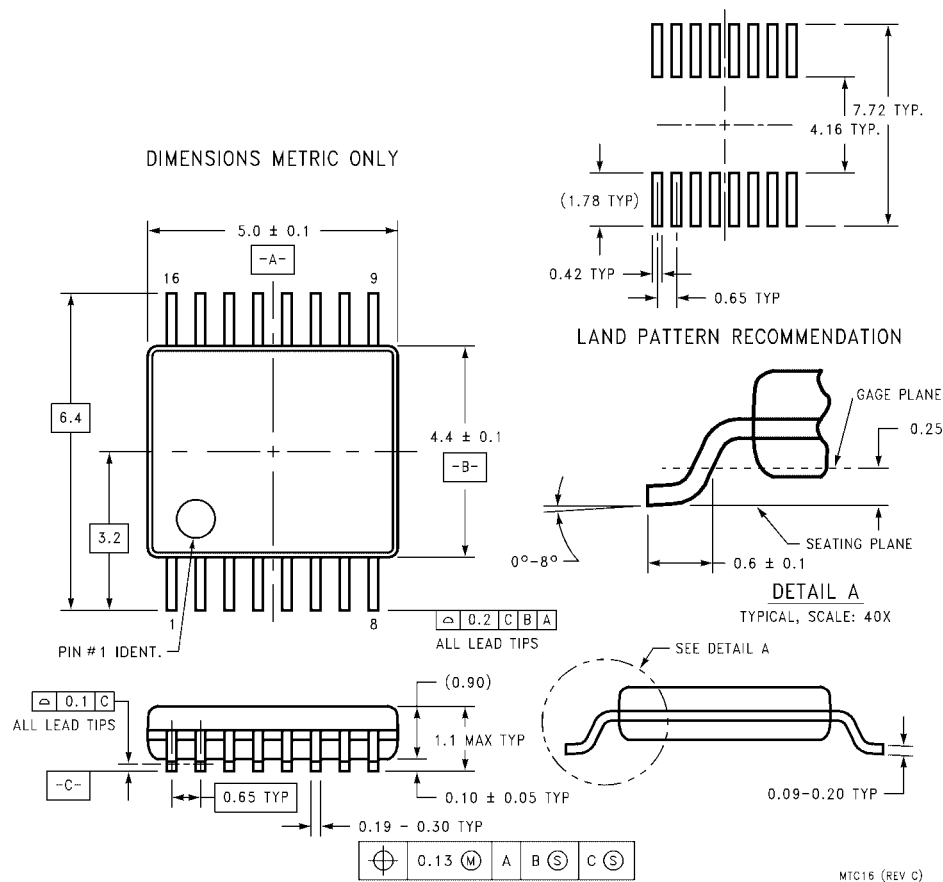
0.25

0°-8° TYP

0.60±0.15

1.25

SEATING PLANE
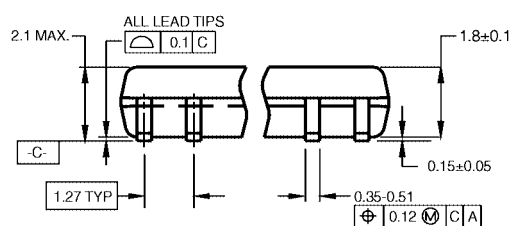
DETAIL A

NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
   ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
   FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS METRIC ONLY

7.72 TYP.

4.16 TYP.

(1.78 TYP)

0.42 TYP

0.65 TYP

LAND PATTERN RECOMMENDATION

5.0 ± 0.1

-A-

16   9

6.4

4.4 ± 0.1

-B-

3.2

1   8

| △ | 0.2 | C | B | A |

ALL LEAD TIPS

PIN #1 IDENT.

| △ | 0.1 | C |

ALL LEAD TIPS

-C-

0.65 TYP

0.19 - 0.30 TYP

(0.90)

1.1 MAX TYP

0.10 ± 0.05 TYP

| ⊕ | 0.13 Ⓜ | A | B Ⓢ | C Ⓢ |

GAGE PLANE

0.25

0°-8°

SEATING PLANE

0.6 ± 0.1

DETAIL A
TYPICAL, SCALE: 40X

SEE DETAIL A

0.09-0.20 TYP

MTC16 (REV C)

16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)
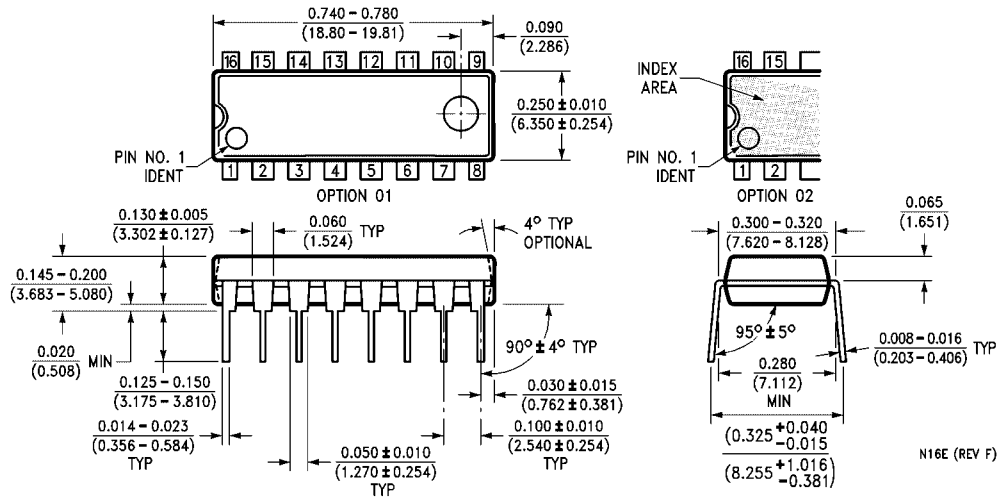
16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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MM74HC4316M   MM74HC4316MTC   MM74HC4316N_Q   MM74HC4316WM_Q   MM74HC4316M_Q
MM74HC4316MTC_Q