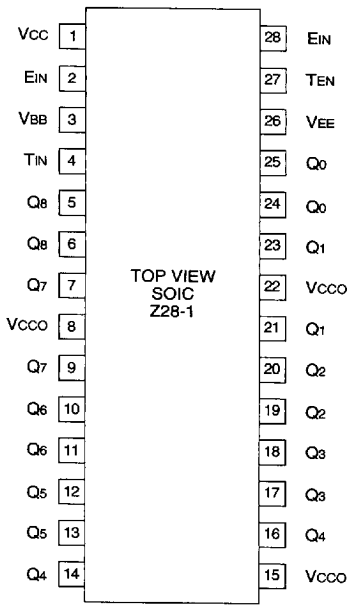
FEATURES

- **PECL version of popular ECLinPS E111**
- **Low skew**
- **Guaranteed skew spec**
- **VBB output**
- **TTL enable input**
- **Selectable TTL or PECL clock input**
- **Single +5V supply**
- **Differential internal design**
- **Similar pin configuration to E111**
- **PECL I/O fully compatible with industry standard**
- **Internal 75KΩ PECL input pull-down resistors**
- **ESD protection of 2000V**

PIN CONFIGURATION



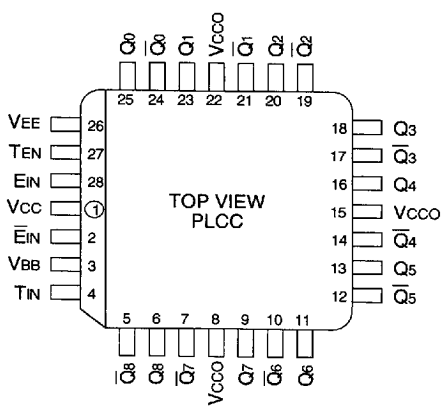
DESCRIPTION

The SY100S811 is a low skew 1-to-9 PECL differential driver designed for clock distribution in new, high-performance PECL systems. It accepts either a PECL clock input or a TTL input by using the TTL enable pin TEN. When the TTL enable pin is HIGH, the TTL input is enabled and the PECL input is disabled. When the enable pin is set LOW, the TTL input is disabled and the PECL input is enabled.

The device is specifically designed and produced for low skew. The interconnect scheme and metal layout are carefully optimized for minimal gate-to-gate skew within the device. Wafer characterization and process control ensure consistent distribution of propagation delay from lot to lot. Since the S811 shares a common set of "basic" processing with the other members of the ECLinPS family, wafer characterization at the point of device personalization allows for tighter control of parameters, including propagation delay.

To ensure that the skew specification is met, it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and, therefore, terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i.e. sharing the same VCCO as the pair(s) being used on that side) in order to maintain minimum skew.

The VBB output is intended for use as a reference voltage for single-ended reception of PECL signals to that device only. When using VBB for this purpose, it is recommended that VBB is decoupled to VCC via a 0.01µF capacitor.



7

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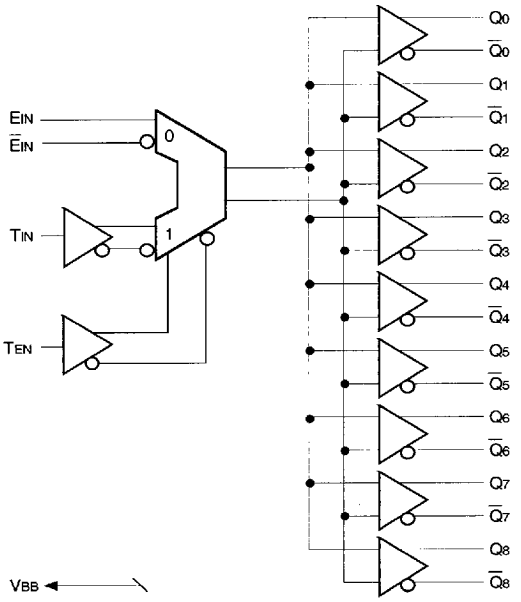
BLOCK DIAGRAM



TRUTH TABLE

TEN	EIN	TIN	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

PIN NAMES

Pin	Function
EIN, $\overline{E_{IN}}$	Differential PECL Input Pair
TIN	TTL Input
TEN	TTL Input Enable
Q0, $\overline{Q_0}$ – $\overline{Q_8}$, Q8	Differential PECL Outputs
VBB	VBB Output
VCC	PECL VCC (+5.0V)
VEE	PECL Ground (0V)

PECL DC ELECTRICAL CHARACTERISTICS

VCC = VCCO = +5.0V ± 5%

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
VBB	Output Reference Voltage	3.62	—	3.74	3.62	—	3.74	3.62	—	3.74	V	VCC = VCCO = 5.0V
IIH	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
IIL	Input LOW Current	0.5	—	—	0.5	—	—	0.5	—	—	µA	—
VIH	Input HIGH Voltage	3.835	—	4.120	3.835	—	4.120	3.835	—	4.120	V	VCC = VCCO = 5.0V
VIL	Input LOW Voltage	3.190	—	3.525	3.190	—	3.525	3.190	—	3.525	V	VCC = VCCO = 5.0V
ICC	Power Supply Current	—	53	65	—	53	65	—	60	74	mA	All inputs and outputs open

TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = +5.0V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IH}	Input HIGH Voltage	2.0	—	—	2.0	—	—	2.0	—	—	V	—
V_{IL}	Input LOW Voltage	—	—	0.8	—	—	0.8	—	—	0.8	V	—
I_{IH}	Input HIGH Current	— —	— —	20 100	— —	— —	20 100	— —	— —	20 100	µA	$V_{IN} = 2.7V$ $V_{IN} = 5.0V$
I_{IL}	Input LOW Current	—	—	–0.6	—	—	–0.6	—	—	–0.6	mA	$V_{IN} = 0.5V$
V_{IK}	Input Clamp Voltage	—	—	–1.2	—	—	–1.2	—	—	–1.2	V	$I_{IN} = -18mA$

AC ELECTRICAL CHARACTERISTICS[1–6]

$V_{CC} = V_{CCO} = +5.0V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output[1] E_{IN} (differential)[2] E_{IN} (single-ended)[3] T_{IN}	 430 330 350	 — — —	 630 730 950	 430 330 350	 — — —	 630 730 950	 430 330 350	 — — —	 630 730 950	ps	
t_{skew}	Within-Device Skew[4]	—	25	50	—	25	50	—	25	50	ps	
V_{PP}	Minimum PECL Input Swing[5]	250	—	—	250	—	—	250	—	—	mV	
V_{CMR}	PECL Common Mode Range[6]	–1.6	—	–0.4	–1.6	—	–0.4	–1.6	—	–0.4	V	
t_r t_f	Output Rise/Fall Times 20% to 80%	275	375	600	275	375	600	275	375	600	ps	—

NOTES:

1. Part-to-part skew is defined as Max. — Min. value at the given temperature.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. V_{PP} (min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP} (min.) is AC limited for the S811, as a differential input as low as 50mV will still produce full PECL levels at the output.
6. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP} (min.).

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S811JC	J28-1	Commercial
SY100S811JCTR	J28-1	Commercial
SY100S811ZC	Z16-1	Commercial
SY100S811ZCTR	Z16-1	Commercial