Optimized-Efficiency Controller for RF Power Amplifier Boost Converter

FEATURES

- Si9160 architecture optimized for **"light-load"** efficiency
- High Frequency Switching (up to 2 MHz)
- Optimized Output Drive Current (300 mA)
- Standby Mode
- Wide Bandwidth Feedback Amplifier
- Single-Cell LiIon and Three-cell NiCd or NiMH Operation

DESCRIPTION

The Si9161 Optimized-Efficiency Controller for RF Power Amplifier Boost Converter is a fixed-frequency, pulse- width-modulated power conversion controller designed for use with the Si6801 application specific MOSFET. The Si9161 and the Si6801 are optimized for high efficiency switched-mode power conversion at 1 MHz and over. The device has an enable pin which can be used to put the converter in a low-current mode compatible with the standby mode of most cellular phones. It has a light-load pin which enables circuitry optimizing efficiency at loads typical of receive operation. A wide bandwidth feedback amplifier minimizes transient response time allowing the device to meet the instantaneous current demands of today's digital protocols. The input voltage range accommodates minimal size and cost battery pack configurations.

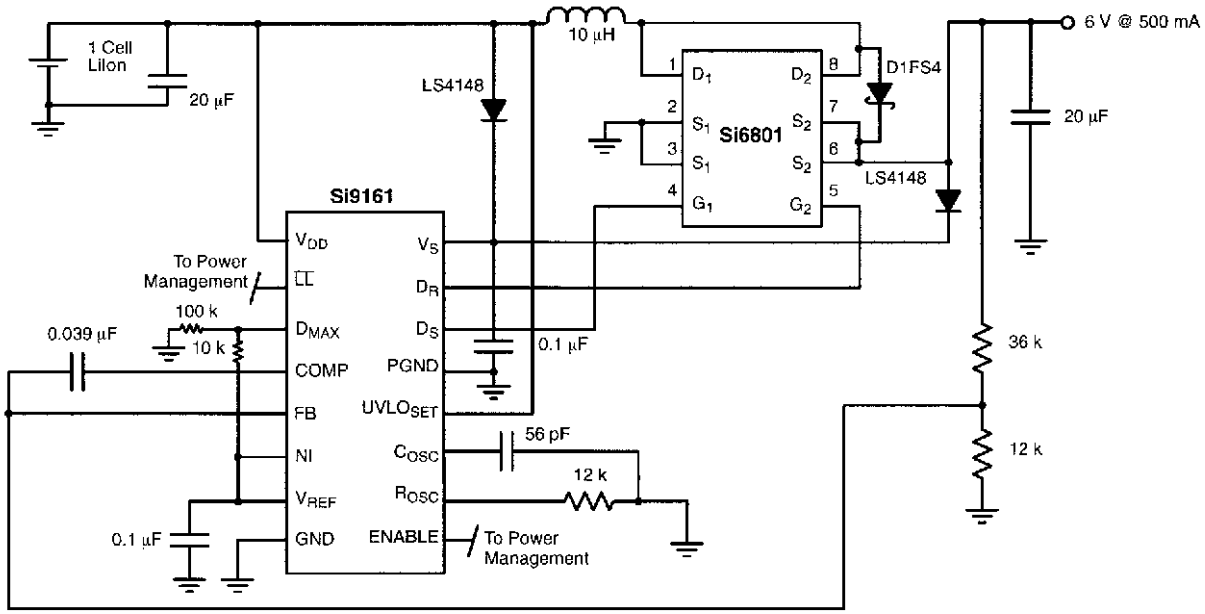
Frequency control in switching is important to noise management techniques in RF communications. The Si9161 is easily synchronized for high efficiency power conversion at frequencies in excess of 1 MHz.

Optimizing the controller and the synchronous FETs results in the highest conversion efficiency over a wide load range at the switching frequencies of interest (1 MHz or greater). It also minimizes the overshoot and gate ringing associated with drive current and gate charge mismatches.

When disabled, the converter requires less than 330 µA. This capability minimizes the impact of the converter on battery life when the phone is in the standby mode.

Finally, operating voltage is optimized for LiIon battery operation (2.7 V to 4.5 V) and can also be used with three-cell NiCd or NiMH (3 V to 3.6 V), as well as four-cell NiCd or NiMH (4 V to 4.8 V) battery packs.

APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Voltages Referenced to GND.			
V_{DD}, V_S		7	V
P_{GND}		± 0.3	
Linear Inputs		- 0.3 V to V_{DD} + 0.3 V	
Logic Inputs		- 0.3 V to V_{DD} + 0.3 V	
Peak Output Drive Current		350	mA
Storage Temperature		- 65 to 150	°C
Operating Junction Temperature		150	
Power Dissipation (Package)[a]	16-Pin TSSOP (Q Suffix)[a, b]	925	mW
Thermal Impedance (Θ_{JA})[a]	16-Pin TSSOP	135	°C/W

Notes:

a. Device Mounted with all leads soldered or welded to PC board.

a. Derate 7.4 mW/°C above 25 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified[a] $\overline{LL}$ = V_{DD}, 2.7 V ≤ V_{DD}, V_S ≤ 6.0 V, GND = P_{GND}	Limits B Suffix - 25 to 85 °C Min[b]	Typ	Max[b]	Unit
Reference						
Output Voltage	V_{REF}	I_{REF} = - 10 µA	1.455		1.545	V
		T_A = 25 °C	1.477	1.50	1.523	
Oscillator						
Maximum Frequency[c]	f_{MAX}	V_{DD} = 5 V, C_{OSC} = 47 pF, R_{OSC} = 5.0 kΩ	2.0			MHz
Oscillator Frequency Accuracy		V_{DD} = 3.0 V, f_{OSC} = 1 MHz (nominal) C_{OSC} = 100 pF, R_{OSC} = 7.0 kΩ, T_A = 25 °C	- 15		15	%
R_{OSC} Peak Voltage	V_{ROSC}			1.0		V
Voltage Stability[c]	Δf/f	4 V ≤ V_{DD} ≤ 6 V, Ref to 5 V, T_A = 25 °C	- 8		8	%
Temperature Stability[c]		Referenced to 25 °C		± 5		
Light-Load Frequency[c]	$f_{\overline{LL}}$	$\overline{LL}$ = 0 V, C_{OSC} = 100 pf, R_{OSC} = 7.0 kΩ		115		kHz
Error Amplifier (C_{OSC} = GND, OSC Disabled)						
Input Bias Current	I_B	V_{NI} = V_{REF} , V_{FB} = 1.0 V	- 1.0		1.0	µA
Open Loop Voltage Gain	A_{VOL}		47	55		dB
Offset Voltage	V_{OS}	V_{NI} = V_{REF}	- 15	0	15	mV
Unity Gain Bandwidth[c]	BW			10		MHz
Output Current	I_{OUT}	Source (V_{FB} = 1 V, NI = V_{REF})		- 2.0	- 1.0	mA
		Sink (V_{FB} = 2 V, NI = V_{REF})	0.4	0.8		
Power Supply Rejection[c]	PSRR	4 V < V_{DD} < 6 V		60		dB
$UVLO_{SET}$ Voltage Monitor						
Under Voltage Lockout	V_{UVLOHL}	$UVLO_{SET}$ High to Low	0.85	1.0	1.15	V
	V_{UVLOLH}	$UVLO_{SET}$ Low to High		1.2		
Hysteresis	V_{HYS}	V_{UVLOLH} - V_{UVLOHL}		200		mV
UVLO Input Current	$I_{UVLO(SET)}$	V_{UVLO} = 0 to V_{DD}	- 100		100	nA

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified[a] $\overline{LL}$ = V_{DD}, 2.7 V ≤ V_{DD}, V_S ≤ 6.0 V, GND = P_{GND}		Limits B Suffix - 25 to 85 °C Min[b]	Typ	Max[b]	Unit
Output Drive (D_R and D_S)							
Output High Voltage	V_{OH}	V_{DD} = 2.7 V, V_S = 5.3 V	I_{OUT} = - 10 mA	5.15	5.2		V
Output Low Voltage	V_{OL}		I_{OUT} = 10 mA		0.06	0.15	
Peak Source Output Current	I_{SOURCE}	V_{DD} = 2.7 V	V_S = 5.3 V		- 300	- 250	mA
Peak Sink Output Current	I_{SINK}		V_S = 5.3 V	250	300		
Break-Before-Make	t_{BBM}	V_{DD} = 6.0 V			40		ns
Logic							
ENABLE Delay to Output	td_{EN}	ENABLE Rising to OUTPUT, V_{DD} = 6.0 V			1.4		µs
ENABLE Logic Low	V_{ENL}					0.2 V_{DD}	V
ENABLE Logic High	V_{ENH}			0.8 V_{DD}			
ENABLE Input Current	I_{EN}	ENABLE = 0 to V_{DD}		- 1.0		1.0	µA
Light Load Delay to Output[c]	$td_{\overline{LL}}$	Light Load Falling to OUTPUTS			1.4		µs
Light Load Logic Low	$V_{\overline{LLL}}$					0.8	V
Light Load Logic High	$V_{\overline{LLH}}$			2.4			
Light Load Input Current	$I_{\overline{LL}}$	$\overline{LL}$ = 0 to V_{DD}		- 1.0		1.0	µA
Duty Cycle							
Maximum Duty Cycle	$CYCLE_{MAX}$	V_{DD} = 6.0 V			80	95	%
D_{MAX}/SS Input Current	I_{DMAX}	D_{MAX} = 0 to V_{DD}		- 100		100	nA
Supply							
Supply Current-Normal Mode	I_{DD}	No Load, V_{LL} = 0 to V_{DD}, f_{OSC} = 1 MHz, R_{OSC} = 7.0 kΩ	V_{DD} = 2.7 V		1.1	1.5	mA
			V_{DD} = 4.5 V		1.6	2.3	
Supply Current-Standby Mode		ENABLE = Low			250	330	µA

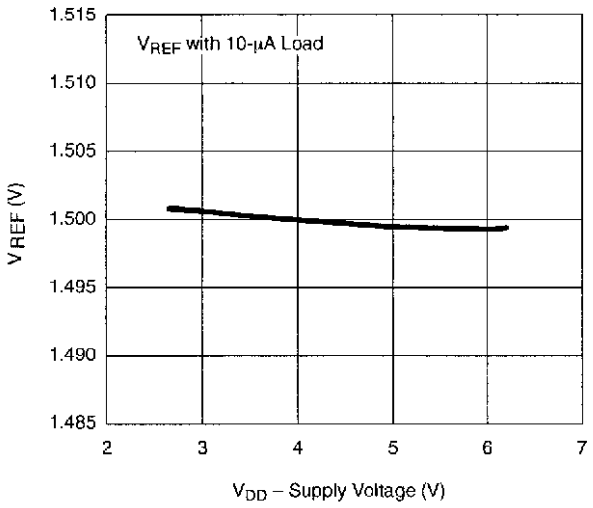
Notes:

a. C_{STRAY} < 5 pF on C_{OSC}. After Start-Up, V_{DD} of ≥ 3 V.

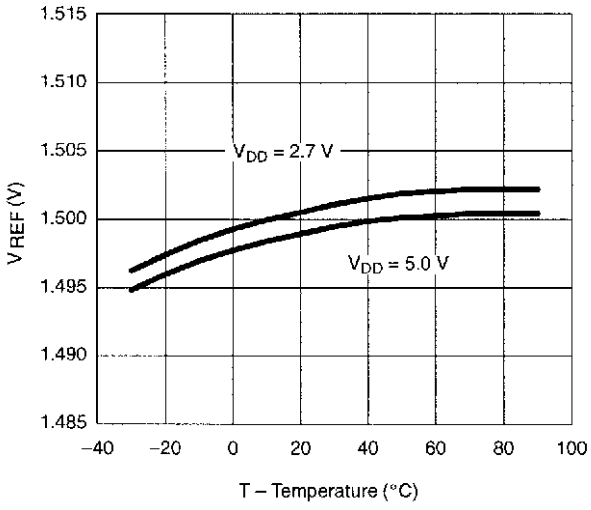
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

c. Guaranteed by design, not subject to production testing.

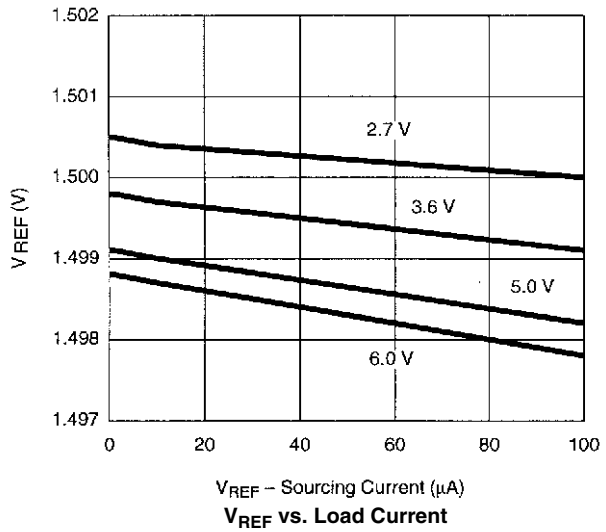
TYPICAL CHARACTERISTICS $\overline{LL}$ = V_{DD}, 25 °C, unless otherwise noted



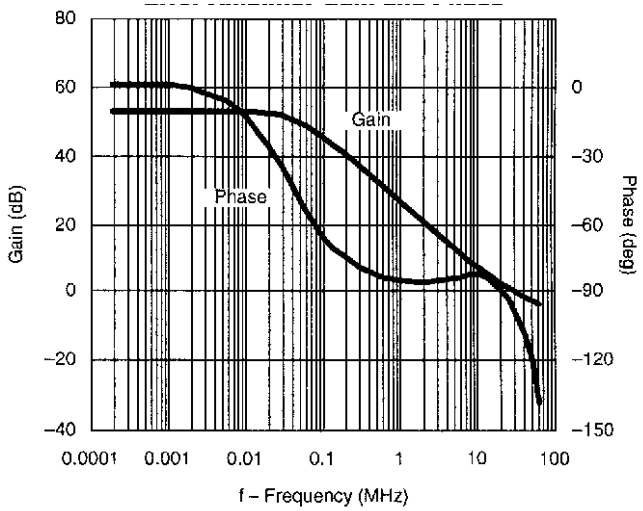
V_{REF} vs. Supply Voltage



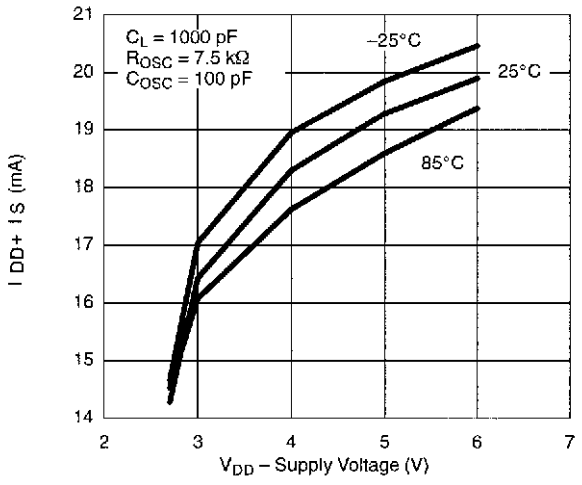
V_{REF} vs. Temperature



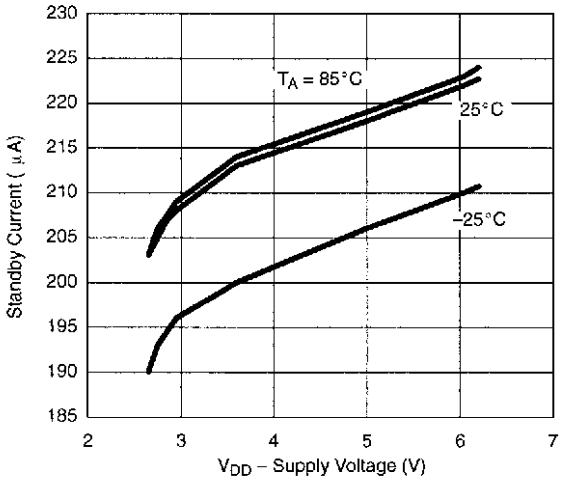
V_{REF} vs. Load Current



Error Amplifier Gain and Phase

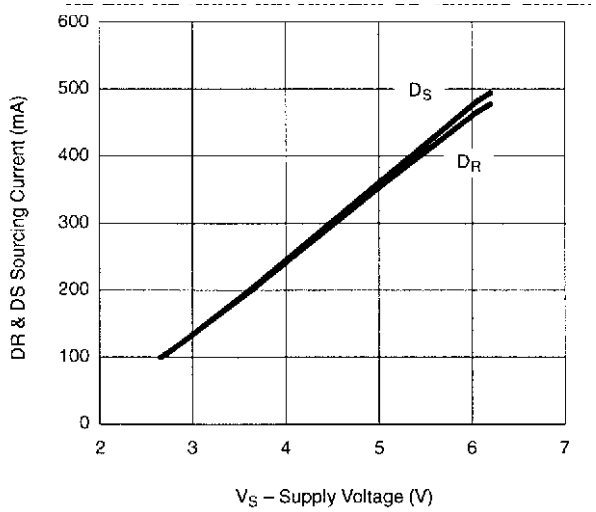


Supply Current vs. Supply Voltage and Temperature

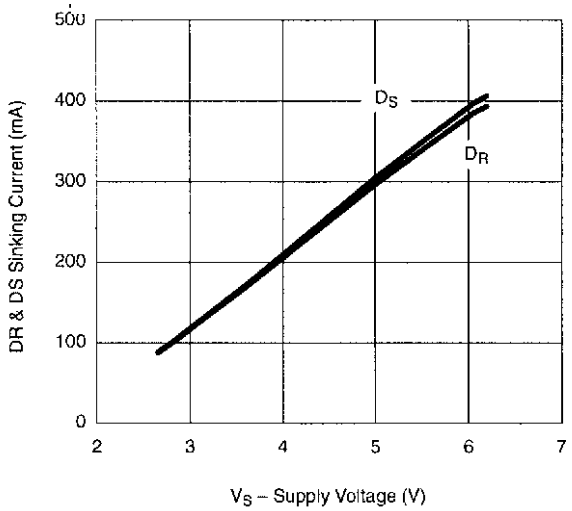


Standby Current vs. Supply Voltage and Temperature

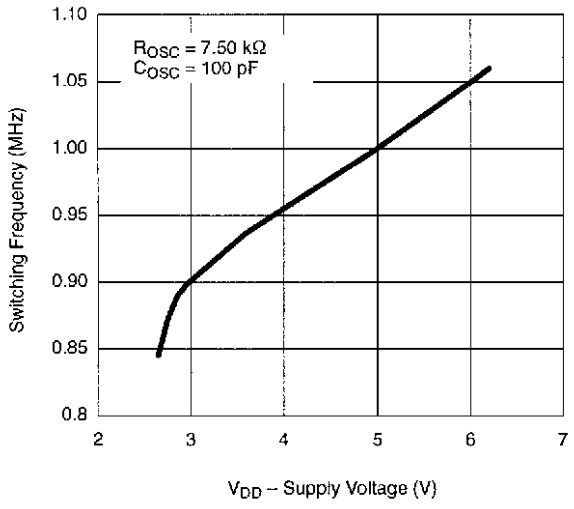
TYPICAL CHARACTERISTICS $\overline{LL}$ = V_{DD}, 25 °C, unless otherwise noted



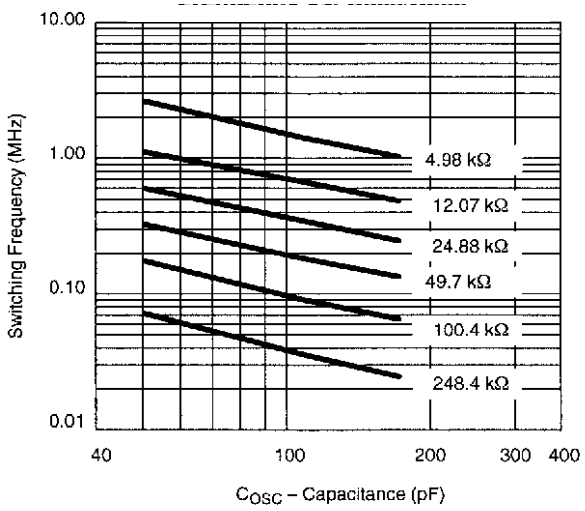
D_R and D_S Sourcing Current vs. Supply Voltage



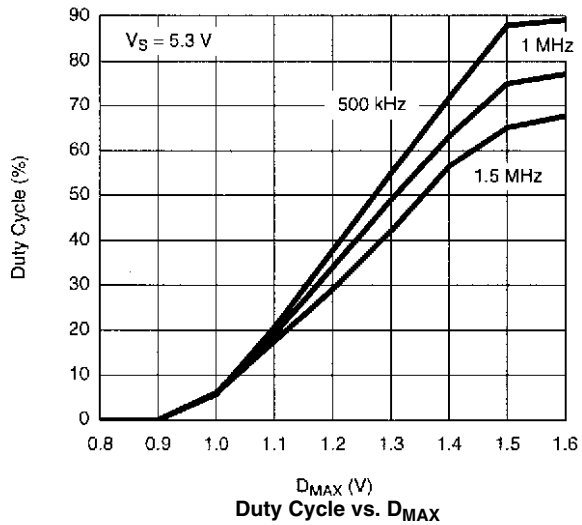
D_R and D_S Sinking Current vs. Supply Voltage



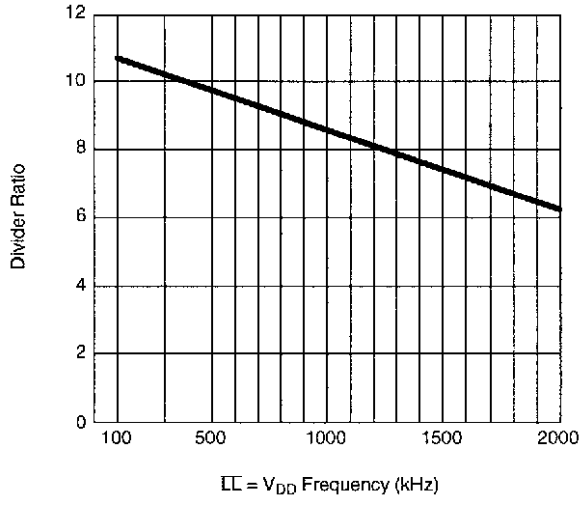
Switching Frequency vs. Supply Voltage



Frequency vs. R_{OSC}/C_{OSC}



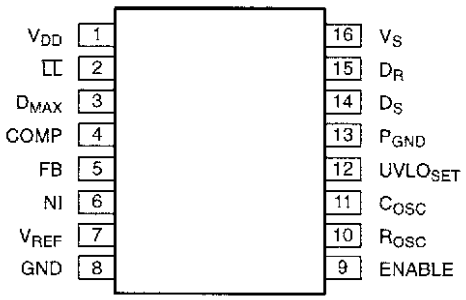
Duty Cycle vs. D_{MAX}



Ratio of $\overline{LL}$ = V_{DD} vs. $\overline{LL}$ = V Frequency

PIN CONFIGURATIONS

TSSOP-16



Top View

Order Number: Si9161BQ-T1

PIN DESCRIPTION

Pin 1: V_{DD}

The positive power supply for all functional blocks except output driver. A bypass capacitor of 0.1 µF (minimum) is recommended.

Pin 2: $\overline{LL}$

A logic high on this pin allows normal operation. A logic low places the chip in light-load optimized-efficiency mode. In light-load mode, the oscillator frequency is reduced and D_R goes high, disabling synchronous rectification. Do not leave pin unconnected.

Pin 3: D_{MAX}

Used to set the maximum duty cycle.

Pin 4: COMP

This pin is the output of the error amplifier. A compensation network is connected from this pin to the FB pin to stabilize the system. This pin drives one input of the internal pulse width modulation comparator.

Pin 5: FB

The inverting input of the error amplifier. An external resistor divider is connected to this pin to set the regulated output voltage. The compensation network is also connected to this pin.

Pin 6: NI

The non-inverting input of the error amplifier. In normal operation it is externally connected to V_{REF} or an external reference.

Pin 7: V_{REF}

This pin supplies a 1.5 V reference.

Pin 8: GND (Ground)

Pin 9: ENABLE

A logic high on this pin allows normal operation. A logic low places the chip in the standby mode. In standby mode, normal operation is disabled, supply current is reduced, the oscillator stops, and D_S goes low while D_R goes high.

Pin 10: R_{OSC}

A resistor connected from this pin to ground sets the oscillator's capacitor (C_{OSC}) charge and discharge current. See the oscillator section of the description of operation.

Pin 11: C_{OSC}

An external capacitor is connected to this pin to set the normal oscillator frequency.

$$f_{OSC} \cong \frac{0.70}{R_{OSC} \times C_{OSC}} \qquad \text{(at } V_{DD} = 5.0 \text{ V)}$$

Pin 12: $UVLO_{SET}$

This pin will place the chip in the standby mode if the $UVLO_{SET}$ voltage drops below 1.2 V. Once the $UVLO_{SET}$ voltage exceeds 1.2 V, the chip operates normally. There is a built-in hysteresis of 200 mV.

Pin 13: P_{GND}

The negative return for the V_S supply.

Pin 14: D_S

This CMOS push-pull output pin drives the external N-Channel MOSFET. This pin will be low in the standby mode. A break-before-make function between D_S and D_R is built-in.

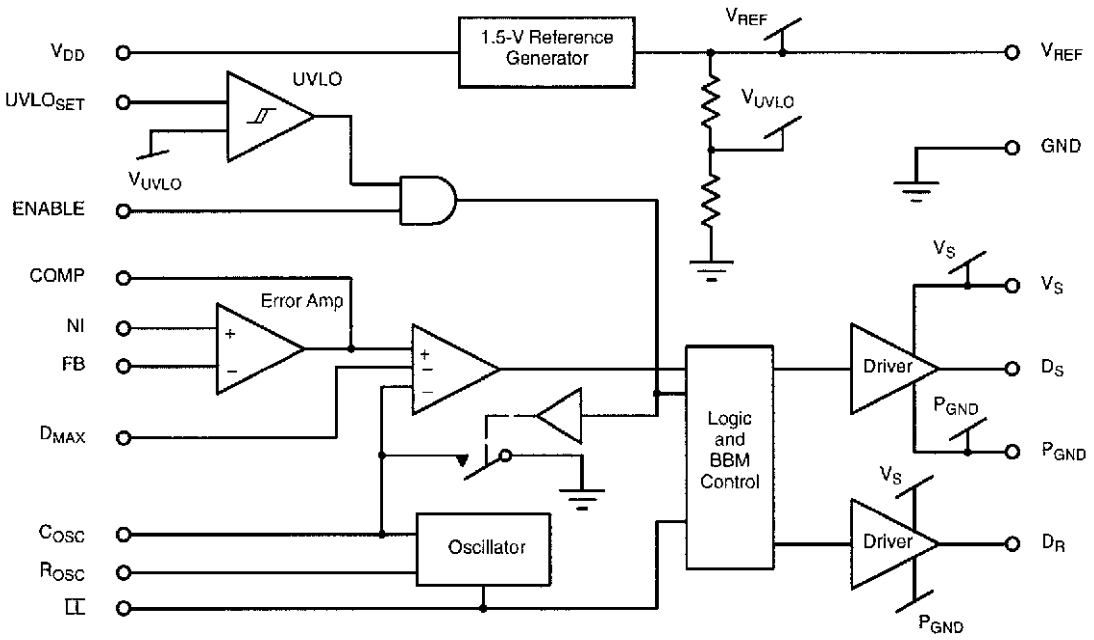
Pin 15: D_R

This CMOS push-pull output pin drives the external P-Channel MOSFET. This pin will be high in the standby and light-load modes. A break-before-make function between the D_S and D_R is built-in.

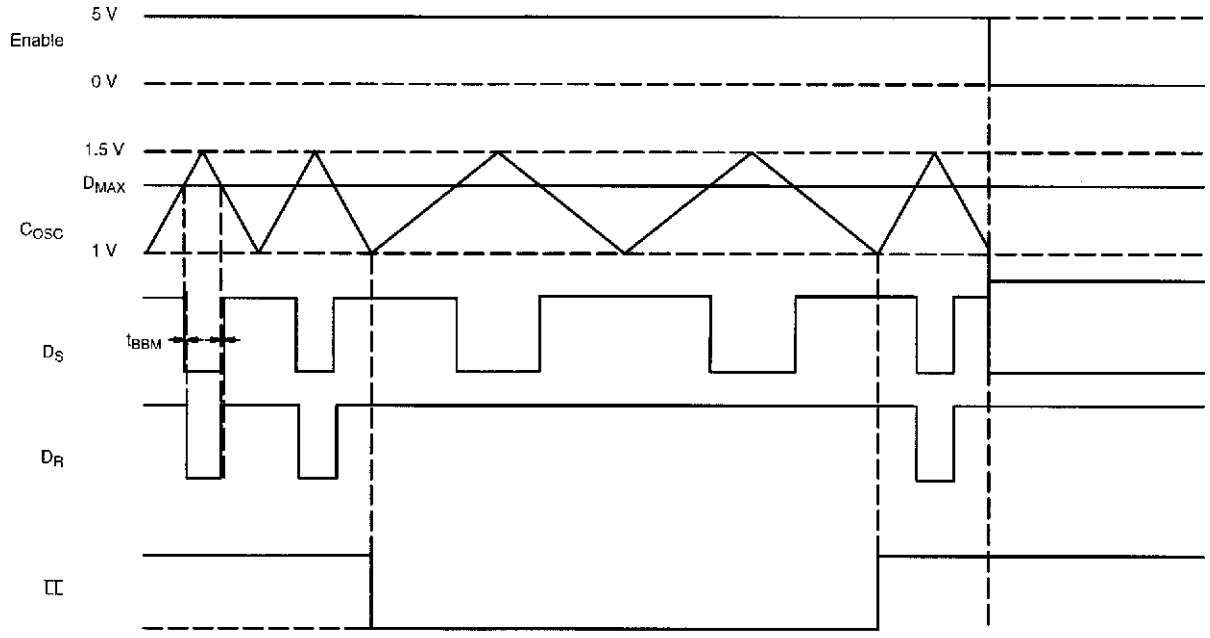
Pin 16: V_S

The positive terminal of the power supply which powers the CMOS output drivers. A bypass capacitor is required.

FUNCTIONAL BLOCK DIAGRAM



TIMING WAVEFORMS



Notes: Timing waveforms are not to scale.

OPERATION OF THE SI9161 BOOST CONVERTER

The Si9161 combined with optimized complementary MOSFETs provides the ideal solution to small, high efficiency, synchronous boost power conversion. Optimized for a 1-cell lithium ion, or 3-cell to 4-cell Nickel metal hydride battery, it is capable of switching at frequencies of up to 2 MHz. Combined with the Si6801, a complimentary high-frequency MOSFET, efficiencies of over 90 % are easily achieved in a very small area; with light-load mode, efficiency over 80 % can be achieved at power less than 1/2 W.

PWM Controller

The Si9161 implements a user-selectable synchronous/non-synchronous voltage mode PWM control topology and is especially designed for battery power conversion. Voltage-mode control results in the most efficient power conversion solution. Figure 1 below illustrates a schematic for a synchronous boost converter with an input range of 2.7 V to 5 V which covers the range of 1-cell LiIon and 3-cell or 4-cell NiMH/NiCd battery input respectively, and an output voltage of 5 V. Note the maximum input voltage is limited to the output voltage for a boost converter.

The switching frequency is determined by an external capacitor and resistor connected to C_{osc} and R_{osc} pins. The graph on page 5 in the Typical Characteristics section shows the typical C_{osc} and R_{osc} values for various switching frequency. Si9161 oscillator frequency can be easily synchronized to external frequency as long as external switching frequency is higher than the internal oscillator frequency. The synchronization circuit is a series resistor and capacitor fed into the C_{osc} pin of the Si9161. The synchronization pulse should be greater than 1.5 V in amplitude and a near square wave pulsed clock. Figure 1 shows typical values for the synchronization components.

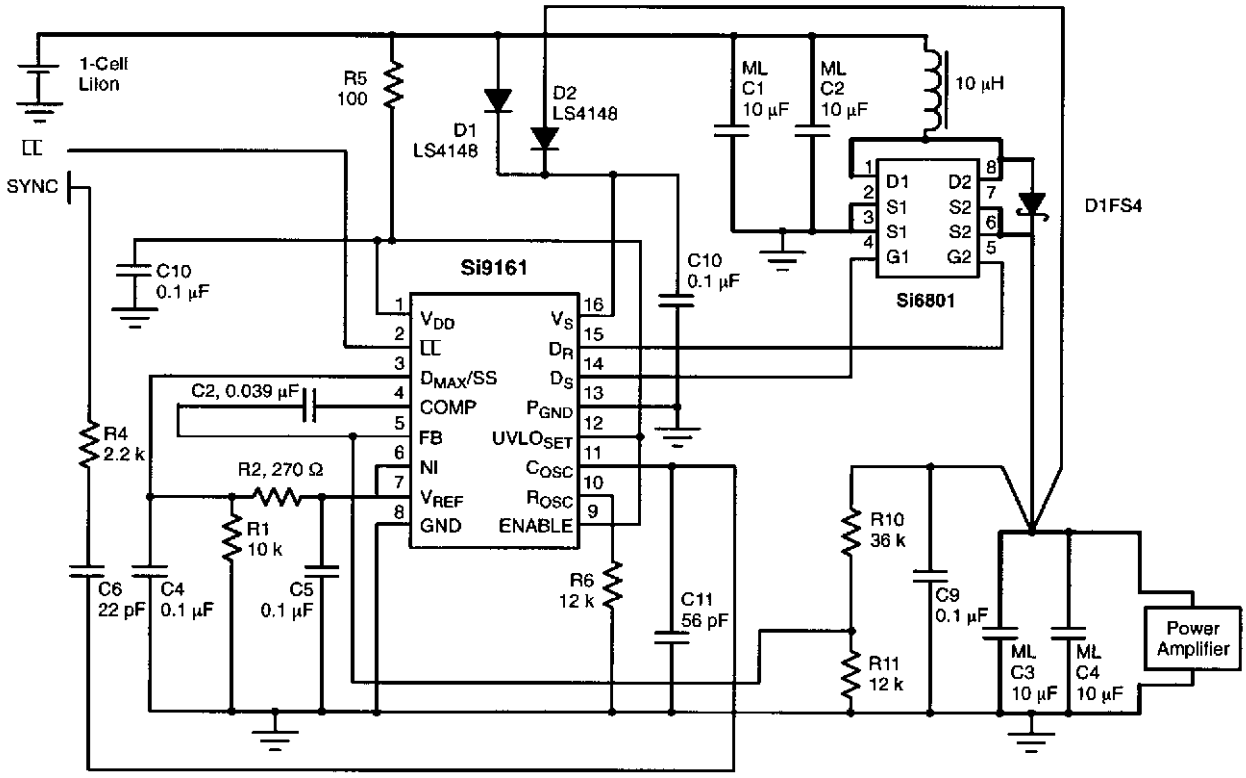


Figure 1. Si9161 Boost Converter

Startup

Designed to operate with single cell Lithium Ion battery voltage, the Si9161 has an operating range of 2.7 V to 6.0 V. During start-up, the device requires 3.0 V to guarantee proper operation, although it will typically start up at less than 2.2 V. Once powered, Si9161 will continue to operate until the voltage at V_{DD} is 2.7 V; at this point, the battery is basically dead. During start-up, power for the chip is provided by the battery through R5 to V_{DD} and through schottky diode D1 to V_S pins. Once the converter is fully operating, V_S supply power is provided by the converter output through diode D2, which overrides the D1 diode. This self perpetuating method of powering further improves the converter efficiency by utilizing higher gate drive to lower the on-resistance loss of the MOSFET.

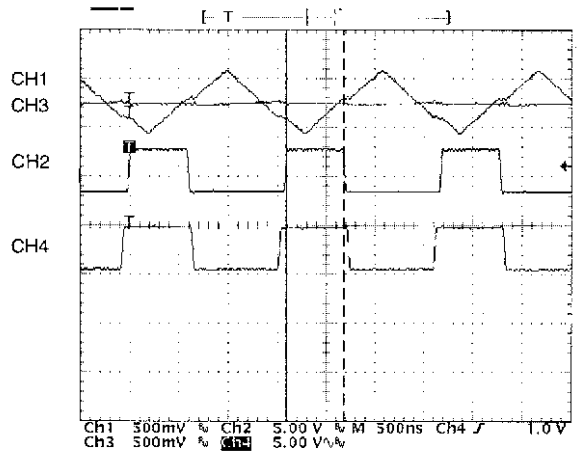
Another benefit of powering from the output voltage is it provides minimum load on the converter. This prevents the converter from skipping frequency pulses typically referred to as Burst or Pulse-Skipping modes. Pulse skipping mode could be dangerous, especially if it generates noise in RF, IF, or signal processing frequency bands.

Enable and Under Voltage Shutdown

The Si9161 is designed with programmable under-voltage lockout and enable features. These features give designers flexibility to customize the converter design. The undervoltage lockout threshold is 1.2 V. With a simple resistor divider from V_{DD}, Si9161 can be programmed to turn-on at any V_{DD} voltage. The ENABLE pin, a TTL logic compatible input, allows remote shutdown as needed.

Gate Drive and MOSFETs

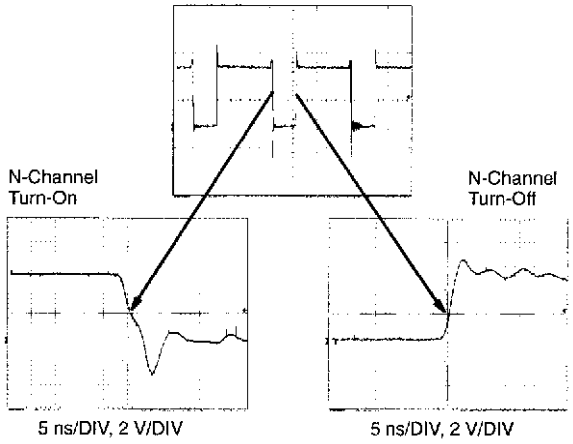
The gate drive section is designed to drive the high-side P-Channel switch and low-side N-Channel switch. The internal 40 ns break-before-make (BBM) timing prevents both MOSFETs from turning-on simultaneously. The BBM circuit monitors both drive voltages, once the gate-to-source voltage drops below 2.5 V, the other gate drive is delayed 40 ns before it is allowed to drive the external MOSFET (see Figure 2 for timing diagram). This smart gate drive control provides additional assurance that shoot-through current will not occur.



CH1: C_{OSC} ; CH2: D_S
CH3: COMP; CH4: D_R

Figure 2. Gate Drive Timing Diagrams

The MOSFET used is the Si6801, an N- and P-Channel in a single package TSSOP-8. The Si6801 is optimized to have very low gate charge and gate resistance. This results in a great reduction in gate switching power losses. The average time to switch on and off a MOSFET in a conventional structure is about 20 ns. The Si6801 will switch on and off in < 5 ns, see Figure 3.



Note the Speed

These MOSFETs have switching speeds of < 5 ns. This high speed is due to the fast, high current output drive of the Si9161 and the optimized gate charge of the Si6801.

Figure 3. Gate Switching Times

Stability Components

A voltage mode boost converter is normally stabilized with simple lag compensation due to the additional 90 ° phase lag introduced by the additional right hand plane zero, as well as having a duty factor dependent resonant frequency for the output filter. The stability components shown in Figure 1 have been chosen to ensure stability under all battery conditions while maintaining maximum transient response. To do this we have used simple lag compensation (type 1 amplifier configuration). Figure 4 shows the bode plot for the above circuit, maintaining > 50 ° phase margin over the entire battery voltage range.

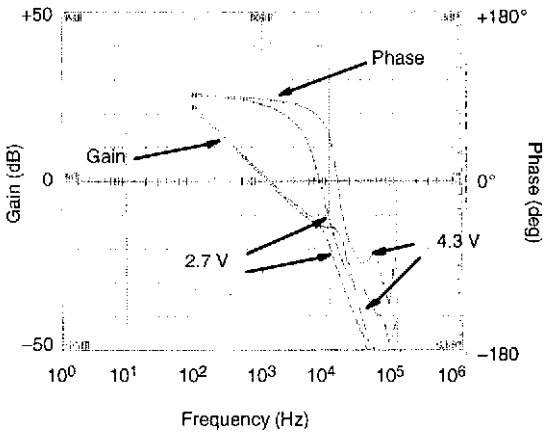


Figure 4. Stability, with 1-cell Li battery input, 5 V at 600 mA output.

Energy Storage Components

The input and output ripple voltage is determined by the switching frequency, and the inductor and capacitor values. The higher the frequency, inductance, or capacitance values, the lower the ripple. The efficiency of the converter is also improved with higher inductance by reducing the conduction loss in the switch, synchronous rectifier, and the inductor itself. In the past, Tantalum was the preferred material for the input and output capacitors. Now, with 2 MHz switching frequencies, Tantalum capacitors are being replaced with smaller surface mount ceramic capacitors. Ceramic capacitors have almost no equivalent series resistance (ESR). Tantalum capacitors have at least 0.1 Ω ESR. By reducing ESR, converter efficiency is improved while decreasing the input and output ripple voltage. With ceramic capacitors, output ripple voltage is a function of capacitance only. The equation for determining output capacitance is stated below.

$$C = \frac{I_{OUT} \cdot (V_{OUT} - V_{IN})}{V_{OUT} \cdot \Delta V_{RIPPLE} \cdot f}$$

I_{OUT} = output dc load current
V_{OUT} = output voltage
V_{IN} = input voltage
ΔV_{RIPPLE} = desired output ripple voltage
f = switching frequency

The inductance value for the converter is a function of the desired ripple voltage and efficiency as stated below. In order to keep the ripple small and improve efficiency, the inductance needs to be large enough to maintain continuous current mode. Continuous current mode has lower RMS current compared to discontinuous current mode since the peak current is lower. This lowers the conduction loss and improves efficiency. The equation that shows the critical inductance which separates continuous and discontinuous current mode at any given output current is stated below. This equation is also plotted in Figure 5 as a function of input voltage.

$$L = \frac{V_{IN}^2 \cdot (V_{OUT} - V_{IN}) \cdot \eta}{2 \cdot V_{OUT}^2 \cdot I_{OUT} \cdot f}$$

η = efficiency

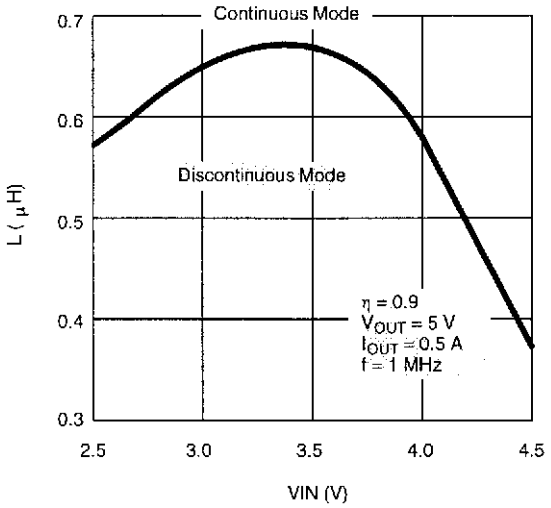


Figure 5. Continuous and Discontinuous Inductance Curve

Designed with small surface mount inductors and capacitors, the Si9161 solution can fit easily within a small space such as a battery pack. Another distinct advantage of a smaller converter size is that it reduces the noise generating area by reducing the high current path; therefore radiated and conducted noise is less likely to couple into sensitive circuits.

RESULTS SECTION

The following section shows the actual results obtained with the circuit diagram shown in Figure 1.

Efficiency

The graph below shows the efficiency of the above design at various constant switching frequencies. The frequencies were generated using a 3 V square wave of the desired frequency to the sync input to the circuit. The input voltage to the circuit is 3.6 V dc.

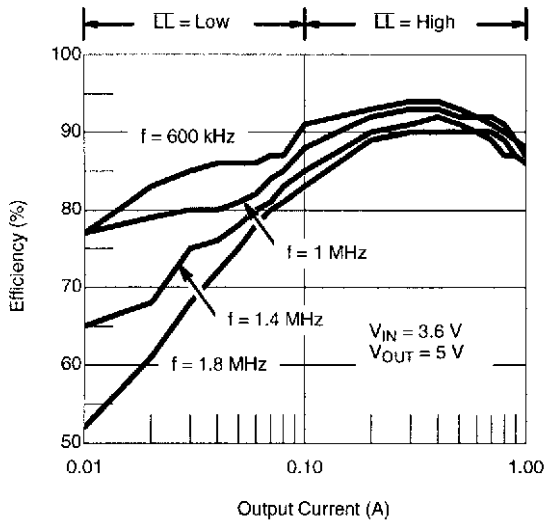
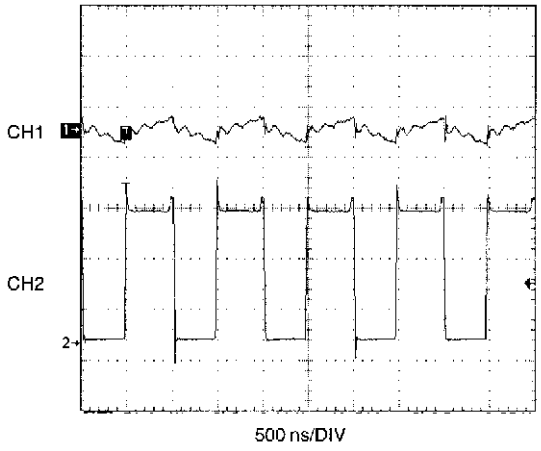


Figure 6. Efficiency of Si9161 and Si6801 Boost converter at various fixed frequencies



CH1: Output Ripple (50 mV/DIV)
CH2: P- and N-Channel Drain Voltage (2 V/DIV)

Figure 7. Output noice of the Si9160 demo board

Output Noise

The noise generated by a dc-dc converter is always an issue within the mobile phone. The Si9161 offers two benefits.

1. The noise spectrum is a constant, i.e. no random noise or random harmonic generation.
2. The switching fundamental can be synchronized to a known frequency, e.g. 812.5 kHz which is $^1/_{16}$-th of the GSM/DCS system clock, or 1.23 MHz which is the channel spacing frequency for CDMA, etc.

Figures 7 through 9 show the output noise and output spectrum analysis.

Output Noise Spectrum

Note there is no random noise, only switching frequency harmonics. This is very good news for the RF stages, where an unknown, or random noise spectrum will cause problems.

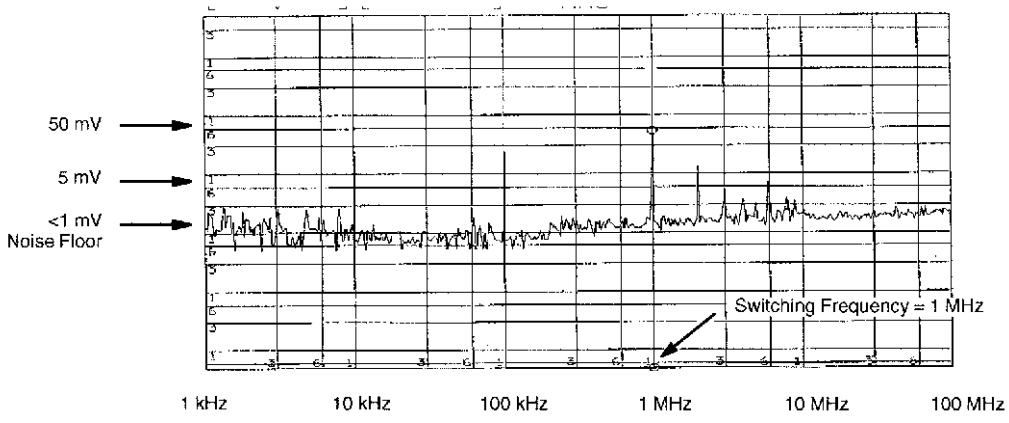


Figure 8. Spectrum response for the Si9161 demo board output voltage

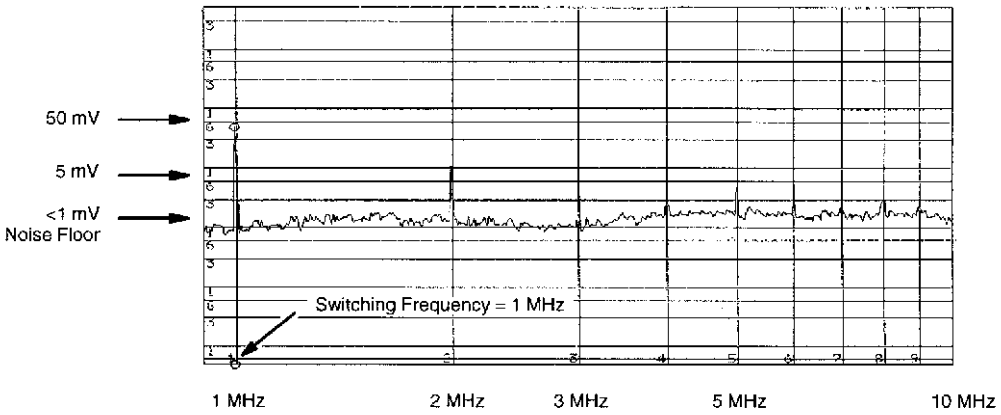


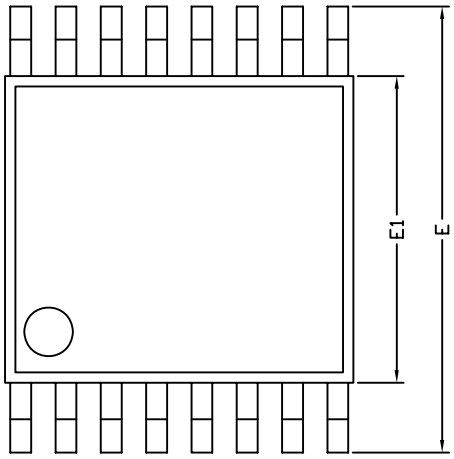
Figure 9. Higher resolution of noise spectrum

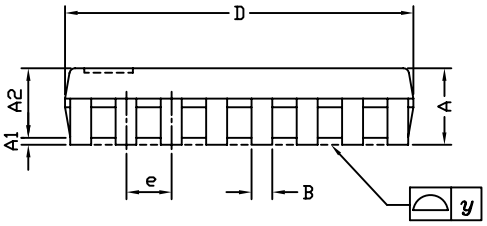
Conclusion

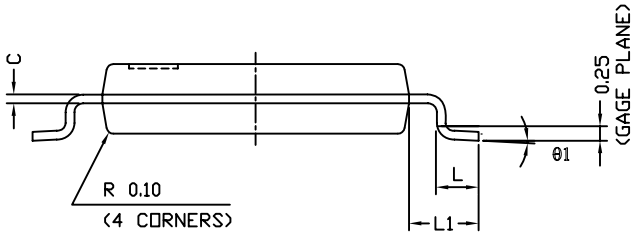
Switching at high, known frequencies results in a smaller footprint while maintaining high efficiency. Efficiencies at high switching frequencies can be improved by using Si6801 optimized low gate charge and low gate resistance MOSFET.

Even though the high frequency MOSFET has been designed with minimum gate charge, it still presents significant power loss during the light load conditions. In order to minimize this switching loss, Si9161 is designed with a light load efficiency improvement pin which decreases the switching frequency by 8.5 times (at 1 MHz) and disables the synchronous rectification. This feature improves the light load efficiency in certain conditions as much as 50 % compare to Si9160. Additionally, under transmitting mode, Si9161 clock frequency can be synchronized to higher external frequency which eliminates or greatly reduces any radio interference concerns and pushes harmonics out beyond signal processing frequencies.

TSSOP: 16-LEAD

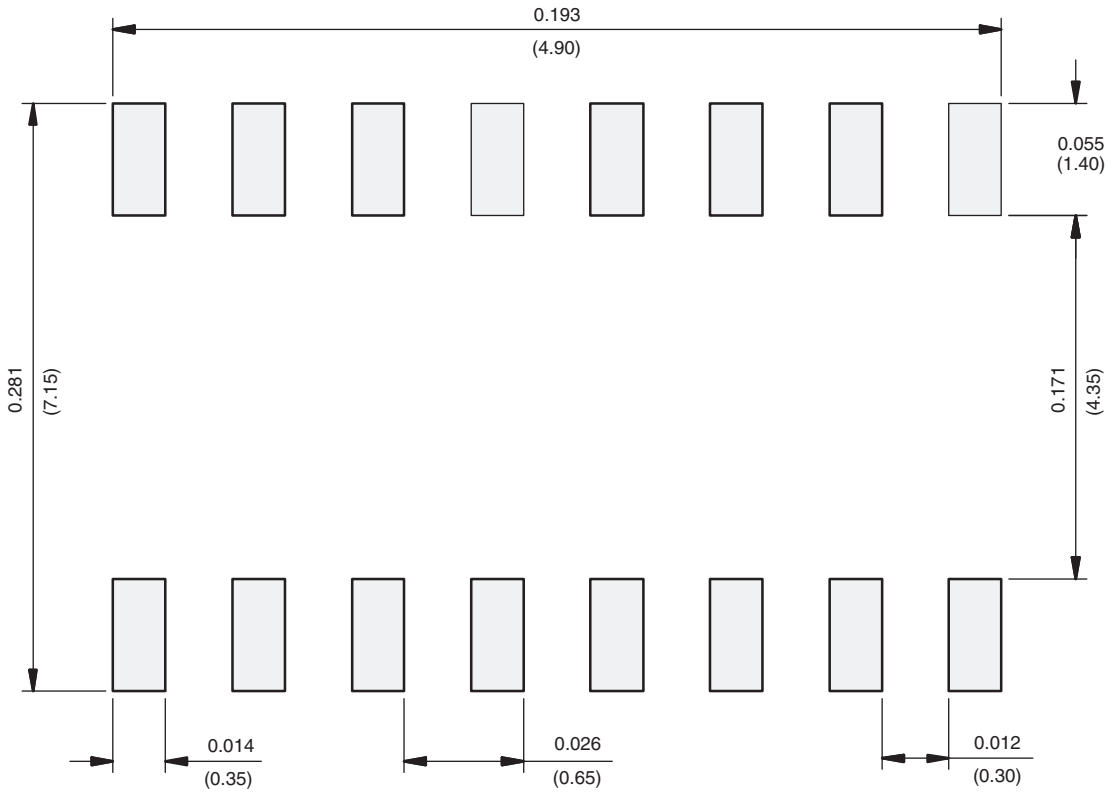






Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06 DWG: 5624			

RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

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