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MOTOROLA

MC33267

Low Dropout Regulator

The MC33267 is a positive fixed 5.0 V regulator that is specifically designed to maintain proper voltage regulation with an extremely low input–to–output voltage differential. This device is capable of supplying output currents in excess of 500 mA and contains internal current limiting and thermal shutdown protection. Also featured is an on–chip power–up reset circuit that is ideally suited for use in microprocessor based systems. Whenever the regulator output voltage is below nominal, the reset output is held low. A programmable time delay is initiated after the regulator has reached its nominal level and upon timeout, the reset output is released.

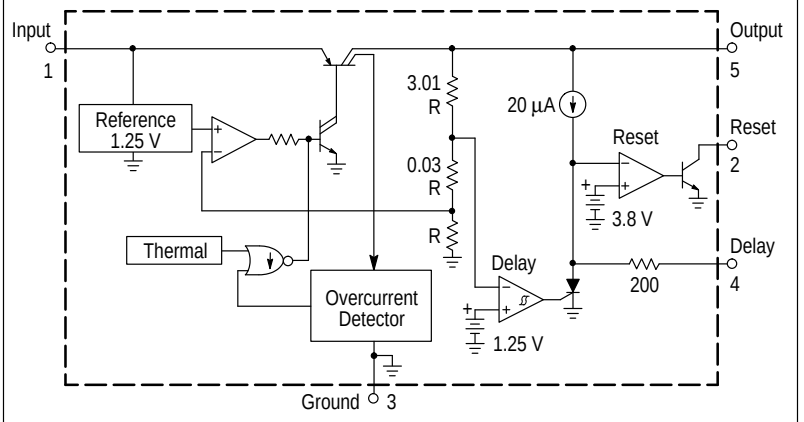
Due to the low dropout voltage specifications, the MC33267 is ideally suited for use in battery powered industrial and consumer equipment where an extension of useful battery life is desirable. This device is contained in an economical five lead TO–220 type package.

- Low Input–to–Output Voltage Differential
- Output Current in Excess of 500 mA
- On–Chip Power–Up Reset Circuit with Programmable Delay
- Internal Current Limiting with Thermal Shutdown
- Economical Five Lead TO–220 Type Packages

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC33267T	T_J = –40 ° to +125°C	Plastic Power
MC33267TV		Plastic Power
MC33267D2T	T_J = –40 ° to +105°C	Surface Mount

Representative Block Diagram

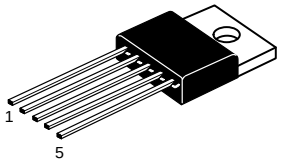


This device contains 37 active transistors.

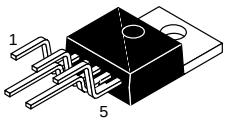
LOW DROPOUT REGULATOR with POWER–UP RESET

SEMICONDUCTOR TECHNICAL DATA

Pin 1. V_{CC} Input
2. Reset
3. Ground
4. Delay
5. Output

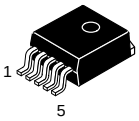


T SUFFIX
PLASTIC PACKAGE
CASE 314D



TV SUFFIX
PLASTIC PACKAGE
CASE 314B

Heatsink surface connected to Pin 3.



D2T SUFFIX
PLASTIC PACKAGE
CASE 936A
(D^2PAK)

Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range	V_{in}	– 20 to + 40	Vdc
Delay Voltage Range	V_{DLYR}	– 0.3 to V_O	V
Delay Sink Current	$I_{DLY(sink)}$	25	mA
Reset Voltage Range	V_{RR}	– 0.3 to +15	V
Reset Sink Current	$I_{R(sink)}$	50	mA
Power Dissipation Case 314B and 314D (TO–220 Type) T_A = 25°C Thermal Resistance, Junction–to–Ambient Thermal Resistance, Junction–to–Case Case 936A (D^2PAK) [Note 1] T_A = 90°C Thermal Resistance, Junction–to–Ambient Thermal Resistance, Junction–to–Case	 P_D $R_{\theta JA}$ $R_{\theta JC}$ P_D $R_{\theta JA}$ $R_{\theta JC}$	 Internally Limited 62.5 4.0 Internally Limited 70 5.0	 W °C/W °C/W W °C/W °C/W
Operating Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

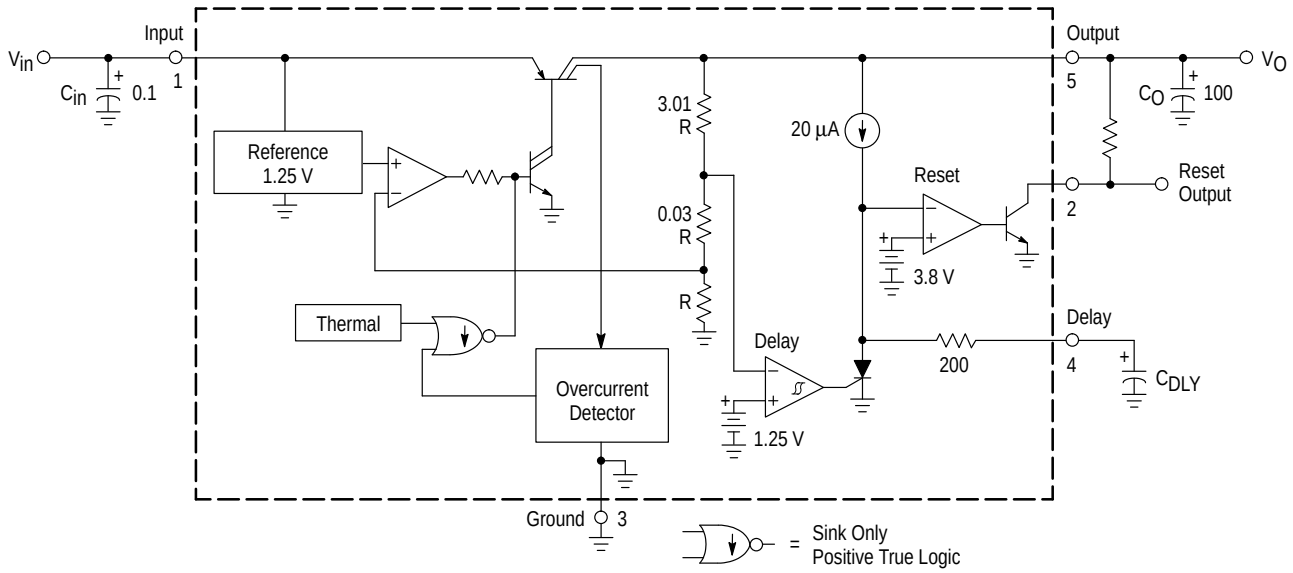
NOTE: 1. D^2PAK Junction–to–Ambient Thermal Resistance is for vertical mounting. Refer to Figure 7 for board mounted thermal resistance.

ELECTRICAL CHARACTERISTICS (V_{in} = 14.4 V, I_O = 5.0 mA, C_O = 100 μF, $C_{O(ESR)} \leq 0.3\ \Omega$, T_J = 25°C (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 5.0 mA to 500 mA, V_{in} = 6.0 V to 28 V) T_J = 25°C T_J = – 40° to +125°C	V_O	 4.95 4.9	 5.05 –	 5.15 5.2	V
Line Regulation (V_{in} = 6.0 V to 26 V)	Reg_{line}	–	3.0	50	mV
Load Regulation (I_O = 5.0 mA to 500 mA)	Reg_{load}	–	1.0	50	mV
Bias Current I_O = 0 mA I_O = 150 mA I_O = 500 mA I_O = 500 mA, V_{in} = 6.2 V	I_B	 – – – –	 12 22 100 120	 20 40 200 300	mA
Ripple Rejection (f = 120 Hz, V_{in} = 7.0 V to 17 V, I_O = 350 mA, C_O = 100 μF)	RR	 60	 80	 –	dB
Dropout Voltage (I_O = 500 mA)	$V_{in} - V_O$	–	0.58	0.8	V
Delay Comparator Threshold (V_O Decreasing)	$V_{th(DLY)}$	4.8	V_O – 0.15	V_O – 0.08	V
Delay Pin Source Current	$I_{DLY(source)}$	12	20	28	μA
Reset Comparator Threshold	$V_{th(R)}$	3.6	3.8	4.0	V
Reset Sink Saturation (I_{sink} = 10 mA)	$V_{CE(sat)}$	–	0.2	0.8	V
Reset Off–State Leakage (V_{CE} = 5.0 V)	$I_{R(leak)}$	–	0.3	10	μA

NOTE: 2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

Figure 1. Typical Application Circuit



APPLICATION CIRCUIT INFORMATION

The MC33267 is a low dropout, positive fixed 5.0 V, 500 mA regulator. Protection features include output current limiting and thermal shutdown. System protection consists of an on–chip power–up microprocessor reset circuit.

A typical applications circuit is shown in Figure 1. The input bypass capacitor (C_{in}) is recommended if the regulator is located an appreciable distance (≥ 4″) from the supply input filter. This will reduce the circuit's sensitivity to the input line impedance at high frequencies.

These regulators are not internally compensated and thus require an external output capacitor (C_O) for stability. The recommended capacitance is 100 μF with an equivalent series resistance (ESR) of less than 0.3 Ω. A minimum capacitance of 33 μF with a maximum ESR of 3.0 Ω can be used in applications where space is a premium, however, these limits must be observed over the entire operating temperature range of the regulator circuit.

With economical electrolytic capacitors, cold temperature operation can pose a serious stability problem. As the electrolyte freezes, around – 30°C, the capacitance will decrease and the ESR will increase drastically, causing the circuit to oscillate. Quality electrolytic capacitors with extended temperature ranges of – 40°C to + 85°C and – 55°C to +105°C are readily available. It is suggested that oven testing of the entire circuit be performed with maximum load, minimum input voltage, and minimum ambient temperature.

Figure 2 shows the reset circuit timing relationship. Note that whenever the regulator's output is less than 4.9 V, the delay capacitor (C_{DLY}) is immediately discharged, and the reset output is held in a low state. As the regulator's output voltage increases beyond 4.97 V, the delay comparator will allow the 20 μA current source to charge C_{DLY}. The reset output will go to a high state when C_{DLY} crosses the 3.8 V threshold of the reset comparator. The reset delay time is controlled by the value selected for C_{DLY}. The required system reset time is governed by the microprocessor and usually a reset signal which lasts several machine cycles is sufficient.

Figure 2. Timing Waveforms

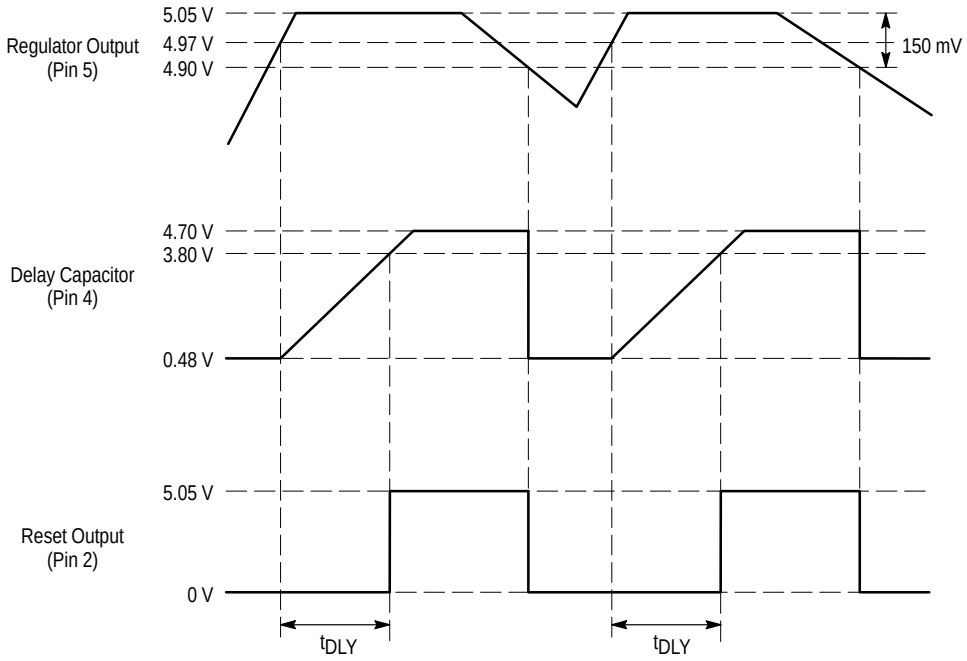


Figure 3. Reset Output versus Input Voltage

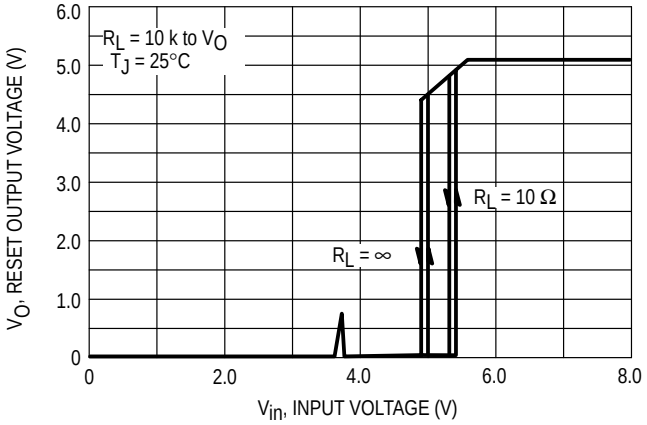


Figure 4. Output Voltage versus Input Voltage

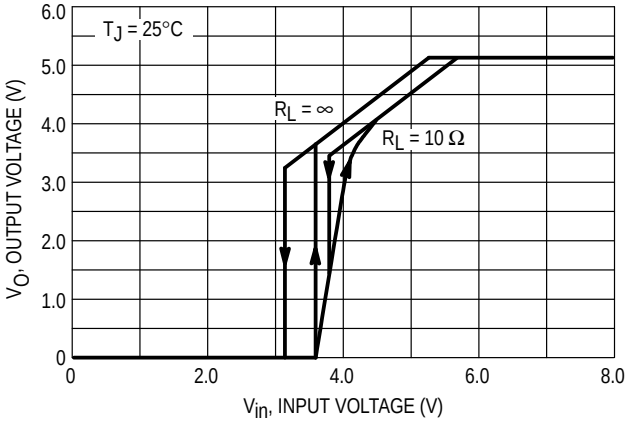


Figure 5. Reset Output versus Input Voltage

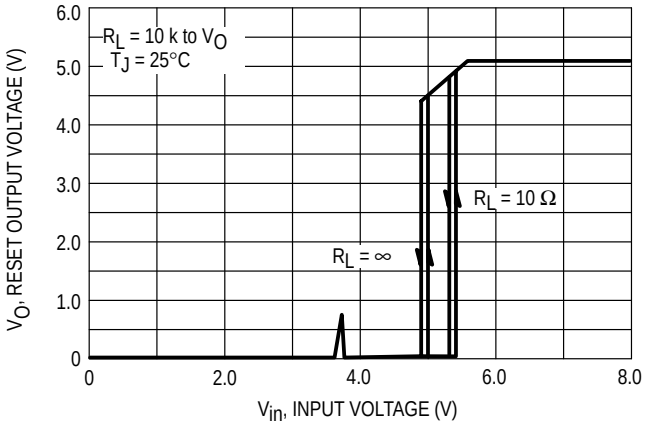


Figure 6. Output Voltage versus Input Voltage

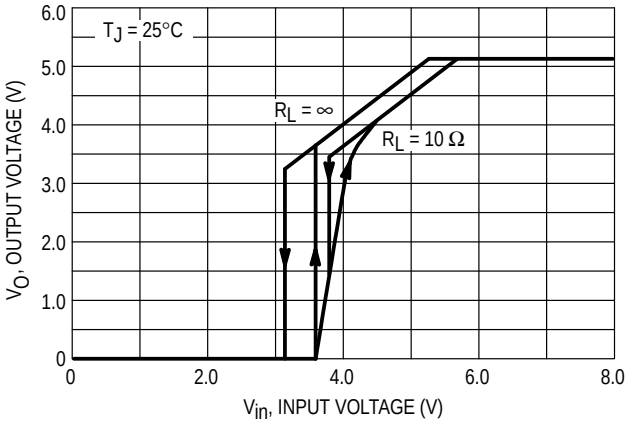
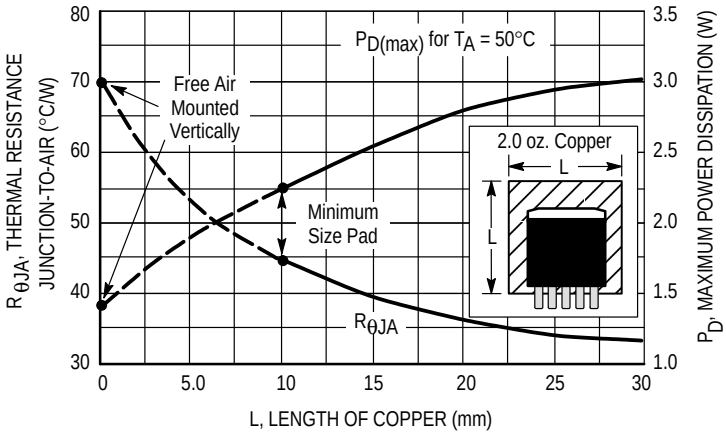
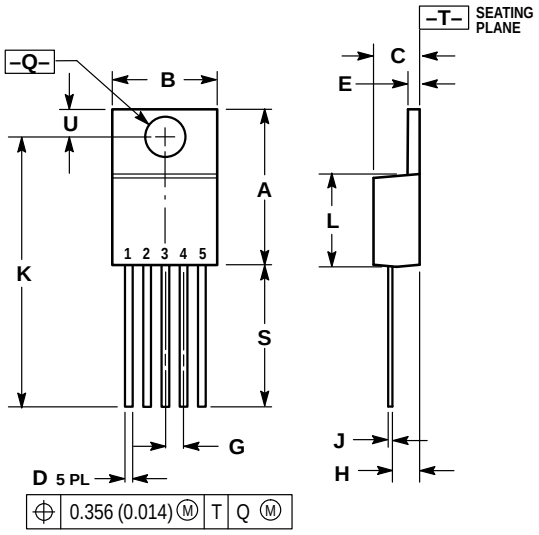


Figure 7. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



OUTLINE DIMENSIONS

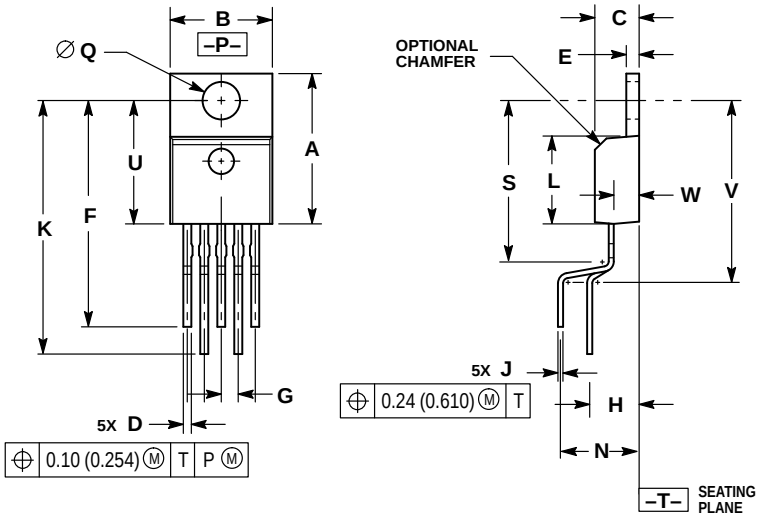
T SUFFIX
PLASTIC PACKAGE
CASE 314D–03
(TO–220 TYPE)
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
G	0.067 BSC		1.702 BSC	
H	0.087	0.112	2.210	2.845
J	0.015	0.025	0.381	0.635
K	1.020	1.065	25.908	27.051
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
U	0.105	0.117	2.667	2.972
S	0.543	0.582	13.792	14.783

TV SUFFIX
PLASTIC PACKAGE
CASE 314B–05
(TO–220 TYPE)
ISSUE J

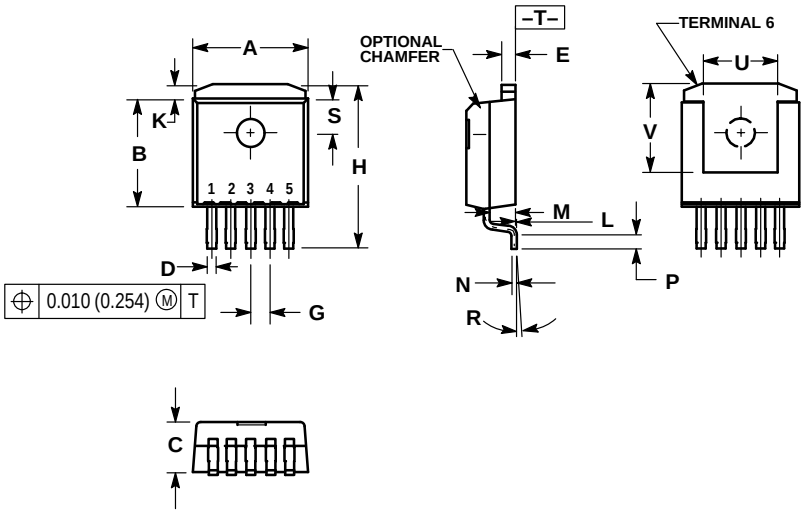


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 0.043 (1.092) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
F	0.850	0.935	21.590	23.749
G	0.067 BSC		1.702 BSC	
H	0.166 BSC		4.216 BSC	
J	0.015	0.025	0.381	0.635
K	0.900	1.100	22.860	27.940
L	0.320	0.365	8.128	9.271
N	0.320 BSC		8.128 BSC	
Q	0.140	0.153	3.556	3.886
S	—	0.620	—	15.748
U	0.468	0.505	11.888	12.827
V	—	0.735	—	18.669
W	0.090	0.110	2.286	2.794

OUTLINE DIMENSIONS

D2T SUFFIX
PLASTIC PACKAGE
CASE 936A–02
(D^2PAK)
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	5 ° REF		5 ° REF	
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

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ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298