DS96F173M/DS96F175C/DS96F175M EIA-485/EIA-422 Quad Differential Receivers

Check for Samples: DS96F173M/DS96F175C/DS96F175M

FEATURES

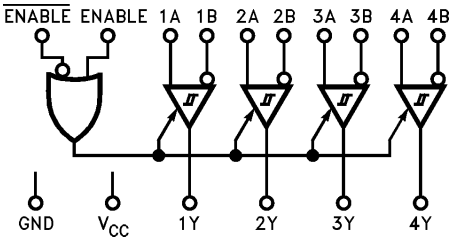
- **Meets EIA-485, EIA-422A, EIA-423A Standards**
- **Designed for Multipoint Bus Applications**
- **Tri-State Outputs**
- **Common Mode Input Voltage Range: −7V to +12V**
- **Operates from Single +5.0V Supply**
- **Reduced Power Consumption (I_{CC} = 50 mA max)**
- **Input Sensitivity of ±200 mV over Common Mode Range**
- **Input Hysteresis of 50 mV Typical**
- **High Input Impedance**
- **Military Temperature Range Available**
- **Qualified for MIL STD 883C**
- **Available to Standard Military Drawings (SMD)**
- **Available in CDIP(NFE), LCCC (NAJ), and CLGA (NAD) Packages**
- **DS96F173 and DS96F175 are Lead and Function Compatible with SN75173/175 or the AM26LS32/MC3486**

DESCRIPTION

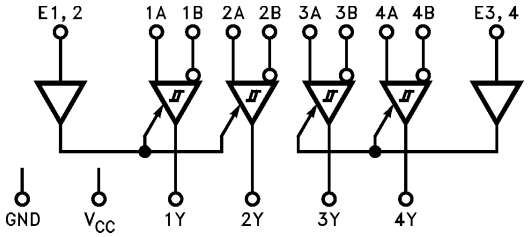
The DS96F173 and the DS96F175 are high speed quad differential line receivers designed to meet the EIA-485 standard. The DS96F173 and the DS96F175 offer improved performance due to the use of L-FAST bipolar technology. The use of LFAST technology allows the DS96F173 and DS96F175 to operate at higher speeds while minimizing power consumption.

The DS96F173 and the DS96F175 have tri-state outputs and are optimized for balanced multipoint data bus transmission at rates up to 15 Mbps. The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −7V to +12V. The receivers are therefore suitable for multipoint applications in noisy environments. The DS96F173 features an active high and active low Enable, common to all four receivers. The DS96F175 features separate active high Enables for each receiver pair.

Logic Diagrams



DS96F173



DS96F175

Function Tables

Table 1. (Each Receiver) DS96F173 (1)

Differential Inputs	Enable		Output
A–B	**E**	**$\overline{E}$**	**Y**
$V_{ID} \geq 0.2V$	H	X	H
	X	L	H
$V_{ID} \leq -0.2V$	H	X	L
	X	L	L
X	L	X	Z
X	X	H	Z

(1) H = High Level
L = Low Level
Z = High Impedance (off)
X = Don't Care

Table 2. (Each Receiver) DS96F175 (1)

Differential Inputs	Enable	Output
A–B	**E**	**Y**
$V_{ID} \geq 0.2V$	H	H
$V_{ID} \leq -0.2V$	H	L
X	L	Z

(1) H = High Level
L = Low Level
Z = High Impedance (off)
X = Don't Care

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings COMMERCIAL (1) (2)

Storage Temperature Range (T_{STG})		−65°C to +175°C
Lead Temperature (Soldering, 60 sec.)		300°C
Max. Package Power Dissipation (3) at 25°C	Ceramic CDIP (NFE)	1500 mW
	Supply Voltage	7.0V
	Input Voltage, A or B Inputs	±25V
	Differential Input Voltage	±25V
	Enable Input Voltage	7.0V
	Low Level Output Current	50 mA

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The tables of Electrical Characteristics provide conditions for actual device operation.
(2) Specifications for the 883 version of this product are listed separately.
(3) Derate package 10 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC}) DS96F175C	4.75	5.0	5.25	V
Common Mode Input Voltage (V_{CM})	−7		+12	V
Differential Input Voltage (V_{ID})			|12|	V
Output Current HIGH (I_{OH})			−400	µA
Output Current LOW (I_{OL})			11	mA
Operating Temperature (T_A) DS96F175C	0	25	70	°C

Electrical Characteristics (1) (2)

Over recommended supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential-Input High Threshold Voltage	$V_O = V_{OH}$				0.2	V
V_{TL}	Differential-Input (3) Low Threshold Voltage	$V_O = V_{OL}$		−0.2			V
$V_{TH} - V_{TL}$	Hysteresis (4)	V_{CM} = 0V			50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA				−1.5	V
V_{OH}	Output Voltage HIGH	V_{ID} = 200 mV	0°C to +70°C	2.8			V
		I_{OH} = −400 µA	−55°C to +125°C	2.5			
V_{OL}	Output Voltage LOW	V_{ID} = −200 mV	I_{OL} = 8.0 mA			0.45	V
			I_{OL} = 11 mA			0.50	
I_{OZ}	High-Impedance State Output	V_O = 0.4V to 2.4V				±20	µA
I_I	Line Input Current (5)	Other Input = 0V	V_I = 12V			1.0	mA
			V_I = −7.0V			−0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V				20	µA

(1) Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS96F175C. All typicals are given for V_{CC} = 5V and T_A = 25°C.
(2) All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.
(3) The algebraic convention, when the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.
(4) Hysteresis is the difference between the positive-going input threshold voltage. V_{TH}, and the negative going input threshold voltage, V_{TL}.
(5) Refer to EIA-485 Standard for exact conditions.

Electrical Characteristics[1][2] (continued)

Over recommended supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V				−100	µA
R_I	Input Resistance			14	18	22	kΩ
I_{OS}	Short Circuit Output Current	See [6]		−15		−85	mA
I_{CC}	Supply Current	No Load	Outputs Enabled			50	mA
I_{CCX}			Outputs Disabled			50	

(6) Only one output at a time should be shorted.

COMMERCIAL
Switching Characteristics

V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{ID} = −2.5V to +2.5V, C_L = 15 pF, See Figure 7	5.0	15	22	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	V_{CM} = 0V	5.0	15	22	ns
t_{ZH}	Output Enable Time to High Level	C_L = 15 pF, See Figure 8		12	16	ns
t_{ZL}	Output Enable Time to Low Level	C_L = 15 pF, See Figure 9		13	18	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5.0 pF, See Figure 8		14	20	ns
t_{LZ}	Output Disable Time from Low Level	C_L = 5.0 pF, See Figure 9		14	18	ns
$\|t_{PLH}–t_{PHL}\|$	Pulse Width Distortion (SKEW)	See Figure 7		1.0	3.0	ns

Absolute Maximum Ratings
MIL-STD-883C (1)(2)

Storage Temperature Range (T_{STG})		−65°C to +175°C
Lead Temperature (Soldering, 60 sec.)		300°C
Max. Package Power Dissipation (3) at 25°C	Ceramic CDIP (NFE)	1500 mW
	Ceramic CLGA (NAD)	1034 mW
	Ceramic LCCC (NAJ)	1500 mW
	Supply Voltage	7.0V
	Input Voltage, A or B Inputs	±25V
	Differential Input Voltage	±25V
	Enable Input Voltage	7.0V
	Low Level Output Current	50 mA

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The tables of Electrical Characteristics provide conditions for actual device operation.
(2) For complete Military Specifications, refer to the appropriate SMD or MDS.
(3) Above T_A = 25°C derate NFE package 10 mW/°C, NAD package 6.90 mW/°C, NAJ package 11.11 mW/°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC}) DS96F173M/DS96F175M	4.50	5.0	5.50	V
Common Mode Input Voltage (V_{CM})	−7		+12	V
Differential Input Voltage (V_{ID})			|12|	V
Output Current HIGH (I_{OH})			−400	µA
Output Current LOW (I_{OL})			11	mA
Operating Temperature (T_A) DS96F173M/DS96F175M	−55	25	125	°C

Electrical Characteristics (1) (2)

Over recommended supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions		Min	Max	Units
V_{TH}	Differential-Input High Threshold Voltage	V_{CC} = 4.5V, 5.5V V_{CM} = 0V, 12V, −12V			0.2	V
V_{TL}	Differential-Input (3) Low Threshold Voltage	V_{CC} = 4.5V, 5.5V V_{CM} = 0V, 12V, −12V		−0.2		V
V_{IH}	Enable Input Voltage HIGH			2.0		V
V_{IL}	Enable Input Voltage LOW				0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA, V_{CC} = 4.5V			−1.5	V
V_{OH}	Output Voltage HIGH	V_{ID} = 200 mV I_{OH} = −400 µA	−55°C to +125°C	2.5		V
V_{OL}	Output Voltage LOW	V_{ID} = −200 mV	I_{OL} = 8.0 mA		0.45	V
I_{OZ}	High-Impedance State Output	V_O = 0.4V, 2.4V, V_{CC} = 5.5V			±20	µA
I_I	Line Input Current (4)	Other Input = 0V	V_I = 12V		1.0	mA
			V_I = −7.0V		−0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V, V_{CC} = 5.5V			20	µA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V, V_{CC} = 5.5V			−100	µA
R_I	Input Resistance			10		kΩ
I_{OS}	Short Circuit Output Current	See (5)		−15	−85	mA
I_{CC}	Supply Current	No Load	Outputs Enabled or Disabled		50	mA
I_{CCX}						

(1) Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS96F175C. All typicals are given for V_{CC} = 5V and T_A = 25°C.
(2) All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.
(3) The algebraic convention, when the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.
(4) Refer to EIA-485 Standard for exact conditions.
(5) Only one output at a time should be shorted.

MIL-STD-883C
Switching Characteristics

V_{CC} = 5.0V

Symbol	Parameter	Conditions	T_A = 25°C		T_A = −55°C	T_A = 125°C	Units
			Typ	Max	Max	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{ID} = −2.5V to +2.5V, C_L = 15 pF, See Figure 7	15	22	30	30	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	V_{CM} = 0V	15	22	30	30	ns
t_{ZH}	Output Enable Time to High Level	C_L = 15 pF, See Figure 8	12	16	27	27	ns
t_{ZL}	Output Enable Time to Low Level	C_L = 15 pF, See Figure 9	13	18	27	27	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5.0 pF, See Figure 8 (1)	14	20	27	27	ns
		C_L = 20 pF, See Figure 8 (1)	14	30	37	37	ns
t_{LZ}	Output Disable Time from Low Level	C_L = 5.0 pF, See Figure 9	14	18	30	30	ns
$\|t_{PLH}-t_{PHL}\|$	Pulse Width Distortion (SKEW)	See Figure 7	1	3	5.0	5.0	ns

(1) Testing at 20 pF assures conformance to 5 pF specification.

Connection Diagrams

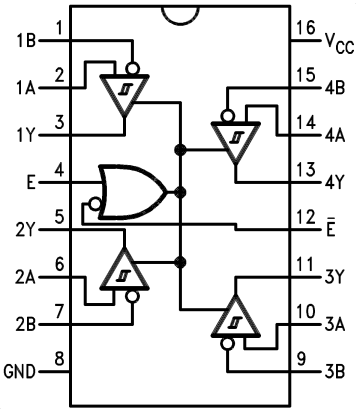


Figure 1. DS96F173 (Top View)(2)
16-Lead Ceramic Dual-In-Line CDIP Package
Package Number NFE

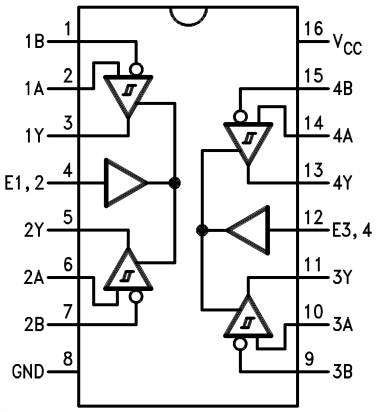
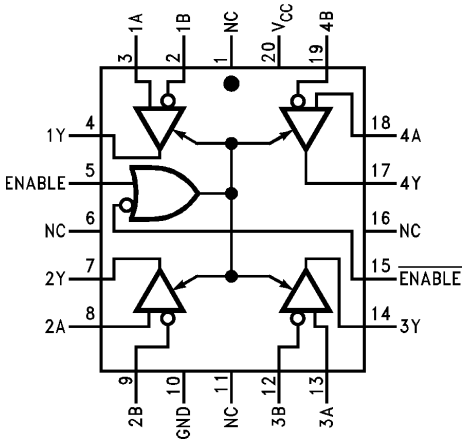


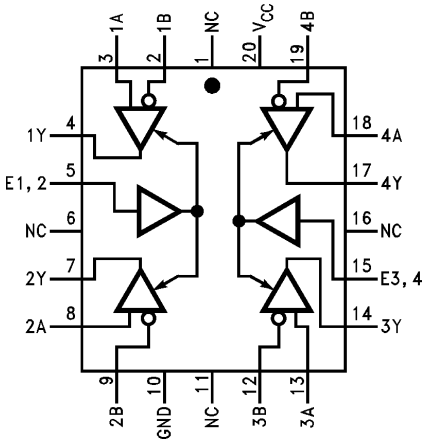
Figure 2. DS96F175 (Top View)(2)
16-Lead Ceramic Dual-In-Line CDIP Package
Package Number NFE

(2) DS96F173 with active high and active low Enables are shown. DS96F175 has active high Enable only.



*NC—No Connection

Figure 3. 20-Lead Ceramic Leadless Chip Carrier - LCCC (Top View)
See Package Number NAJ



*NC—No Connection

Figure 4. 20-Lead Ceramic Leadless Chip Carrier - LCCC (Top View)
See Package Number NAJ

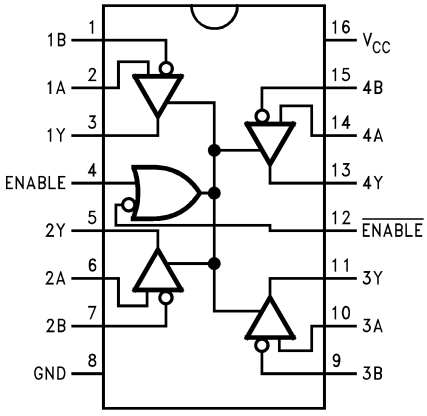


Figure 5. 16-Lead Ceramic Flatpak - CLGA (Top View)
See Package Number NAD

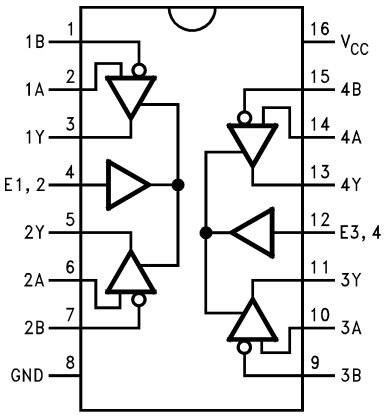


Figure 6. 16-Lead Ceramic Flatpak - CLGA (Top View)
See Package Number - NAD

Parameter Measurement Information

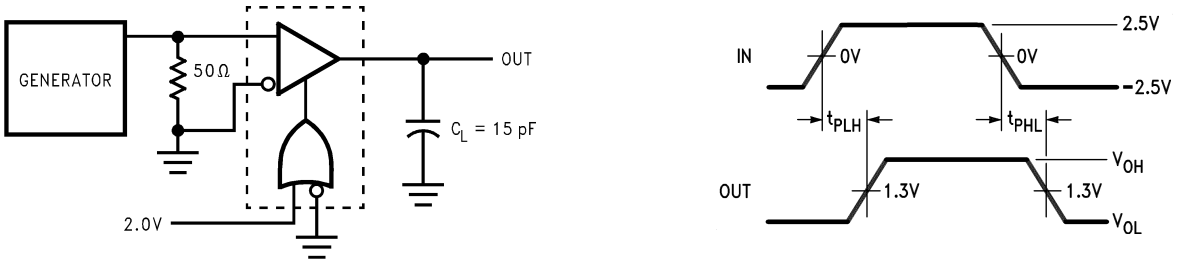


Figure 7. t_{PLH}, t_{PHL} (3)(4)

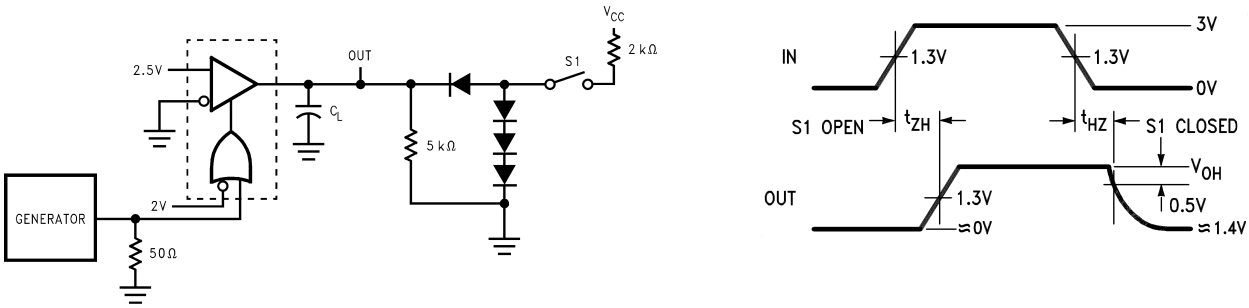


Figure 8. t_{HZ}, t_{ZH} (3)(4)(5)(6)

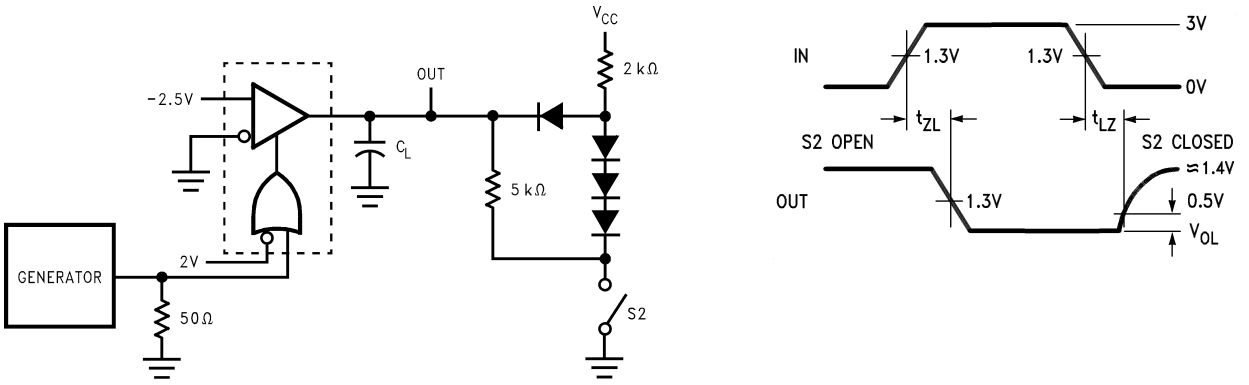
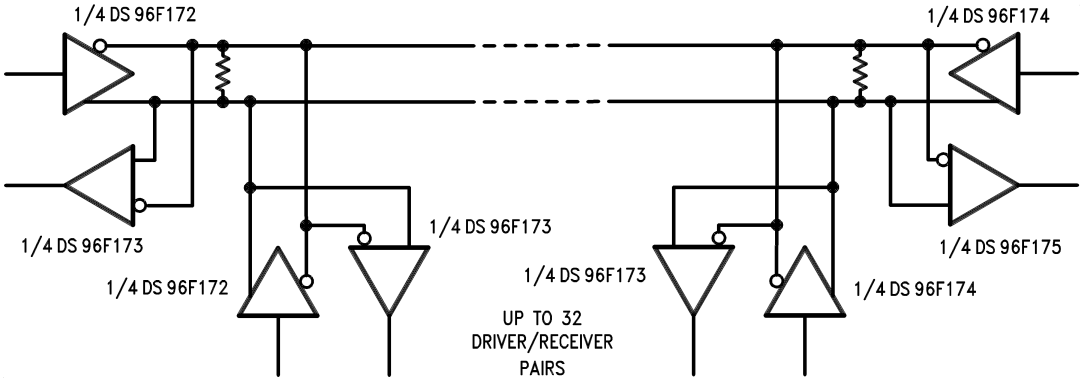


Figure 9. t_{ZL}, t_{LZ} (3)(4)(5)(6)

(3) The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% duty cycle, tr ≤ 6.0 ns, tf ≤ 6.0 ns, ZO = 50Ω.
(4) CL includes probe and stray capacitance
(5) All diodes are 1N916 or equivalent
(6) To test the active low Enable E of DS96F173, ground E and apply an inverted input waveform to E. DS96F175 has active high enable only.

Typical Application



NOTE

The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	10

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