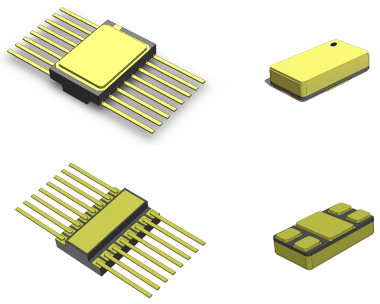
RHFL4913A

Datasheet

Rad-hard adjustable positive voltage regulator



Flat-16P SMD5C

The metallic lid of both package and the bottom metalization of the Flat-16P are electrically floating

Maturity status link
RHFL4913A

Features

- Operating input voltage from 3 V to 12 V
- Adjustable output voltage
- 3 A maximum guaranteed output current in SMD5C package, 2 A in Flat-16P
- Very low dropout voltage: 350 mV typ. @ 400 mA
- Embedded overtemperature and overcurrent protection
- Adjustable overcurrent limitation
- Very low noise: 40 μV_{RMS} (10 Hz-100 kHz)
- Output overload monitoring/signalling
- Inhibit (ON/OFF) TTL-compatible control
- Programmable output short-circuit current
- Remote sensing operation
- Low quiescent current: 1.5 mA typ. @ no load, 150 µA in shutdown
- Radiation hardness
  - TID : 300 krad(Si) RHA, ELDRS free up to 300 krad(Si)
  - SEL free up to 120 MeV.cm2/mg
  - SEU and SEFI immune up to 120 MeV.cm2/mg
- SET characterized
- QML-V qualified, SMD# 5962F02524

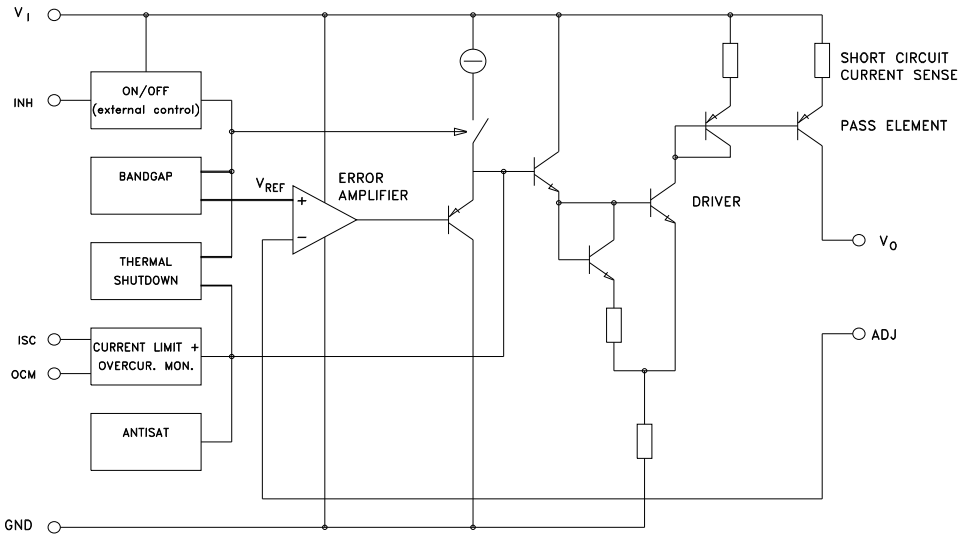
Description

The RHFL4913A is a high-performance adjustable positive voltage regulator, able to provide up to 2 A in Flat-16P and up to 3 A in SMD5C from a 3 to 12 Volt input voltage. The Flat-16P features a bottom metalization to maximize power dissipation.

The RHFL4913A features exceptional radiation hardness in both total ionization dose and single effect event. Both packages are made in ceramic and are hermetically sealed, allowing the product to be QML-V qualified for use in space. Its high reliability makes it also ideal for civil nuclear and other harsh environments.

1 Diagram

Figure 1. Block diagram



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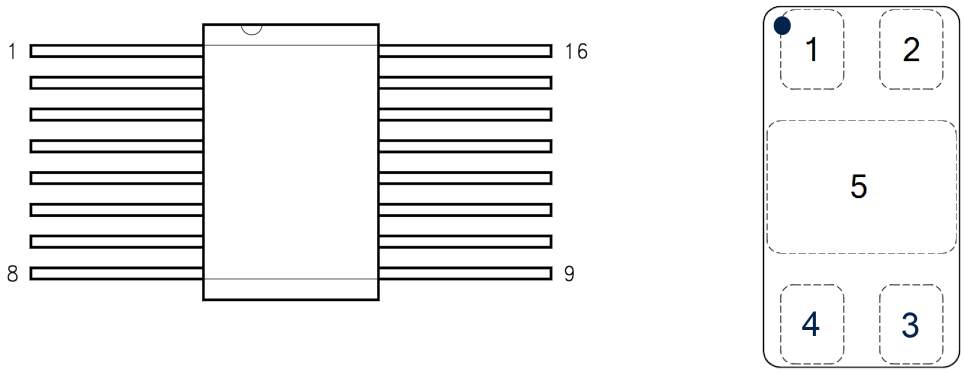
2 Pin configuration

Figure 2. **Pin configuration (top views)**



Flat-16P **SMD5C**

Table 1. **Pin description**

Pin name	Flat-16P (1)	SMD5C (2)
V_O	1, 2, 6, 7	1
V_I	3, 4, 5	4
GND	13	5
ISC	8	
OCM	10	
INHIBIT	14	3
ADJ	15	2
NC	9, 11, 12, 16	

1. *The upper metallic lid and the bottom metalization are not connected to any fix potential and are therefore electrically floating.*
2. *The upper metallic package lid is not connected to any fix potential and is therefore electrically floating.*

3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_I	DC input voltage Vi - V_{GROUND}		-0.3 to 14	V
V_O	DC output voltage range		-0.3 to V_I+0.3	V
V_{ADJ}	ADJ pin voltage		See note 1	V
V_{OCM}	OCM pin voltage		-0.3 to V_I+0.3	V
V_{ISC}	I_{SC} pin voltage vs GND		See note 2	A
$V_{INHIBIT}$	INIHBIT pin voltage		-0.3 to V_I+0.3	V
T_J	Maximum junction temperature		175	°C
P_D	Maximum power dissipation at 25 °C		15	W
T_{STG}	Storage temperature range		-65 to +150	°C
ESD	Electrostatic discharge capability	HBM	2.0	kV
		CDM	750	V

- **Note 1:** V_{ADJ} is internally maintained at 1.23 Volt. A forced excursion below - 0.3 Volt or above the smallest of (V_I + 0.3) and 3.93 Volt may permanently damage the product.
- **Note 2:** V_{ISC} may be pulled-up to V_I or left floating. A forced excursion below the lowest of -0.3 Volt and (V_I - 2.7) or above (V_I + 0.3) may permanently damage the product.

Table 3. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_I	DC input voltage V_I - V_{GROUND}		3 to 12	V
V_O	DC output voltage range		1.23 to 9	V
I_{OMAX}	Maxium output current	RHFL4913KPA	2	A
		RHFL4913SCA	3	A
Top	Operating junction temperature		-55 to +125	°C
P_D	TC = 25 °C power dissipation		15	W

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case, Flat-16P and SMD5C	8.3	°C/W
T_{SOLD}	Maximum soldering temperature, 10 sec.	300	°C

4 Electrical characteristics

Parameters in Table 5 are guaranteed over -55 to 125 °C and with $V_I = V_O + 2.5$ V, $C_I = C_O = 1$ µF, unless otherwise specified.

Table 5. Electrical characteristics

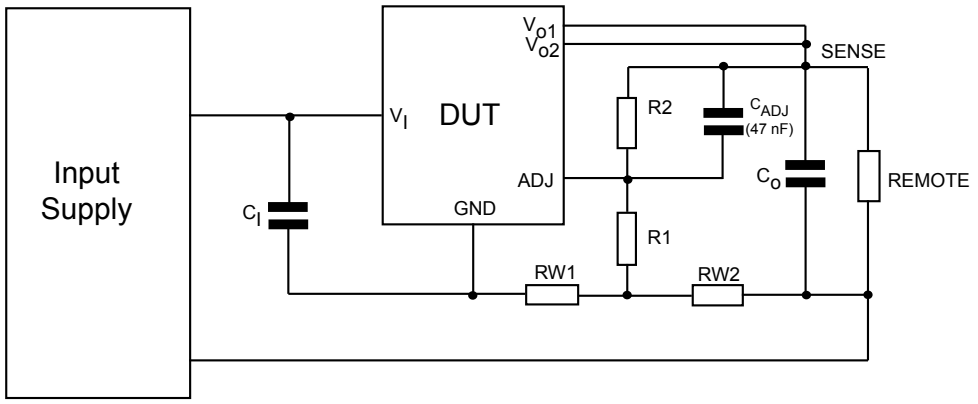
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_I	Operating input voltage	I_O = 1 A	3		12	V
V_O	Output voltage	I_O = 1 A for Flat-16P, I_O = 2 A for SMD5C, $V_O = V_{ADJ}$	1.19	1.23	1.27	V
		I_O = 1 A for Flat-16P, I_O = 2 A for SMD5C, V_O = 9 V	8.7		9.3	
$V_{OTDrift}$	Output voltage thermal drift	-55 °C to +125 °C, pre-radiation		40		ppm/°C
I_{OLIM}	Overcurrent protection limitation (1)	V_O = 0 Volt	0.8		2	A
$\Delta V_O/\Delta V_I$	Line regulation	$V_I = V_O$ +2.5 V to 12 V, I_O = 5 mA, T_J = +25 °C		0.07	0.35	%
		$V_I = V_O$ +2.5 V to 12 V, I_O = 5 mA, T_J = -55 °C		0.05	0.4	
		$V_I = V_O$ +2.5 V to 12 V, I_O = 5 mA, T_J = +125 °C		0.1	0.4	
		V_I = 3 V to 12 V, I_O = 5 mA, T_J = -55 °C to +125 °C		0.1	0.5	
$\Delta V_O/\Delta I_O$	Load regulation	$V_I = V_O$ + 2.5 V, I_O = 5 to 400 mA, T_J = +25 °C		0.04	0.3	%
		$V_I = V_O$ + 2.5 V, I_O = 5 to 400 mA, T_J = -55 °C		0.02	0.5	
		$V_I = V_O$ + 2.5 V, I_O = 5 to 400 mA, T_J = +125 °C		0.02	0.5	
		$V_I = V_O$ + 2.5 V, I_O = 5 mA to 1 A, T_J = +25 °C		0.08	0.5	
		$V_I = V_O$ + 2.5 V, I_O = 5 mA to 1 A, T_J = -55 °C		0.05	0.6	
		$V_I = V_O$ + 2.5 V, I_O = 5 mA to 1 A, T_J = +125 °C		0.04	0.6	
		V_I = 3 V, I_O = 5 mA to 1 A, T_J = -55 °C to +125 °C		0.1	0.7	
Z_{OUT}	Output impedance	I_O = 100 mA DC and 20 mA rms		100		mΩ
I_q	Quiescent current	$V_I = V_O$ + 2.5 V,		1.5	6	mA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_q	Quiescent current	I_O = 5 mA, ON mode (+25 °C)				mA
		$V_I = V_O$ + 2.5 V, I_O = 30 mA, ON mode (+25 °C)		2.7	8	
		$V_I = V_O$ + 2.5 V, I_O = 300 mA, ON mode (+25 °C)		11	25	
		$V_I = V_O$ + 2.5 V, I_O = 1 A, ON mode (+25 °C)		32	60	
		$V_I = V_O$ + 2.5 V, I_O = 3 A (2) ON mode (+25 °C)			150	
$I_{q(on)}$	Quiescent current ON mode	$V_I = V_O$ + 2.5 V, I_O = 30 mA, (-55 °C)		3	14	mA
		$V_I = V_O$ + 2.5 V, I_O = 300 mA, (-55 °C)		15	40	
		$V_I = V_O$ + 2.5 V, I_O = 1 A, (-55 °C)		52	100	
		$V_I = V_O$ + 2.5 V, I_O = 30 mA, (+125 °C)		3	8	
		$V_I = V_O$ + 2.5 V, I_O = 300 mA, (+125 °C)		8	20	
		$V_I = V_O$ + 2.5 V, I_O = 1 A, (+125 °C)		20	40	
$I_{q(off)}$	Quiescent current Shutdown mode	$V_I = V_O$ + 2 V, V_{INH} = 2.4 V, OFF mode		0.15	1	mA
V_d	Dropout voltage	I_O = 0 mA, V_O = 2.5 V to 9 V		130		mV
		I_O = 400 mA, V_O = 2.5 to 9 V, (+25 °C)		350	450	
		I_O = 400 mA, V_O = 2.5 to 9 V, (-55 °C)		300	400	
		I_O = 400 mA, V_O = 2.5 to 9 V, (+125 °C)		450	550	
		I_O = 1 A, V_O = 2.5 to 9 V, (+25 °C)		500	650	
		I_O = 1 A, V_O = 2.5 to 9 V, (-55 °C)		400	550	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_d	Dropout voltage	I_O = 1 A, V_O = 2.5 to 9 V, (+125 °C)		640	800	mV
		I_O = 2 A, V_O = 2.5 to 9 V, (+25 °C)		750		
		I_O = 2 A, V_O = 2.5 to 9 V, (+125 °C)		950		
$V_{INH(ON)}$	Inhibit voltage	I_O = 5 mA, T_J = -55 to +125 °C			0.8	V
$V_{INH(OFF)}$	Inhibit voltage	I_O = 5 mA, T_J = -55 to +125 °C	2.4			
SVR	Supply voltage rejection (1)	$V_I = V_O$ + 2.5 V ± 0.5 V, V_O = 3 V, I_O = 5 mA f = 120 Hz	60	70		dB
		$V_I = V_O$ + 2.5 V ± 0.5 V, V_O = 3 V, I_O = 5 mA f = 33 kHz	30	40		
I_{SHD}	Shutdown input current	V_{INH} = 5 V		15		µA
V_{OCM}	OCM pin voltage	Sinked I_{OCM} = 24 mA active low		0.38		V
t_{PLH}	Inhibit propagation delay (1)	$V_I = V_O$ + 2.5 V, V_{INH} = 2.4 V, I_O = 400 mA, V_O = 3 V	On to Off		20	µs
t_{PHL}			Off to On		100	µs
eN	Output noise voltage (1)	B = 10 Hz to 100 kHz, I_O = 5 mA to 2 A		40		µVrms

1. *These values are guaranteed by design., not tested in production.*
2. *SMD5C version only.*

Figure 3. Application diagram for remote sensing operation



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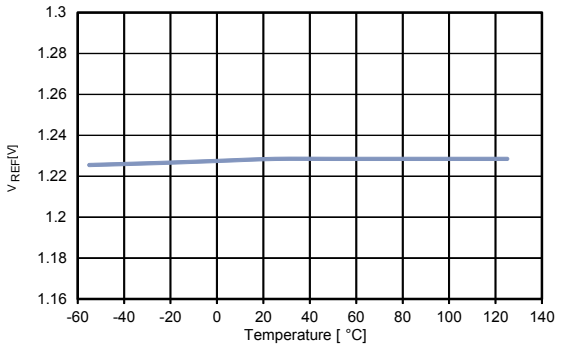
5 Typical characteristics

Figure 4. Reference voltage vs. temp. (V_{in} = V_{out} + 2.5 V)



Vin=Vout+2.5V, Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant), Iout =5mA

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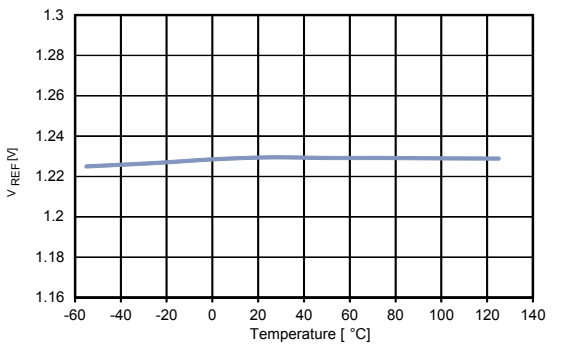
Figure 5. Reference voltage vs. temp. (V_{in} = 12 V)



Vin=12V, Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant), Iout =5mA

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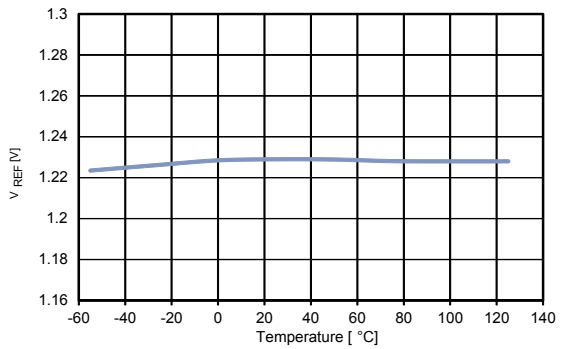
Figure 6. Reference voltage vs. temp. (V_{in} = V_{out} + 2.5 V, I_{out} = 1 A)



Vin=Vout+2.5V, Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant), Iout =1A

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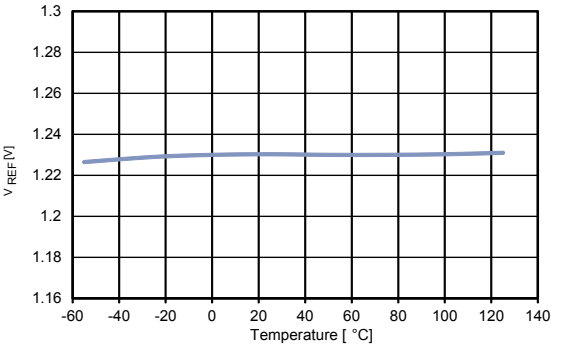
Figure 7. Reference voltage vs. temp. (V_{in} = 12 V, I_{out}= 1 A)



Vin=12V, Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant), Iout =1A

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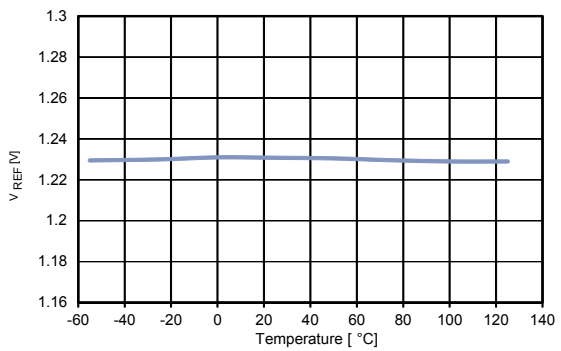
Figure 8. Reference voltage vs. temp. (V_{in} = V_{out} + 2.5 V, I_{out} = 2 A)



Vin=Vout+2.5V, Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant), Iout =2A

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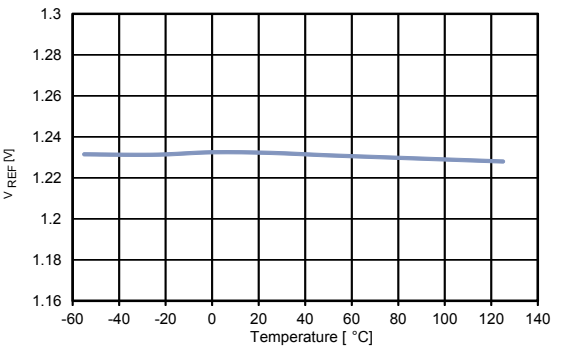
Figure 9. Reference voltage vs. temp. (V_{in} = 12 V, I_{out}= 2 A)



Vin=12V, Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant), Iout =2A

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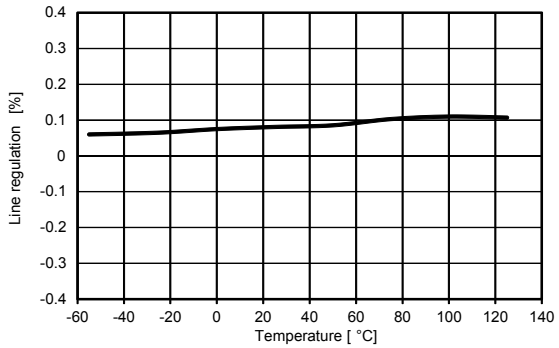
Figure 10. Line regulation vs. temperature



Vout+2.5V <Vin < 12V, Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant), Iout =5mA

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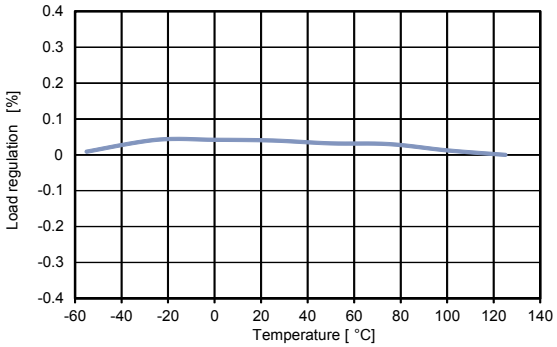
Figure 11. Load regulation vs. temp. (I_{out} = 5 mA to 400 mA)



Vin =Vout+2.5V , Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant), 5mA< Iout <0.4A

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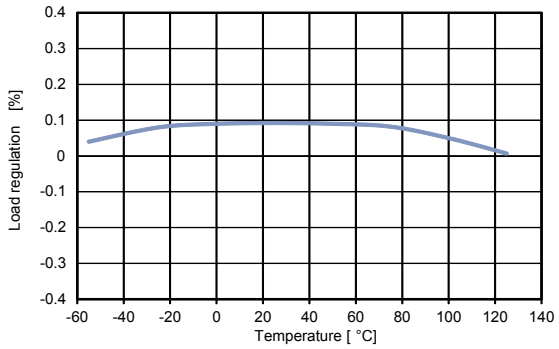
Figure 12. Load regulation vs. temp. (I_{out} = 5 mA to 1 A)



Vin =Vout+2.5V , Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant), 5mA< Iout <1A

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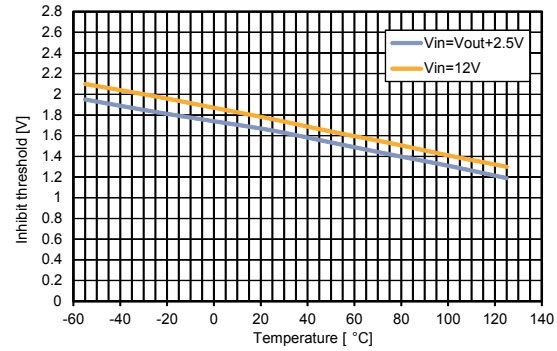
Figure 13. Inhibit threshold vs. temperature



Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant), no load

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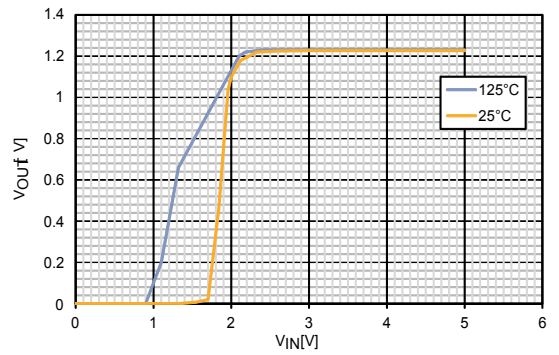
Figure 14. Output voltage vs. input voltage (I_{out} = 0 mA, T = 25 °C and T = 125 °C)



Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant), No load, T=25°C, T=125°C

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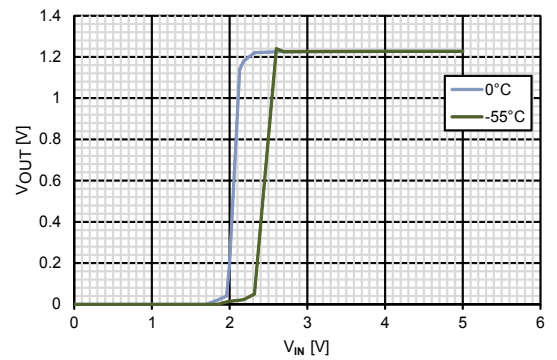
Figure 15. Output voltage vs. input voltage (I_{out} = 0 mA, T = 0 °C and T = -55 °C)



Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant), No load, T=0°C, T= -55 °C

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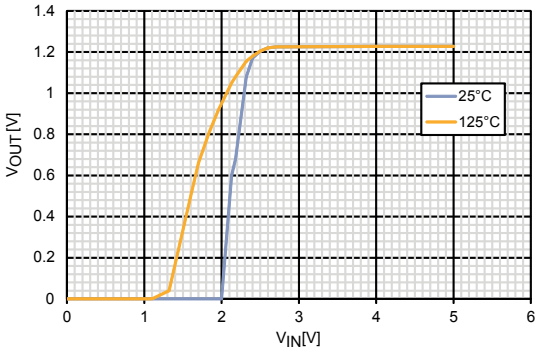
Figure 16. Output voltage vs. input voltage (I_{out} = 3 A, T = 25 °C and T = 125 °C)



Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant), Iout =3A, T=25°C, T=125°C

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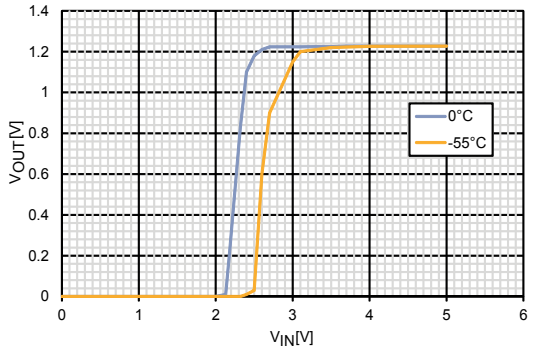
Figure 17. Output voltage vs. input voltage (I_{out} = 3 A, T = 0 °C and T = -55 °C)



Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant), Iout =3A, T=0°C, T= -55°C

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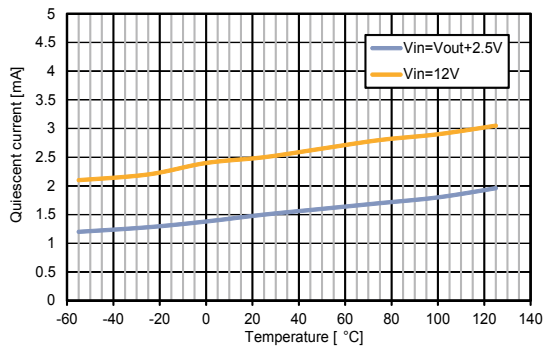
Figure 18. Quiescent current vs. temp. (no load)



Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant), No load

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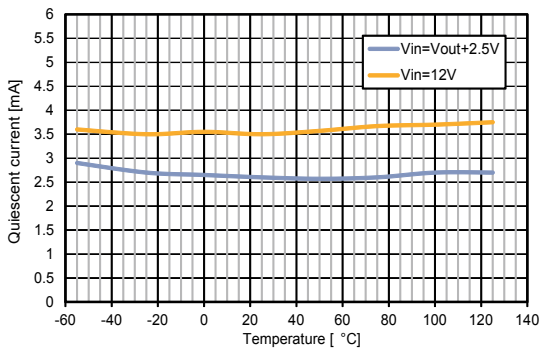
Figure 19. Quiescent current vs. temp. (I_{out} = 30 mA)



Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant), Iout = 30mA

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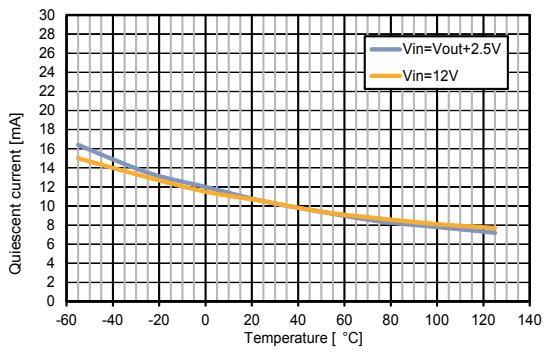
Figure 20. Quiescent current vs. temp. (I_{out} = 300 mA)



Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant), Iout = 300mA

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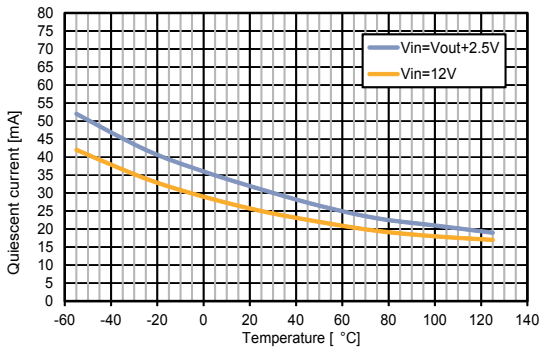
Figure 21. Quiescent current vs. temp. (I_{out} = 1 A)



Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant), Iout = 1A

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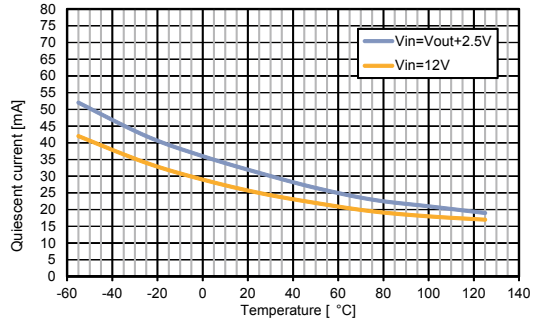
Figure 22. Quiescent current vs. temp. (I_{out} = 2 A)



Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant), Iout = 1A

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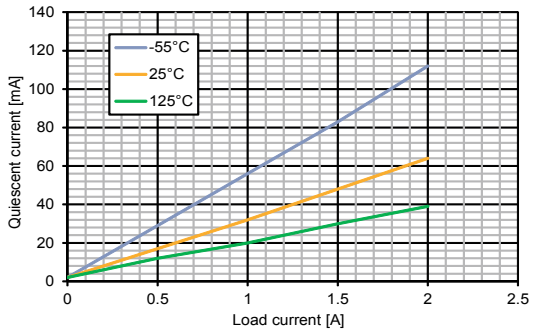
Figure 23. Quiescent current vs. load current, (V_{in} = V_{out} + 2.5 V)



Vin=Vout+2.5V, Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant)

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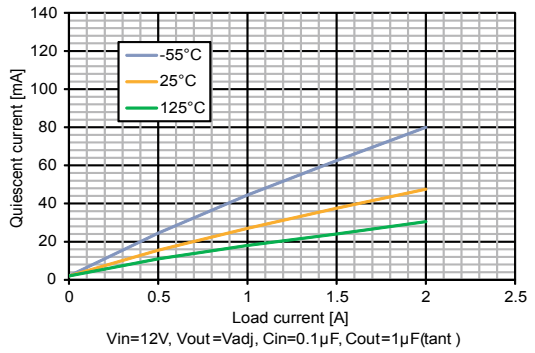
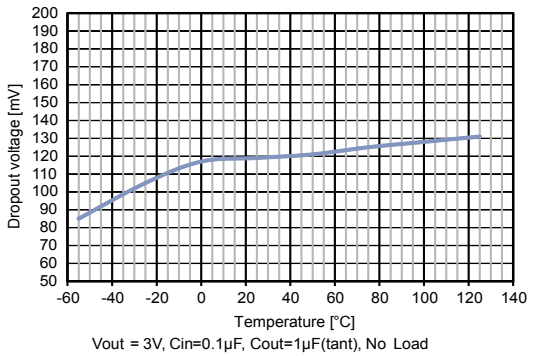
Figure 24. Quiescent current vs. load current, (V_{in} = 12 V)



Vin=12V, Vout =Vadj, Cin=0.1 µF, Cout=1 µF(tant)

AMG081120161325MT

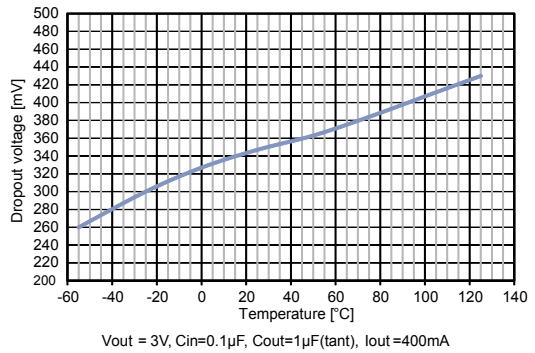
Figure 25. Dropout voltage vs. temp. (V_{out} = 3 V, no load)



Vout = 3V, Cin=0.1µF, Cout=1µF(tant), No Load

AMG081120161326MT

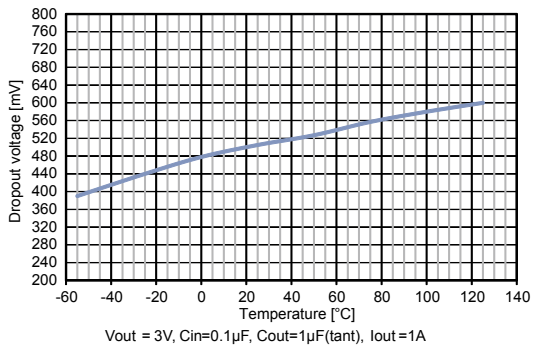
Figure 26. Dropout voltage vs. temp. (V_{out} = 3 V, I_{out} = 400 mA)



Vout = 3V, Cin=0.1µF, Cout=1µF(tant), Iout =400mA

AMG081120161327MT

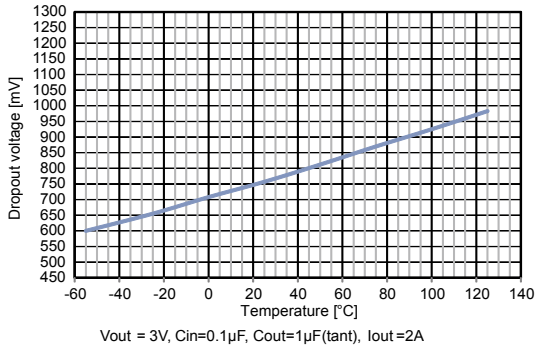
Figure 27. Dropout voltage vs. temp. (V_{out} = 3 V, I_{out} = 1 A)



Vout = 3V, Cin=0.1µF, Cout=1µF(tant), Iout =1A

AMG081120161328MT

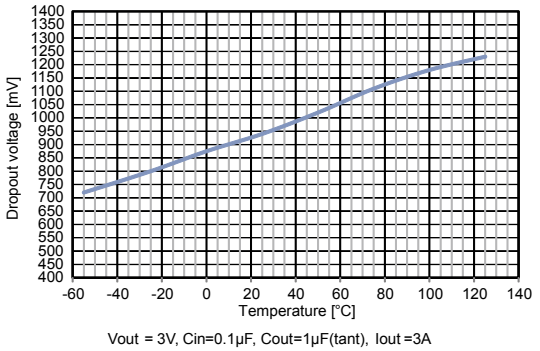
Figure 28. Dropout voltage vs. temp. (V_{out} = 3 V, I_{out}= 2 A)



Vout = 3V, Cin=0.1µF, Cout=1µF(tant), Iout =2A

AMG081120161329MT

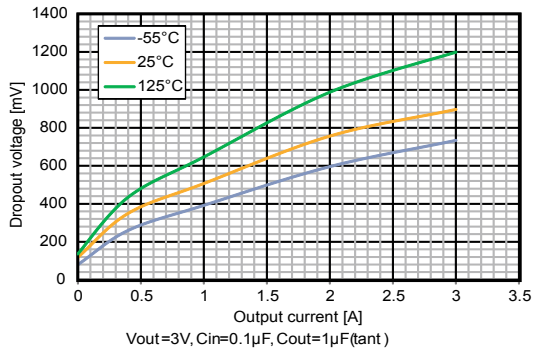
Figure 29. Dropout voltage vs. temp. (V_{out} = 3 V, I_{out}= 3 A)



Vout = 3V, Cin=0.1µF, Cout=1µF(tant), Iout =3A

AMG081120161330MT

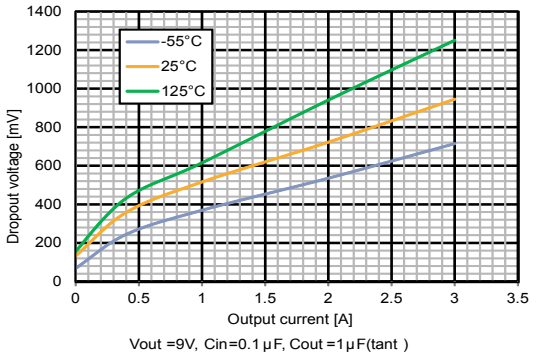
Figure 30. Dropout voltage vs. load current (V_{out} = 3 V)



Vout=3V, Cin=0.1µF, Cout=1µF(tant)

AMG081120161331MT

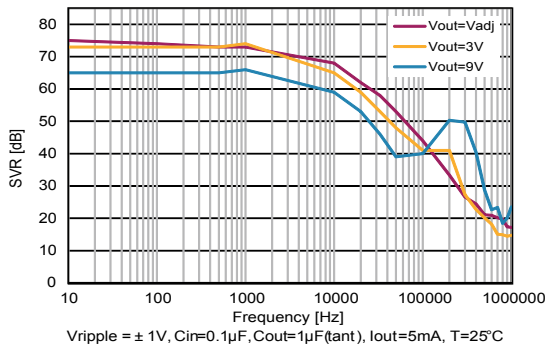
Figure 31. Dropout voltage vs. load current (V_{out} = 9 V)



Vout =9V, Cin=0.1 µF, Cout =1 µF(tant)

AMG081120161332MT

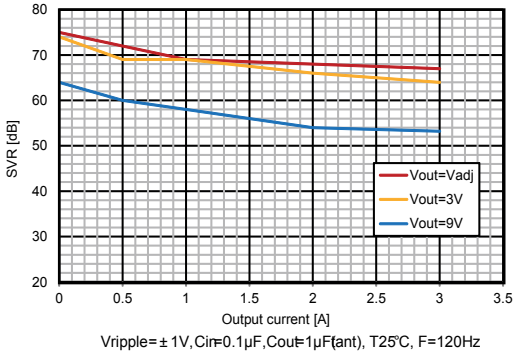
Figure 32. SVR vs. frequency



Vripple = ± 1V, Cin=0.1µF, Cout=1µF(tant), Iout=5mA, T=25°C

AMG081120161333MT

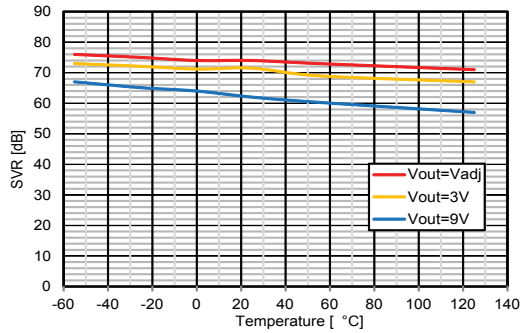
Figure 33. SVR vs. load current



Vripple= ± 1V, Cin=0.1µF, Cout=1µF(tant), T25°C, F=120Hz

AMG081120161334MT

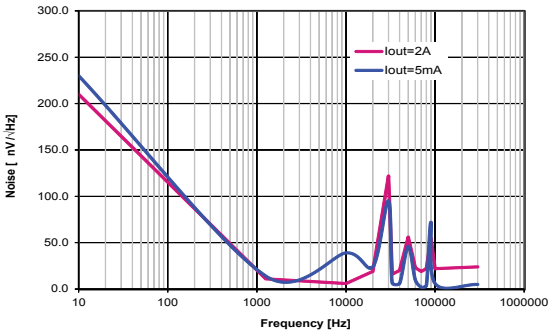
Figure 34. SVR vs. temperature



Vripple = ±1V, Iout =5mA, Cin=0.1µF, Cout=1µF(tant), T25°C, F=120Hz

AMG081120161335MT

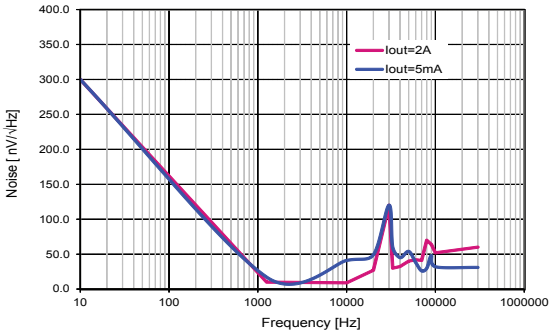
Figure 35. Output noise spectum (V_{out} = V_{adj})



V_{IN}=3.5V, V_{OUT} = V_{ADJ}, C_{IN}=220µF, C_{OUT}=220µF tantalum+0.47µF ceramic

AMG081120161336MT

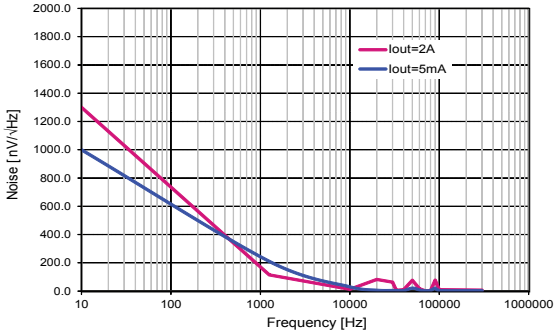
Figure 36. Output noise spectum (V_{out} = V_{adj}, C_{out} = 1 µF)



V_{IN}=3.5V, V_{OUT}=V_{ADJ}, C_{IN}=220µF, C_{OUT}=1µF tantalum

AMG081120161337MT

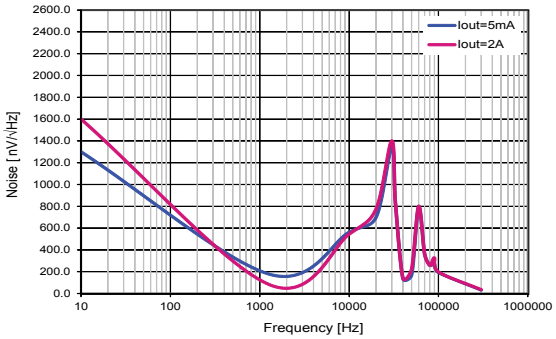
Figure 37. Output noise spectum (V_{out} = 9 V)



V_{IN}=11.5V , V_{OUT}=9V, C_{IN}=220µF, C_{OUT}=220µF tantalum+0.47µF ceramic

AMG081120161338MT

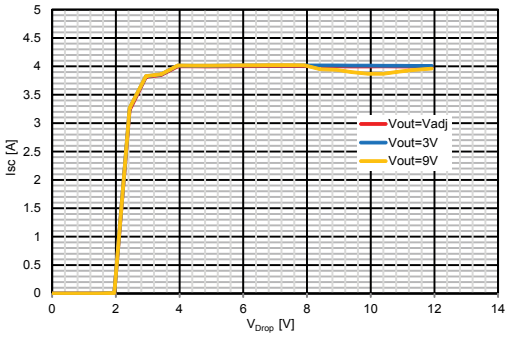
Figure 38. Output noise spectum (V_{out} = 9 V, C_{out} = 1 µF)



V_{IN}=11.5V , V_{OUT}=9V, C_{IN}=220µF, C_{OUT}=1µF tantalum

AMG081120161339MT

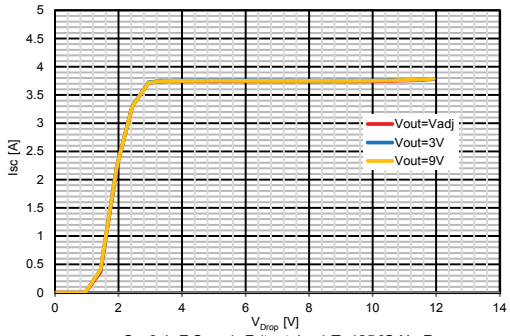
Figure 39. Short circuit current vs. dropout voltage (T = 25 °C)



C_{IN}=0.1µF,C_{OUT}=1µF (tantalum),T=25°C,No R_{SH}

AMG081120161340MT

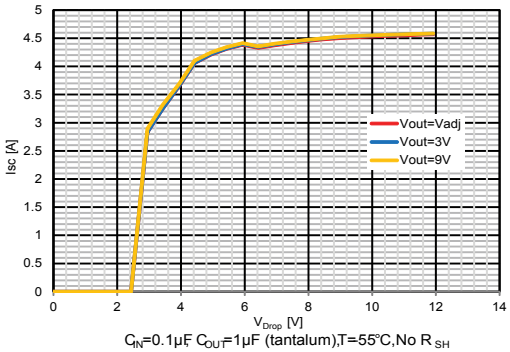
Figure 40. Short circuit current vs. dropout voltage (T = 125 °C)



C_{IN}=0.1µF, C_{OUT}=1µF (tantalum),T=125 °C,No R_{SH}

AMG081120161341MT

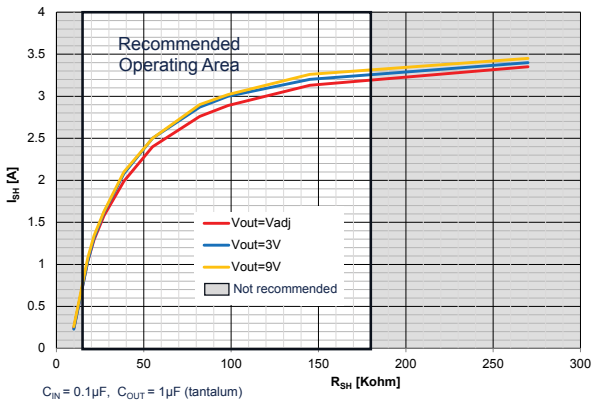
Figure 41. Short circuit current vs. dropout voltage (T = -55 °C)



C_{IN}=0.1µF, C_{OUT}=1µF (tantalum),T=55°C,No R_{SH}

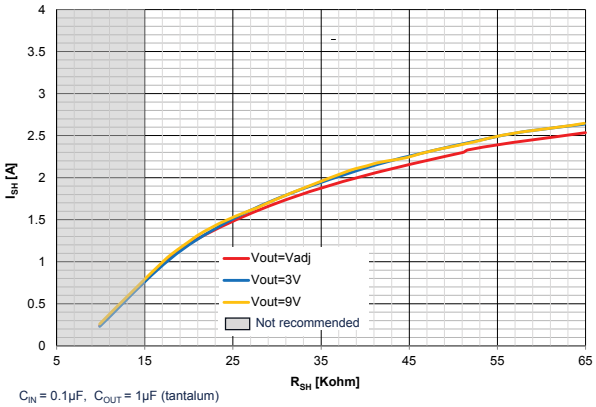
AMG081120161342MT

Figure 42. Short circuit current vs. R_{SH}



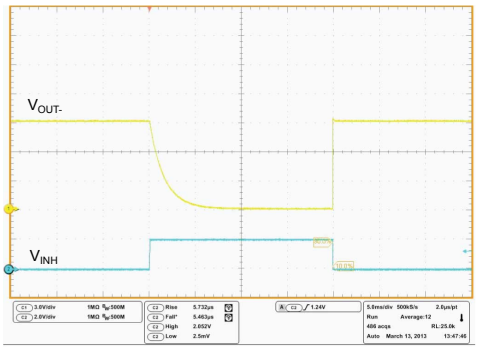
C_{IN} = 0.1µF, C_{OUT} = 1µF (tantalum)
I_{SHADJ} = I_{OLIM} x 1.6

Figure 43. Short circuit current vs. R_{SH} (zoom)



C_{IN} = 0.1µF, C_{OUT} = 1µF (tantalum)
I_{SHADJ} = I_{OLIM} x 1.6

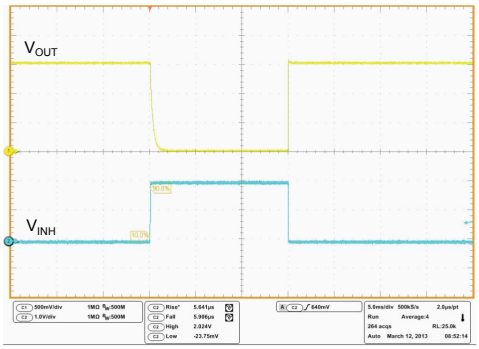
Figure 44. Enable turn-on/off (V_{out} = 9 V)



V_{IN}=12V; V_{INH} from 0V to 2V; V_{OUT}= 9V; I_{OUT}=5mA
C_{IN}=C_{OUT}=1µF; T_r=T_f=5µs

AMG081120161345MT

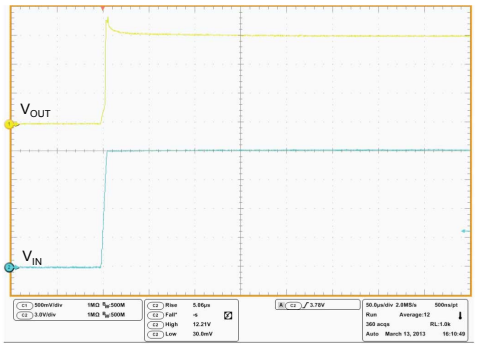
Figure 45. Enable turn-on/off (V_{out} = 1.5 V)



V_{IN}=4V; V_{INH} from 0V to 2V; V_{OUT}= 1.5V; I_{OUT}=5mA
C_{IN}=C_{OUT}=1µF; T_r=T_f=5µs

AMG081120161346MT

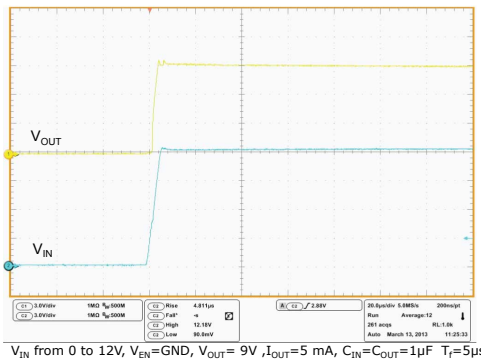
Figure 46. Turn-on time (V_{out} = 1.5 V)



V_{IN} from 0 to 12V, V_{EN}=GND, V_{OUT}= 1.5V ,I_{OUT}=5 mA, C_{IN}=C_{OUT}=1µF T_f=5µs

AMG081120161347MT

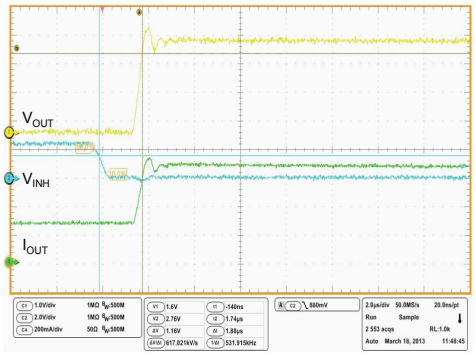
Figure 47. Turn-on time (V_{out} = 9 V)



V_{IN} from 0 to 12V, V_{EN}=GND, V_{OUT}= 9V ,I_{OUT}=5 mA, C_{IN}=C_{OUT}=1µF T_f=5µs

AMG081120161348MT

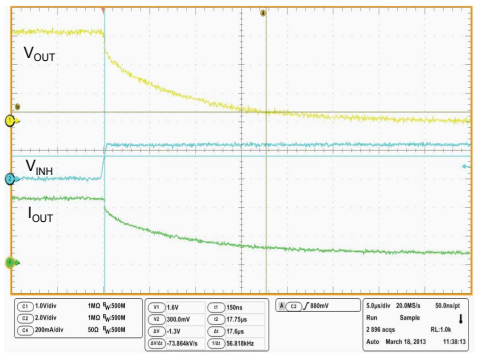
Figure 48. Inhibit propagation delay (Lo-Hi)



V_{IN}=5.5V, V_{INH}=from 2.4V to 0V, I_{OUT}=400mA,V_{OUT}=3V,C_{IN}=C_{OUT}=1µF, T_f=0.5µs

AMG081120161349MT

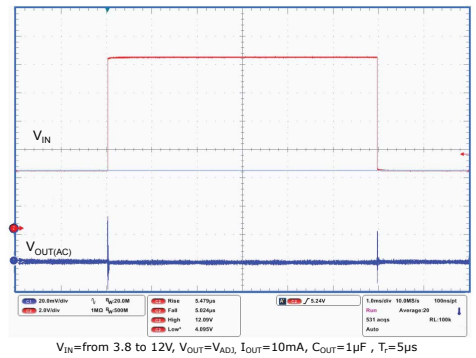
Figure 49. Inhibit propagation delay (Hi-Lo)



V_{IN}=5.5V, V_{INH}=from 0V to 2.4V, I_{OUT}=400mA,V_{OUT}=3V,C_{IN}=C_{OUT}=1µF, T_r=0.5µs

AMG081120161350MT

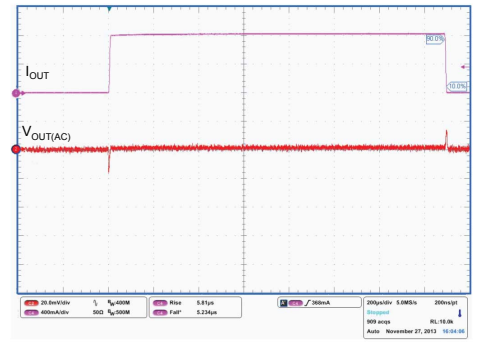
Figure 50. Line transient



V_{IN}=from 3.8 to 12V, V_{OUT}=V_{ADJ}, I_{OUT}=10mA, C_{OUT}=1µF , T_r=5µs

AMG081120161351MT

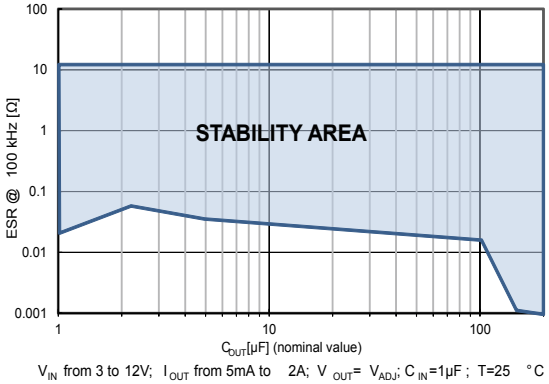
Figure 51. Load transient



V_{IN}= 3.8V, V_{OUT}=V_{ADJ}, I_{OUT}= from 0 to 800mA, C_{OUT}=1µF , T_r=5µs

AMG081120161352MT

Figure 52. **Stability plan ($V_{out} = V_{adj}$)**



V_{IN} from 3 to 12V; I_{OUT} from 5mA to 2A; V_{OUT}= V_{ADJ}; C_{IN}=1µF ; T=25 °C

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6 Radiations

6.1 Total ionizing dose

The RHFL4913A is RHA guaranteed at 300 rad(Si) and ELDRS immune up to 300 krad(Si) as per MIL-STD-883 TM 1019 cond A and D.

The TID has been characterized within the QML-V qualification as described below:

- MIL-STD-883 TM 1019 cond A compliant high dose rate test (between 50 and 300 rad/s) has been performed for the QML-V qualification up to 300 krad(Si).
- The qualification is completed by a low dose rate test (below 10 mrad(SI)/s) as per MIL-STD-883 TM1019 cond D up to 300 krad(Si) to cover the worst case of the bipolar structures the RHFL4913A is made of. Furthermore, the product successfully pass the Enhanced Low Dose Rate Susceptibility (ELDRS) conditions: low dose rate post radiation drift of all parameters stays less than 50% above its high dose rate value, making the RHFL4913A ELDRS immune up to 300 krad(Si).
- The post-irradiation electrical and timing characteristics are the same as the pre-irradiation ones. They are provided in table 4.

In addition, each wafer lot is submitted to a TID high dose rate MIL-STD-883 TP 1019 cond A acceptance test performed on 5 unbiased pieces from 3 wafers. The acceptance criteria is 0 fail.

6.2 Single event effects

The RHFL4913A has been characterized under heavy ions within the qualification of the product as described below:

- SEL test has been tested up to 120 MeV.cm2/mg.
- SET has been tested in various conditions of Vin, Vout, Iout and Vinhibit on a board populated with 2 different sets of external components and 6 bias conditions (see details on figure x and tables y and z below). Each configuration has been tested with 4 samples. The worst case SET Weibull curve is provided in figure x

Single event effect are not tested within the wafer lot acceptance test of production parts.

The SEE performance is summarized in Table 7. Complete SEE report is available upon request.

Figure 53. Radiation test board schematic

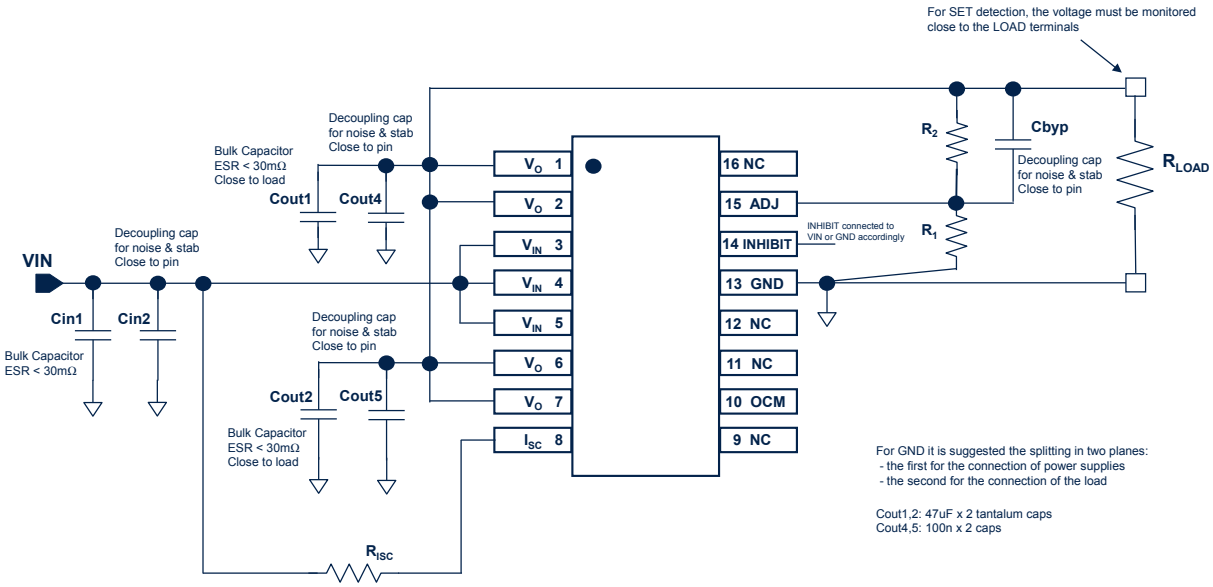


Table 6. SET test board hardware configurations

Test mode	Test configuration	
SET	Configuration 1	- Cin1 = 100 µF tantalum, ESR < 30 mΩ - Cout1 = Cout2 = 47 µF tantalum, < 30 mΩ - Cin2 = Cout4 = Cout5 = 100 nF polyester - Cbyp = 10 nF polyester - Risc = 40 kΩ (to achieve 2 A current limit)
	Configuration 2	- Cin1 = Cout1 = 220 µF tantalum, ESR < 30 mΩ - Cout2 = not connected - Cin2 = Cout4 = 100 nF polyester - Cout5 = not connected - Cbyp = 10 nF polyester - Risc = 40 kΩ (to achieve 2 A current limit)

Table 7. SET bias conditions tested

Test mode	Bias#	Bias conditions
SET	Bias 1	V_{IN} = 3 V, V_{OUT} =1.5 V (R1 = 1 kΩ, R2 = 200 Ω), $V_{INHIBIT}$ = 0 V, I_{OUT} = 1 A
	Bias 2	V_{IN} = 3 V, V_{OUT} = 1.5 V (R1 = 1 kΩ, R2 = 200 Ω), $V_{INHIBIT}$ = 3 V, I_{OUT} = 1 A
	Bias 3	V_{IN} = 3.3 V, V_{OUT} = 2.5 V, (R1 = 1 kΩ, R2 = 1 kΩ), $V_{INHIBIT}$ = 0 V, I_{OUT} = 150 mA
	Bias 4	V_{IN} = 7 V, V_{OUT} = 5 V, (R1 = 1 kΩ, R2 = 3 kΩ), $V_{INHIBIT}$ = 0 V, I_{OUT} = 300 mA
	Bias 5	V_{IN} = 9 V, V_{OUT} = 1.5 V, (R1 = 1 kΩ, R2 = 200 Ω), $V_{INHIBIT}$ = 0 V, I_{OUT} = 100 mA
	Bias 6	V_{IN} = 12 V, V_{OUT} = 9 V, (R1 = 1 kΩ, R2 = 6.2 kΩ), $V_{INHIBIT}$ = 0 V, I_{OUT} = 300 mA

Hardware configuration 1 – Bias condition 6

Table 8. Radiation hardness performance summary

Type	Parameter	Conditions	Value	Unit
TID		High dose rate RHA	300	krad(Si)
		Low dose rate		
		ELDRS		
	Output voltage post radiation drift	0 to 300 krad(Si) low dose rate (0.55 rad(Si)/s)	8	ppm/krad(Si)
		0 to 300 krad(Si) high dose rate MIL-STD-883J TM1019.9	6	
SEL	LET threshold	Up to 120 MeV.cm^2/mg, T = 125 °C, Fluence = 1.10^{+7} ion/cm²	120	MeV.cm²/mg
SET	LET threshold	Configuration 1, bias 1, 2, and 3	> 85	
		Configuration 2, bias 1, 2, and 3		

7 Device description

The RHFL4913A adjustable voltage regulator contains a PNP type power element controlled by a signal resulting from an amplified comparison between the internal temperature-compensated band-gap and the fraction of the desired output voltage value obtained from an external resistor divider bridge. The device is protected by several functional blocks.

7.1 ADJ pin

The load output voltage feedback comes from an external resistor divider bridge mid-point connected to the ADJ pin (allowing all possible output voltage settings as per user requirements) established between load terminals.

7.2 Inhibit ON-OFF control

By setting the INHIBIT pin TTL high, the device switches off the output current and voltage. The device is ON when the INHIBIT pin is set low. Since the INHIBIT pin is pulled down internally, it can be left floating in cases where the inhibit function is not used.

7.3 Overtemperature protection

A temperature detector internally monitors the power element junction temperature. The device turns off when a temperature of approximately 175 °C is reached, returning to ON mode when back to approximately 135 °C. Combined with the other protection blocks, the device is protected from destructive junction temperature excursions in all load conditions. It should be noted that when the internal temperature detector reaches 175 °C, the active power element can be as high as 225 °C. Prolonged operation under these conditions far exceeds the maximum operating ratings and device reliability cannot be guaranteed.

7.4 Configurable overcurrent protection

An internal non-fold-back short circuit over-current limitation limits by default the short circuit output current I_{SH} at typically 3.6 A when pin ISC is left floating. This overcurrent limitation is primarily designed to protect the device itself.

In the Flat-16P packaged version, the overcurrent limitation can be used as a basic adjustable overcurrent protection of the load. However, to secure proper startup of the regulator in all conditions, the current limit must comply with the guidelines provided below.

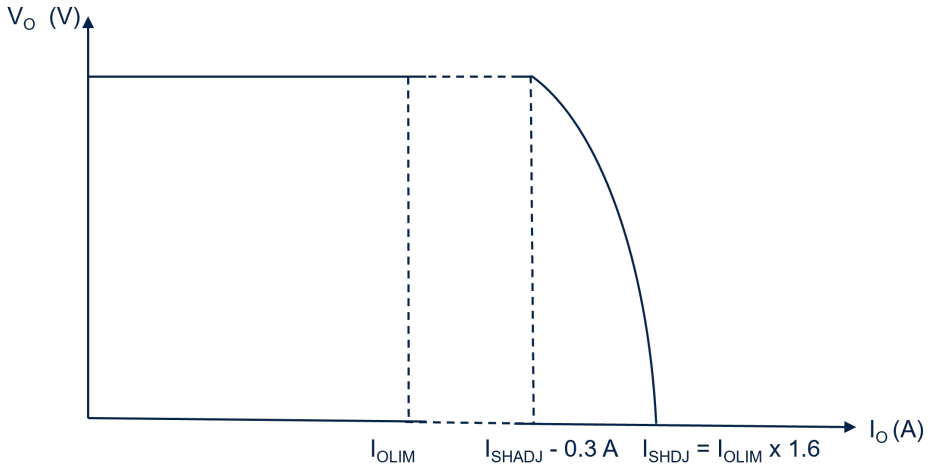
The overcurrent protection must be set above the maximum current required by the load in worst case conditions, including temperature and radiations, but low enough to be an effective protection. Furthermore, this I_{OLIM} value must be within the limits specified in the electrical specification in Table 5.

Once I_{OLIM} is defined, I_{SHADJ} is calculated by applying the formula $I_{SHADJ} = I_{OLIM} \times 1.6$ to account for the 0.3 A where the protection is active (see Figure 54), for the temperature and radiation drifts as well as for the part to part variations of the default ISH and the protection circuits.

Figure 42 and Figure 43 allow to define the typical value of the RSH resistors to be connected between pins ISC and V_I to set ISH_{ADJ} at the desired value.

When I_O reaches I_{OLIM}, the current protection progressively reduces the effectiveness of the regulation. When IO reaches I_{SHADJ} - 0.3 A, the current limiter overrules the regulation (see Figure 54), leading V_O to drop and OCM flag to raise.

Figure 54. I_{OLIM} setting guardband vs I_{SHADJ}



I_{SH} drift down of typically 5 mV between 25 °C and 125 °C and and raises of typically 15 mA between 25 °C and -55 °C.

The impact of total ionizing dose on I_{SH}, as measured on few pieces from 3 wafers from the same wafer lot up to 300 krad(Si), is a drift up to few percent, negative or slightly positive.

7.5 OCM pin

The OCM pin goes low when the current limit becomes active, otherwise $V_{OCM} = V_I$. It is buffered and can sink 10 mA. The OCM pin is internally pulled up by a 5 kΩ resistor.

8 Application information

To adjust the output voltage, the R2 resistor must be connected between the V_O and ADJ pins. The R1 resistor must be connected between ADJ and ground. Resistor values can be derived from the following formula:

$V_O = V_{ADJ}$ (R1+ R2) / R1

The V_{ADJ} is typically 1.23 V, controlled by the internal temperature-compensated band gap block.

The minimum input voltage is 3 V. The RHFL4913A adjustable is functional as soon as the V_I - V_O voltage difference is slightly above the power element saturation voltage. The adjust pin to ground resistor (R1) value must not be greater than 10 kΩ, in order to keep the output feedback error below 0.2 %. A minimum of 0.5 mA I_O must be set to ensure perfect no-load regulation. It is advisable to dissipate this current into the divider bridge resistor.

All available V_I pins, as well as all available V_O pins, should always be externally interconnected, otherwise the stability and reliability of the device cannot be guaranteed.

The inhibit function switches off the output current electronically, and therefore very quickly. According to Lenz's law, external circuitry reacts with LdI/dt terms which can be of high amplitude in case somewhere a serial coil inductance exists. Large transient voltage would develop on both device terminals. It is advisable to protect the device with Schottky diodes to prevent negative voltage excursions. In the worst case, a 14 V Zener diode could protect the device input.

Since the RHFL4913A adjustable voltage regulator is manufactured with very high speed bipolar technology (6 GHz f_T transistors), the PCB layout must be designed with great care, with very low inductance and low mutually coupling lines. Otherwise, high frequency parasitic signals may be picked up by the device resulting in system self-oscillation. The benefit is an SVR performance extended to far higher frequencies.

8.1 Output capacitor selection and stability.

The device has been designed for high stability and low dropout operation.

To ensure regulator stability, input and output capacitors with a minimum 1 µF are mandatory. When large transient currents are expected, larger value capacitors are necessary. The detailed stability plane versus output capacitance and ESR is shown in Figure 52. Stability plan ($V_{out} = V_{adj}$).

In the case of high current operation with short circuit events expected, caution must be exercised with regard to capacitors. They must be connected as close as possible to the device terminals. As some tantalum capacitors may permanently fail when subjected to high charge-up surge currents, it is recommended to decouple them with 470 nF polyester capacitors.

8.2 Remote sensing operation

A separate kelvin voltage sensing line provides the ADJ pin with exact load "high potential" information (see Figure 3. Application diagram for remote sensing operation). But variable remote load current consumption induces variable Iq current (Iq is roughly the I_O current divided by the h_{FE} of the internal PNP series power element) routed through the parasitic series line resistor RW2. To compensate for this parasitic voltage, resistor RW1can be introduced to provide the necessary compensating voltage signal to the ADJ pin.

A ceramic or poliester 47nF C_{ADJ} capacitor between ADJ and V_{OUT} pins is recommended when the remote sensing technique is implemented.

8.3 FPGA power supply lines

FPGA being very sensitive to V_{DD} transients beyond a few % of their nominal supply voltage, special attention must be given to mitigate possible SET induced disturbances. The worst-case heavy ion effect occurs when the RHFL4913A internal control loop is open or short-circuited for a sub-microsecond duration. During such events, the RHFL4913A power element can provide important up or down variations of I_O for a duration of about one microsecond, after which time the RHFL4913A smoothly recovers to nominal operation.

Low duration SET may also be caused by layout dependent stray inductances. Simulations show that such SETs last less than 100 ns. Proper PCB layout allows to mitigate them, and worst case, dramatically reduce their duration and amplitude (no more than 90 mV deviation observed in simulation).

Such mitigations include:

- Minimizing series/parallel parasitic inductances of the PCB path

- Using an effective grounding scheme with short connections to GND, such as a star-bus topology, whose board GND is at the GND force. The best solution is a ground plane.
- Using a low ESR 47 µF C_{OUT} filtering capacitor, with ESR lower than 30 mΩ, together with a 470 nF ceramic capacitor in parallel (to reduce dynamic ESR)
- Implementing the SET mitigation circuit, by adding additional filtering components as described in Figure 55. Baseline bias configuration with remote feedback and Figure 56. Local feedback configuration.

Additional comments on SET mitigation techniques for linear voltage regulators can be found in AN2984 (“Minimizing the SET-related effects on the output of a voltage linear regulator, available on www.st.com).

Figure 55. Baseline bias configuration with remote feedback

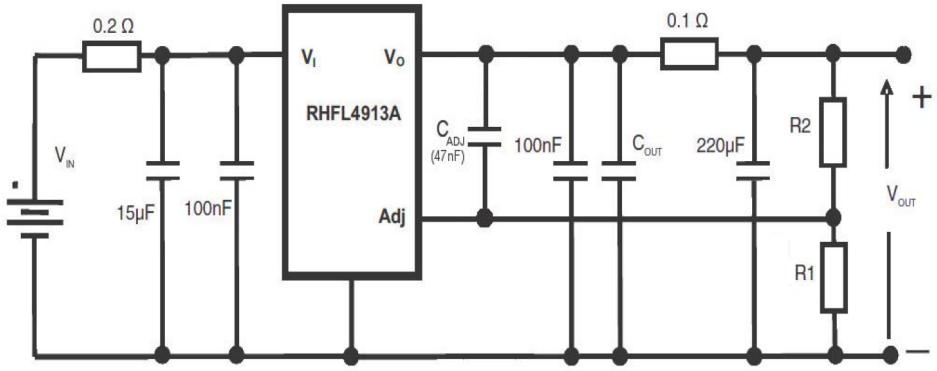
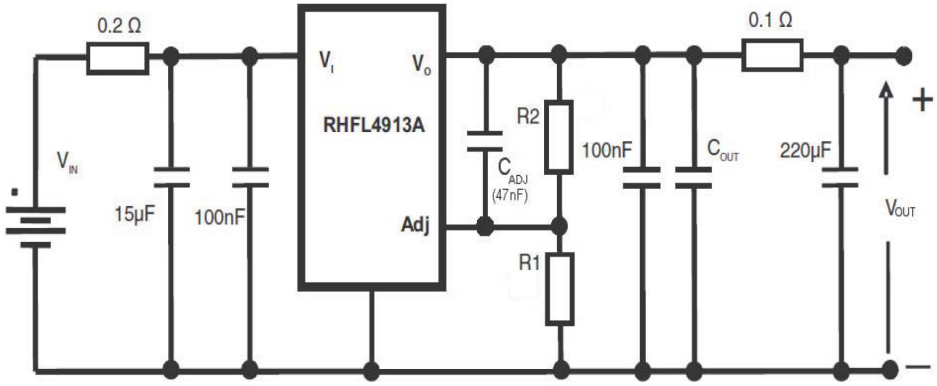


Figure 56. Local feedback configuration

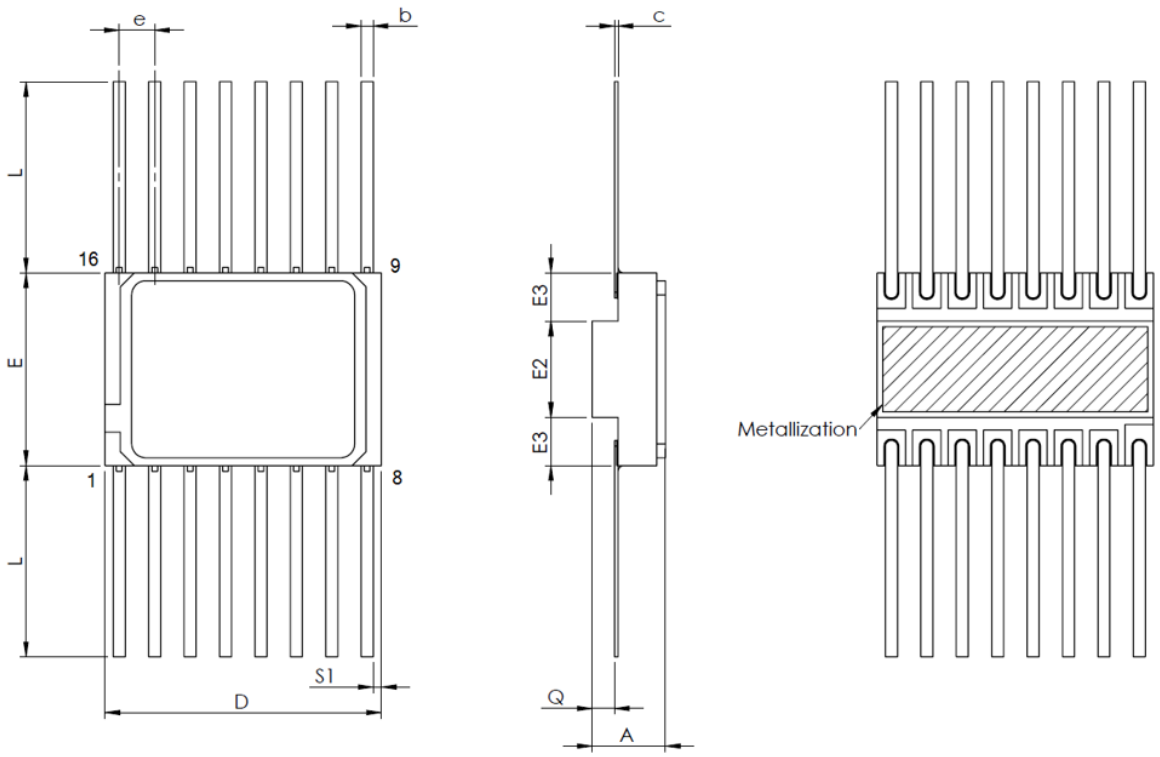


9 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 Flat-16P package information

Figure 57. **Flat-16P package outline**



1: The metalic lid and the bottom metalization are floating.

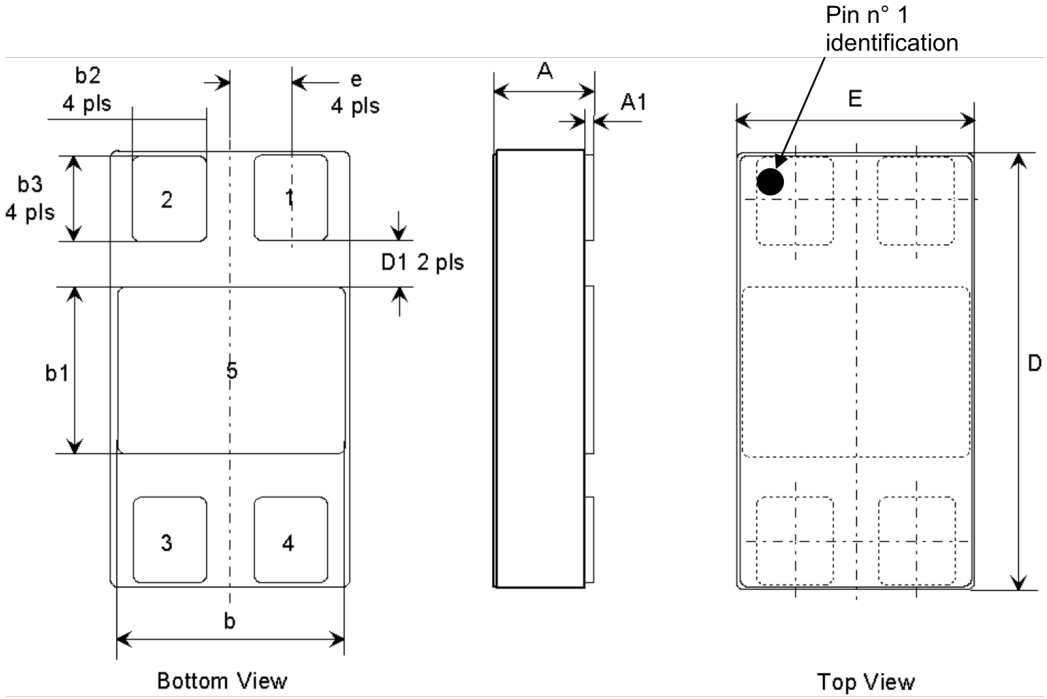
2: The bottom section of the Flat-16P package is metallized, allowing it to be brazed onto PCB, to maximize power dissipation. However, the Flat-16P AlN ceramic, while featuring a superior dissipation, has a low thermal coefficient of expansion. Brazing it therefore implies proper selection and layout of the PCB as well as adequate mounting process design and qualification to ensure the quality of the mounting. Failure to do so could lead to failing the thermal cycling test usually required for space.

Table 9. **Flat-16P package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.42		2.88
b	0.38		0.48
c	0.10		0.18
D	9.71		10.11
E	6.71		7.11
E2	3.30	3.45	3.60
E3	0.76		
e		1.27	
L	6.35		7.36
Q	0.66		1.14
S1	0.13		

9.2 SMD5C package information

Figure 58. **SMD5C package outline**



Note: The metalic lid is floating.

Table 10. **SMD5C package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.99	3.15	3.30
A1	0.25	0.38	0.51
b	7.13	7.26	7.39
b1	4.95	5.08	5.21
b2	2.28	2.41	2.54
b3	2.92	3.05	3.18
D	13.71	13.84	13.97
D1	0.76		
E	7.39	7.52	7.65
e		1.91	

10 Ordering information

Table 11. Ordering information

Order code [1]	SMD pin	Quality level	Package	Lead finish	Marking [2]	Packing	mass (g)
RHFL4913KPA1	-	Engineering Model	Flat-16P	Gold	RHFL4913KPA1	Strip Pack	0.60
RHFL4913KPA-01V	5962F0252401VXC	QML-V		Gold	5962F0252401VXC	Strip Pack	
RHFL4913KPA-02V	5962F0252401VXA	QML-V		Solder dip	5962F0252401VXA	Strip Pack	
RHFL4913SCA1	-	Engineering Model	SMD5C	Gold	RHFL4913SCA1	Strip Pack	1.25
RHFL4913SCA07V	5962F0252403VUC	QML-V		Gold	5962F0252403VUC	Strip Pack	

1. *Contact ST sales representative for information about specific conditions for product in die form and other quality levels.*
2. *Specific marking only. See section xx for complete marking information.*

11 Other information

11.1 Product marking

The marking of the parts is described in table y and figures x for flight model and figure y for engineering model

Figure 59. **Product marking outline, flight model**

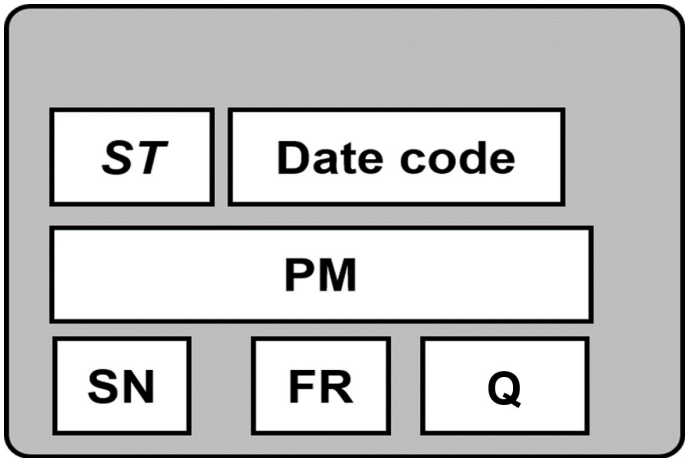


Figure 60. **Product marking outline, engineering model**

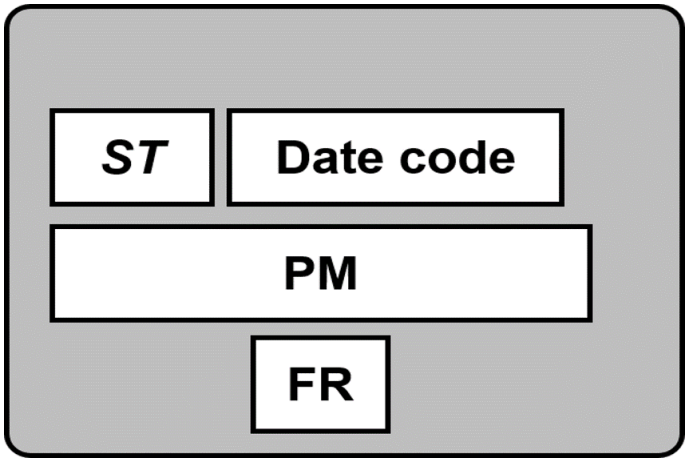


Table 12. **Product marking**

Field	Description
ST	ST logo
Date code	YYWWA format: - YY : year's last 2 digits - WW : week of the year - A : lot in the week
PM	Specific product marking (see table w)
SN	Serial number
FR	Country of origin
Q	QML-V logo

11.2 Product documentation

Each product shipment includes a set of associated documentation within the shipment box . This documentation depends on the quality level of the products, as detailed Table 13.

By default, the documentation is provided on CDROM(1) , and an additional paper copy of the certificate of conformance is provided. Contact ST sales representative for information of optional documentation and digital data transfer.

Note: Contact your ST representative for information about secured ftp transfer.

Table 13. Default documentation by quality level

Quality level	Item
Engineering Model	Certificate of conformance including: • Customer name • Customer purchase order number • ST sales order number & item • ST part number • Quantity delivered • Date code • Reference to ST datasheet reference to TN1181 on engineering models • ST Rennes assembly lot ID
QML-V Flight	Certificate of conformance including: • Customer name • Customer purchase order number • ST sales order number & item • ST part number • Quantity delivered • Date code • Serial numbers • Group C reference • Group D reference • Reference to the applicable • SMD ST Rennes assemblyy lot ID
	Quality Control Inspection (groups A, B, C, D, E)
	Screening electrical data
	Precap report
	PIND (1) test
	SEM (2) inspection report
	W-Ray Report

1. *PIND : Particle Impact Noise Detection.*
2. *SEM : Scanning Electronic Microscope.*

Revision history

Table 14. **Document revision history**

Date	Revision	Changes
29-Oct-2004	3	New order codes added - Tables 4 and 5.
27-May-2005	4	Features, Tables 4, 5 and the Figure 1 has been updated. Add the Mechanical Data SOC-16.
08-Jun-2005	5	Mistake on Table 4 (Q.ty Level), Table 7 has been updated and add DIE Information.
30-Jan-2006	6	Added new package SMD5C and removed old package SOC-16.
26-Jan-2007	7	DIE Information and DIE Pad has been updated par. 6, pages 9 and 10.
23-Nov-2007	8	Pin information for the SMD5C package updated in Table 1; added section 6.3: FPGA power supply lines on page 10. Minor text changes.
22-Sep-2008	9	Modified Application information on page 9.
17-Nov-2008	10	Modified Table 8 on page 26.
21-Jan-2010	11	Modified Table 7 on page 26.
18-Oct-2010	12	Modified Section 6.2 on page 9.
07-Feb-2011	13	Added: note Table 1 on page 3.
07-Dec-2011	14	Removed the note under Table 1 on page 3 and added footnotes 1 and 2.
20-Aug-2012	15	Order code updated in Table 7 on page 26 about the SMD5C package
15-Jan-2014	16	Updated Features in cover page. Added Section 7: Typical characteristics. Modified Table 4: Electrical characteristics. Updated Section 9: Package mechanical data and Section 10: Ordering information. Minor text changes.
05-May-2014	17	Updated Figure 18: Output voltage vs input voltage (I_{out} = 3 A, T = 25 °C and T = 125 °C). Minor text changes.
22-Nov-2016	18	Updated description in cover page. Updated Section 9: "Package information". Minor text changes.
30-Mar-2018	19	Updated: - Figure 5. Baseline bias configuration with remote feedback and Figure 6. Local feedback configuration. - Section 6.4 Notes on the 16-pin hermetic package. - Section 9 Ordering information.
27-Apr-2018	20	Updated: Section 3 Maximum ratings.
08-Feb-2019	21	Minor text change in Description on the cover page.
10-Jul-2025	22	Updated figure, features and description on the cover page, Figure 2, Section 3, Section 7.4, Figure 42, Figure 43 and Section 9.2: SMD5C package information. Added new section Section 6: Radiations.

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