

## 8-Mbit (1M x 8) Static RAM

### Features

- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 110 \text{ mA}$
- Low CMOS standby power
  - $I_{SB2} = 20 \text{ mA}$
- 2.0V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Available in lead-free 36-ball FBGA and 44-pin TSOP II ZS44 packages

### Functional Description<sup>[1]</sup>

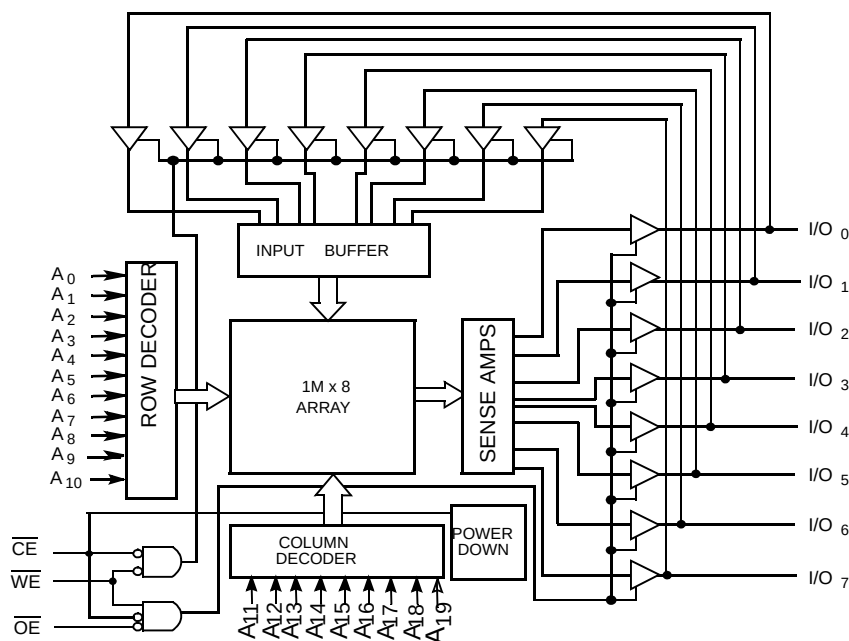
The CY7C1059DV33 is a high-performance CMOS Static RAM organized as 1M words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ), and tri-state drivers. Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a Write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1059DV33 is available in 36-ball FBGA and 44-pin TSOP II package with center power and ground (revolutionary) pinout.

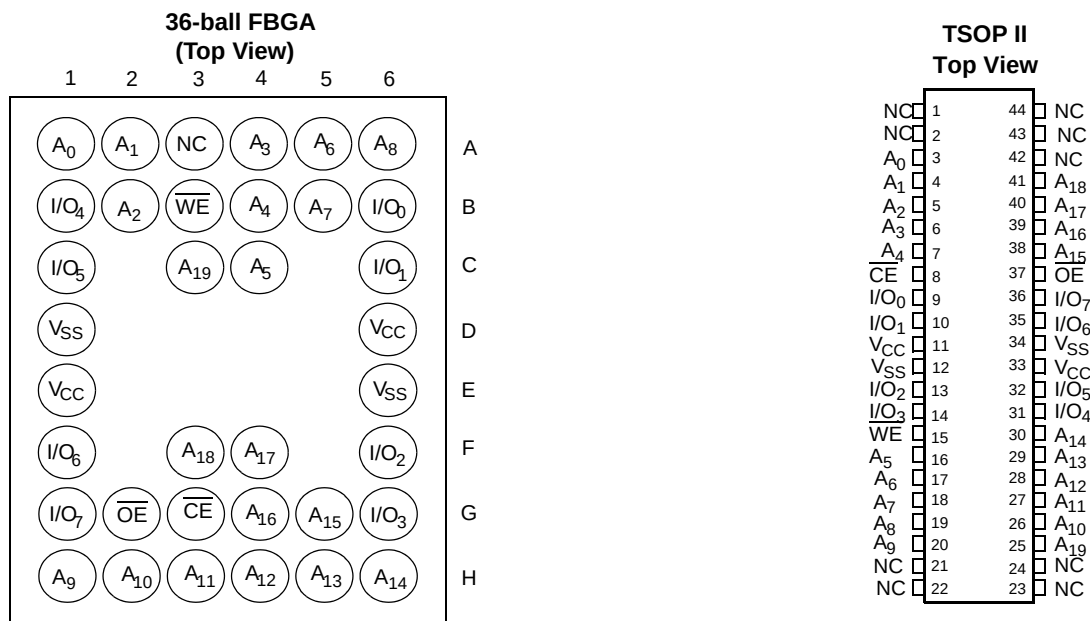
### Logic Block Diagram



#### Note:

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

## Pin Configuration



## Selection Guide

|                              | <b>-10</b> | <b>Unit</b> |
|------------------------------|------------|-------------|
| Maximum Access Time          | 10         | ns          |
| Maximum Operating Current    | 110        | mA          |
| Maximum CMOS Standby Current | 20         | mA          |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[2]</sup> .... -0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State<sup>[2]</sup> ..... -0.3V to  $V_{CC} + 0.3V$

DC Input Voltage<sup>[2]</sup> ..... -0.3V to  $V_{CC} + 0.3V$

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... >200 mA

## Operating Range

| Range      | Ambient Temperature | $V_{CC}$    |
|------------|---------------------|-------------|
| Industrial | -40°C to +85°C      | 3.3V ± 0.3V |

## Electrical Characteristics Over the Operating Range

| Parameter | Description                                  | Test Conditions                                                                                                    | -10  |                | Unit |
|-----------|----------------------------------------------|--------------------------------------------------------------------------------------------------------------------|------|----------------|------|
|           |                                              |                                                                                                                    | Min. | Max.           |      |
| $V_{OH}$  | Output HIGH Voltage                          | $V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$                                                                   | 2.4  |                | V    |
| $V_{OL}$  | Output LOW Voltage                           | $V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$                                                                    |      | 0.4            | V    |
| $V_{IH}$  | Input HIGH Voltage                           |                                                                                                                    | 2.0  | $V_{CC} + 0.3$ | V    |
| $V_{IL}$  | Input LOW Voltage <sup>[2]</sup>             |                                                                                                                    | -0.3 | 0.8            | V    |
| $I_{IX}$  | Input Leakage Current                        | $GND \leq V_I \leq V_{CC}$                                                                                         | -1   | +1             | μA   |
| $I_{OZ}$  | Output Leakage Current                       | $GND \leq V_{OUT} \leq V_{CC}$ , Output Disabled                                                                   | -1   | +1             | μA   |
| $I_{CC}$  | $V_{CC}$ Operating Supply Current            | $V_{CC} = \text{Max.}, f = f_{MAX} = 1/t_{RC}$                                                                     |      |                | mA   |
|           |                                              | 100 MHz                                                                                                            |      | 110            |      |
|           |                                              | 83 MHz                                                                                                             |      | 100            |      |
|           |                                              | 66 MHz                                                                                                             |      | 90             |      |
|           |                                              | 40 MHz                                                                                                             |      | 80             |      |
| $I_{SB1}$ | Automatic CE Power-down Current —TTL Inputs  | Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$         |      | 40             | mA   |
| $I_{SB2}$ | Automatic CE Power-down Current —CMOS Inputs | Max. $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ , or $V_{IN} \leq 0.3V$ , $f = 0$ |      | 20             | mA   |

## Capacitance<sup>[3]</sup>

| Parameter | Description       | Test Conditions                                            | Max. | Unit |
|-----------|-------------------|------------------------------------------------------------|------|------|
| $C_{IN}$  | Input Capacitance | $T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 3.3V$ | 16   | pF   |
| $C_{OUT}$ | I/O Capacitance   |                                                            | 16   | pF   |

## Thermal Resistance<sup>[3]</sup>

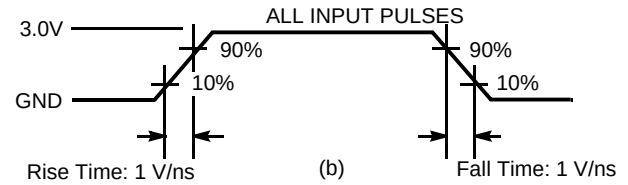
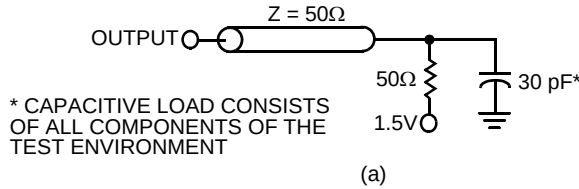
| Parameter     | Description                              | Test Conditions                                                         | FBGA | TSOP II | Unit |
|---------------|------------------------------------------|-------------------------------------------------------------------------|------|---------|------|
| $\theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | TBD  | TBD     | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction to Case)    |                                                                         | TBD  | TBD     | °C/W |

### Notes:

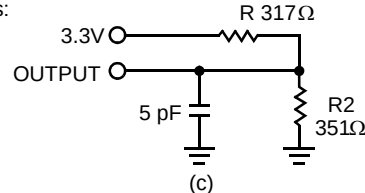
2.  $V_{IL}$  (min.) = -2.0V and  $V_{IH}$  (max.) =  $V_{CC} + 2V$  for pulse durations of less than 20 ns.

3. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms<sup>[4]</sup>



High-Z characteristics:



## AC Switching Characteristics<sup>[5]</sup> Over the Operating Range

| Parameter                         | Description                                      | -10  |      | Unit |
|-----------------------------------|--------------------------------------------------|------|------|------|
|                                   |                                                  | Min. | Max. |      |
| Read Cycle                        |                                                  |      |      |      |
| t <sub>power</sub> <sup>[6]</sup> | V <sub>CC</sub> (typical) to the first access    | 100  |      | μs   |
| t <sub>RC</sub>                   | Read Cycle Time                                  | 10   |      | ns   |
| t <sub>AA</sub>                   | Address to Data Valid                            |      | 10   | ns   |
| t <sub>OHA</sub>                  | Data Hold from Address Change                    | 3    |      | ns   |
| t <sub>ACE</sub>                  | $\overline{CE}$ LOW to Data Valid                |      | 10   | ns   |
| t <sub>DOE</sub>                  | $\overline{OE}$ LOW to Data Valid                |      | 5    | ns   |
| t <sub>LZOE</sub>                 | $\overline{OE}$ LOW to Low-Z                     | 0    |      | ns   |
| t <sub>HZOE</sub>                 | $\overline{OE}$ HIGH to High-Z <sup>[7, 8]</sup> |      | 5    | ns   |
| t <sub>LZCE</sub>                 | $\overline{CE}$ LOW to Low-Z <sup>[8]</sup>      | 3    |      | ns   |
| t <sub>HZCE</sub>                 | $\overline{CE}$ HIGH to High-Z <sup>[7, 8]</sup> |      | 5    | ns   |
| t <sub>PU</sub>                   | $\overline{CE}$ LOW to Power-up                  | 0    |      | ns   |
| t <sub>PD</sub>                   | CE HIGH to Power-down                            |      | 10   | ns   |
| Write Cycle <sup>[9, 10]</sup>    |                                                  |      |      |      |
| t <sub>WC</sub>                   | Write Cycle Time                                 | 10   |      | ns   |
| t <sub>SCE</sub>                  | CE LOW to Write End                              | 7    |      | ns   |
| t <sub>AW</sub>                   | Address Set-up to Write End                      | 7    |      | ns   |
| t <sub>HA</sub>                   | Address Hold from Write End                      | 0    |      | ns   |
| t <sub>SA</sub>                   | Address Set-up to Write Start                    | 0    |      | ns   |
| t <sub>PWE</sub>                  | $\overline{WE}$ Pulse Width                      | 7    |      | ns   |
| t <sub>SD</sub>                   | Data Set-up to Write End                         | 5    |      | ns   |
| t <sub>HD</sub>                   | Data Hold from Write End                         | 0    |      | ns   |
| t <sub>LZWE</sub>                 | $\overline{WE}$ HIGH to Low-Z <sup>[8]</sup>     | 3    |      | ns   |
| t <sub>HZWE</sub>                 | $\overline{WE}$ LOW to High-Z <sup>[7, 8]</sup>  |      | 5    | ns   |

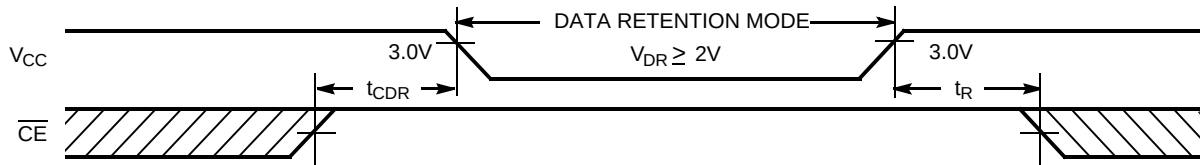
### Notes:

- AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
- $t_{\text{POWER}}$  gives the minimum amount of time that the power supply should be at stable, typical  $V_{CC}$  values until the first memory access can be performed.
- $t_{HZOE}$ ,  $t_{LZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal Write time of the memory is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Data Retention Characteristics Over the Operating Range

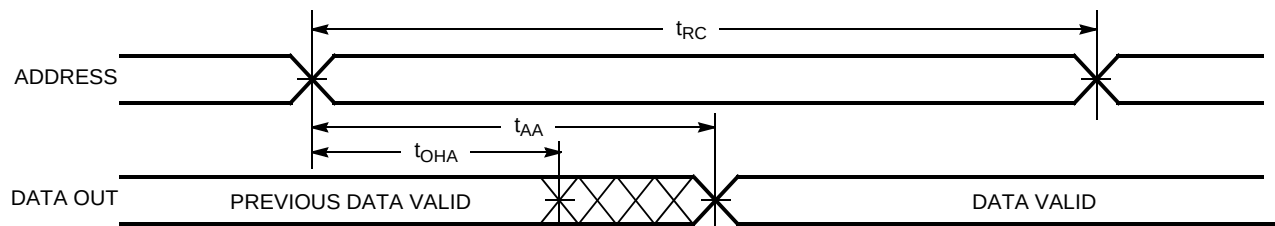
| Parameter       | Description                          | Conditions <sup>[11]</sup>                                                                                      | Min.     | Max. | Unit |
|-----------------|--------------------------------------|-----------------------------------------------------------------------------------------------------------------|----------|------|------|
| $V_{DR}$        | $V_{CC}$ for Data Retention          |                                                                                                                 | 2.0      |      | V    |
| $I_{CCDR}$      | Data Retention Current               | $V_{CC} = V_{DR} = 2.0V$ ,<br>$CE \geq V_{CC} - 0.3V$ ,<br>$V_{IN} \geq V_{CC} - 0.3V$ or<br>$V_{IN} \leq 0.3V$ |          | 20   | mA   |
| $t_{CDR}^{[3]}$ | Chip Deselect to Data Retention Time |                                                                                                                 | 0        |      | ns   |
| $t_R^{[12]}$    | Operation Recovery Time              |                                                                                                                 | $t_{RC}$ |      | ns   |

## Data Retention Waveform

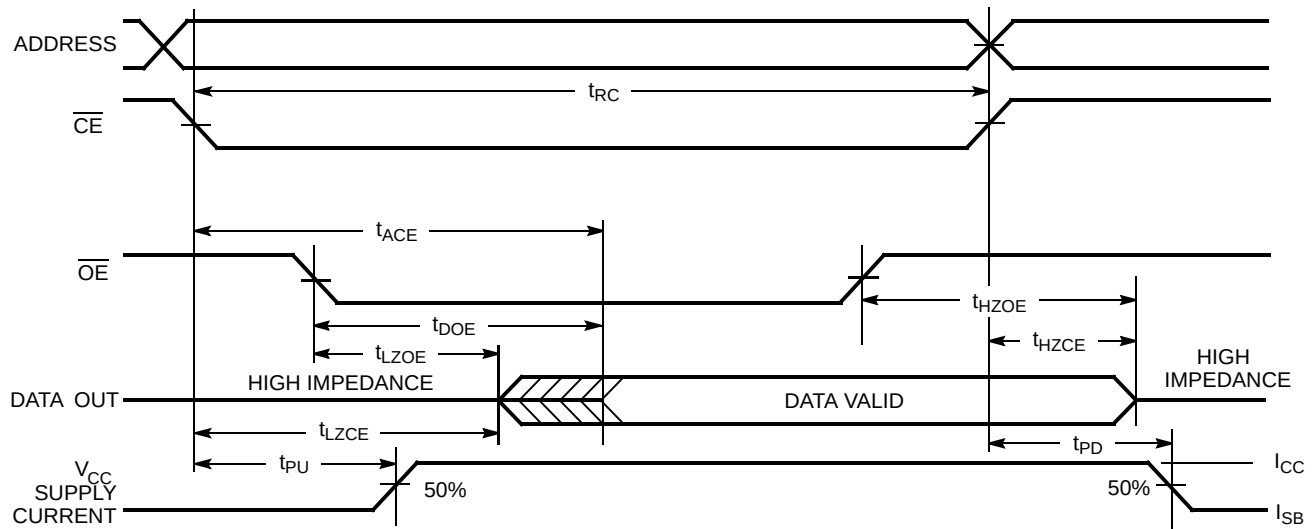


## Switching Waveforms

### Read Cycle No. 1<sup>[13, 14]</sup>



### Read Cycle No. 2 ( $\overline{OE}$ Controlled)<sup>[14, 15]</sup>

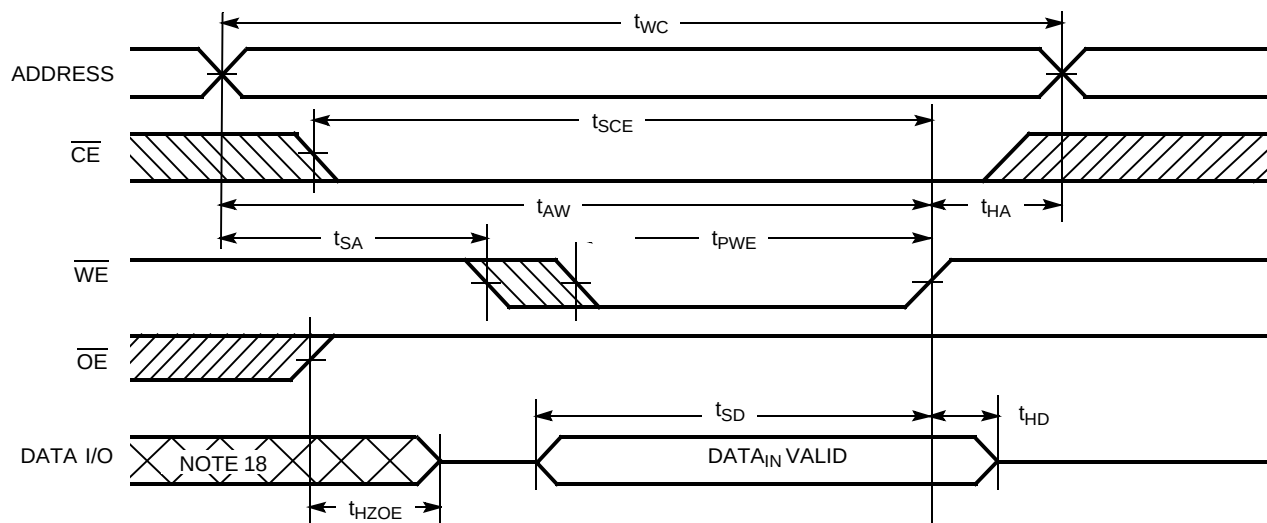


#### Notes:

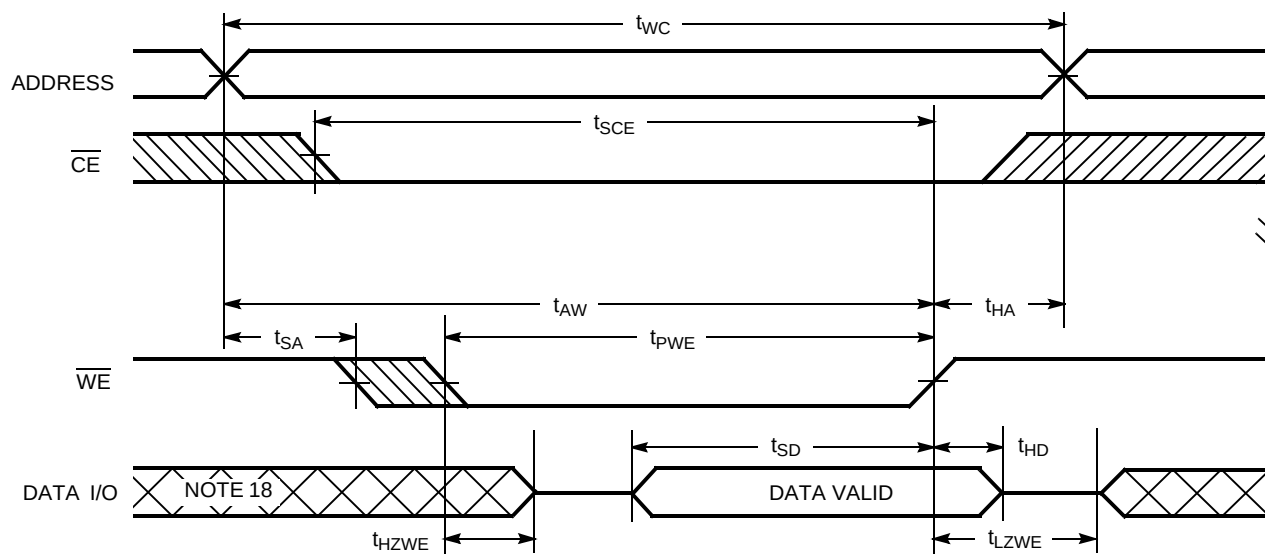
- No inputs may exceed  $V_{CC} + 0.3V$ .
- Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 50 \mu s$  or stable at  $V_{CC(min.)} \geq 50 \mu s$ .
- Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
- $\overline{WE}$  is HIGH for Read cycle.
- Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

## Switching Waveforms(continued)

### Write Cycle No. 1( $\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)<sup>[16, 17]</sup>



### Write Cycle No. 2 ( $\overline{WE}$ Controlled, $\overline{OE}$ LOW)<sup>[17]</sup>



#### Notes:

16. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .

17. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.

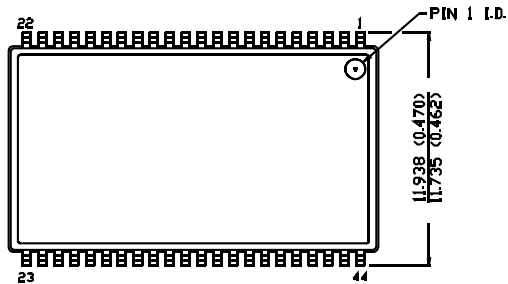
18. During this period the I/Os are in the output state and input signals should not be applied.



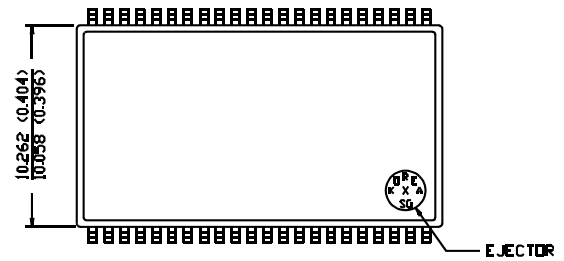
**Package Diagrams (continued)**

**44-pin TSOP II (51-85087)**

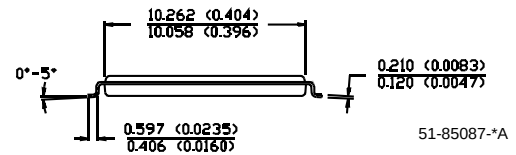
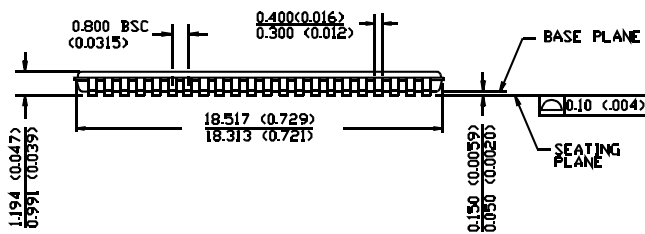
DIMENSION IN MM (INCH)  
MAX  
MIN



**TOP VIEW**



**BOTTOM VIEW**



51-85087-A

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**Document History Page**

| Document Title: CY7C1059DV33 8-Mbit (1M x 8) Static RAM<br>Document Number: 001-00061 |         |            |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|---------------------------------------------------------------------------------------|---------|------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| REV.                                                                                  | ECN NO. | Issue Date | Orig. of Change | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| **                                                                                    | 342195  | See ECN    | PCI             | New Data Sheet                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| *A                                                                                    | 380574  | See ECN    | SYT             | Redefined $I_{CC}$ values for Com'l and Ind'l temperature ranges<br>$I_{CC}$ (Com'l): Changed from 110, 90 and 80 mA to 110, 100 and 95 mA for 8, 10 and 12 ns speed bins respectively<br>$I_{CC}$ (Ind'l): Changed from 110, 90 and 80 mA to 120, 110 and 105 mA for 8, 10 and 12 ns speed bins respectively<br>Changed the Capacitance values from 8 pF to 10 pF on Page # 3                                                                                                                                                                                                                                  |
| *B                                                                                    | 485796  | See ECN    | NXR             | Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court"<br>Removed -8 and -12 Speed bins from product offering,<br>Removed Commercial Operating Range option,<br>Modified Maximum Ratings for DC input voltage from -0.5V to -0.3V and $V_{CC} + 0.5V$ to $V_{CC} + 0.3V$<br>Updated footnote #7 on High-Z parameter measurement<br>Added footnote #11<br>Changed the Description of $I_{IX}$ from Input Load Current to Input Leakage Current.<br>Updated the Ordering Information table and Replaced Package Name column with Package Diagram. |