



High-Speed SERDES Briefcase Board

Evaluation Board for ORSO/ORT82G5, ispGDX2™ and ispPAC® Devices

User's Guide

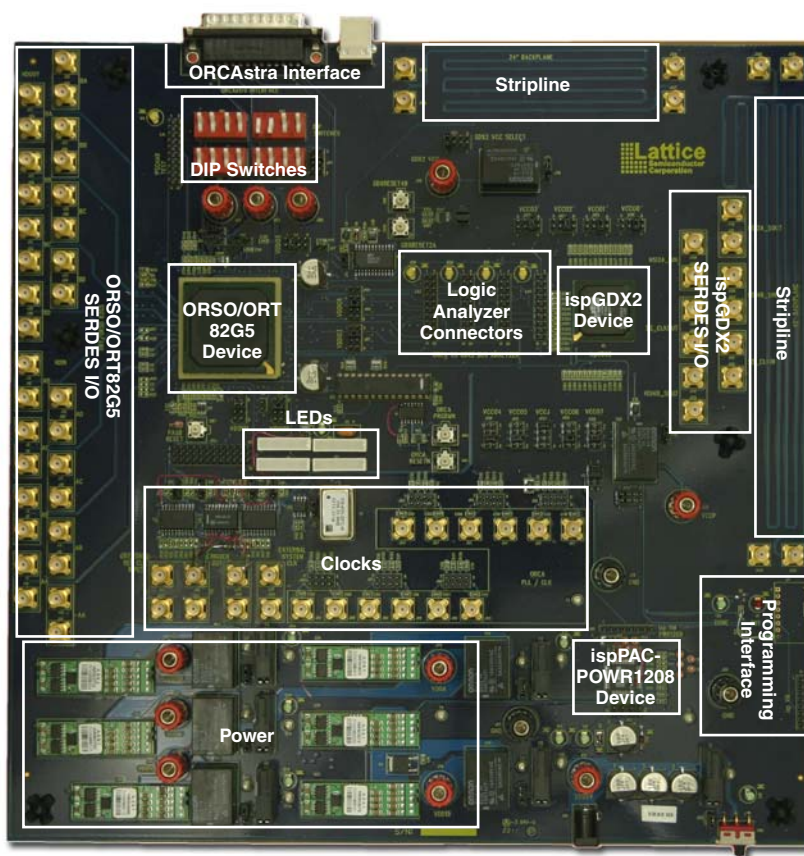
Introduction

This user's guide describes the Lattice High-Speed SERDES Briefcase Board, a stand-alone evaluation board for the Lattice ORSO82G5 and ORT82G5 Field Programmable System Chips (FPSCs). The board also contains a socket and test connections for evaluation of the ispGDX2-256 programmable digital crosspoint switch, and an integrated power supply controller by the ispPAC-POWR1208. The board includes the following features:

- Stand-alone power source
- ispVM[®] programming support
- On-board reference clock sources (external clock source can be used)
- Discrete high speed interface SMA test points and clock connections
- Simulated matched backplane controlled impedance test runs

The contents of this user's guide include top level functional descriptions of the various portions of the evaluation board, descriptions of all connectors, diodes and switches and a complete set of schematics for version 1.1 of the board. Figure 1 shows the functional partitioning of the board.

Figure 1. Lattice High-Speed SERDS Briefcase Board



The evaluation board is also supported by the ORCAstra[™] graphical user interface (GUI). ORCAstra enables the user to configure bits on the control registers of the FPSC devices via a PC. For more information, refer to the *ORCAstra Users Manual* available on the Lattice web site at www.latticesemi.com. The Lattice web site also contains further information about the Lattice devices used on this board, including device data sheets and application notes.

Electrical, Mechanical and Environmental Specifications

The nominal board dimensions are 12 inches by 12 inches. The environmental specifications are as follows:

- Operating temperature: 0°C to 55°C
- Storage temperature: -40°C to 75°C
- Humidity: < 95% without condensation

Regulated power is available from on-board supplies operated from a wall-type 5V supply. Alternately, power may be supplied from an external source. 3.3V, 2.5V, 1.8V and 1.5V power buses are supplied.

The devices may be driven by the on-board 156MHz oscillator or, to allow operation at different speeds, from independent differential clock sources. When the clock is sourced from the internal oscillator, a trigger output for test equipment is available.

In addition to the high-speed SMA connectors, five logic analyzer connections are supplied for Agilent P/N 01650-63203 isolation adapters or equivalents. Standard headers and DIP switches are provided for setup of the evaluation environment, and LEDs are provided to indicate current board and device status. Connections are provided both to device pins with dedicated functions, and to general purpose I/Os from the FPGA portion of the FPSC.

Jacks, Connectors, Diodes and Switches

Bitstream Configuration Connectors

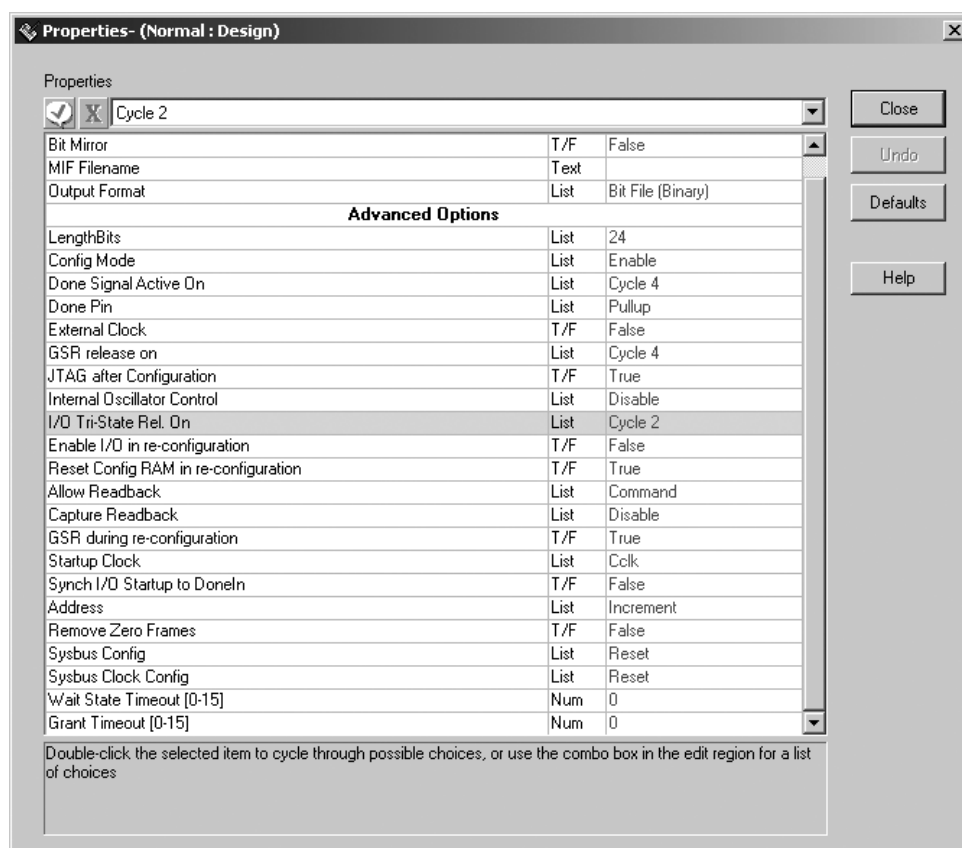
The following connectors are used for configuration and programming.

Table 1. Programming Connections

Jack Number	Size	Function
J1	8 pins (6 used)	ispVM Download - FPSCs and ispGDX2
J4	8 pins (6 used)	ORCA® Download (not populated)
J60	8 pins (6 used)	ispVM Download - ispPAC-POWR1208

Notes:

1. LEDs are used to indicate the status of FPSC and ispGDX2 downloads.
2. The preference selections shown in Figure 2 are recommended for generating ORCA bitstreams. Note particularly the selections of the "Cycle 2" and "Cycle 4" options.
3. Programming jacks J1 and J60 are intended for use with the Lattice ispDOWNLOAD® Cable, type pDS4102-DL2.

Figure 2. ispVM Preference Settings for ORCA Bitstreams

Note: With some operating system configurations, the ispVM software will generate failure and error messages related to the USB when programming is first attempted. If this occurs, do the following:

1. Click on **Options** in the ispVM toolbar and select **Cable and I/O Port Setup**
2. Verify that "Cable Type" is "USB" and "Port Setting" is "Ezusb-0"
3. Unplug the USB cable from the system running ispVM
4. Replug the USB cable into the system running ispVM
5. Click **OK**

The device should now program successfully.

ORCAstra Interface Connectors

The following connectors are used to interface with the ORCAstra GUI.

Table 2. ORCAstra GUI Connections

Jack Number	Size	Function
P1	24 pin	Parallel Port (LPT) ORCAstra Interface
J53	4 pin	Universal Serial Bus (USB) ORCAstra Interface

Note: The USB serial interface device and supporting EPROM are not specifically highlighted on the board photograph in Figure 1.

Headers

Standard 0.100 headers are provided for interconnecting points on the board. This can be accomplished with 0.100 IDC connectors and ribbon cable for bus connections or 0.025 pin socket patch cords (such as Pomona Electronics #5948. See www.pomonaelectronics.com for more information).

The following standard headers are used on the evaluation board. Boards are provided with default connections (ORSO/ORT82G5 listed here. Refer to the schematics in Appendix A for other configuration options).

Table 3. General Purpose Headers

Jack Number	Related Schematic	Size	Function	Default Connection
J2	Figure 6	1x2	Tristates ORSO/ORT82G5 (located between J55 and J56)	None
J3	Figure 6	3x2	Sets up configuration path, U1, U2 or daisy chain (located under J128)	[1-2][3-4][5-6]
J37	Figure 8	1x2	ORSO/ORT82G5 PTEMP pin (located to the right of J69)	None
J39	Figure 9	2>1	On-Board Oscillator Power, +3.3 or GND (located below the LEDs and J54)	[1-2]
J41	Figure 9	2>1	External/On-board Clock Select (located below the LEDs and J54)	[1-2] ¹
J42	Figure 9	2>1	On-Board Clock __2 (located below the LEDs and J54)	[2-3] ¹
J45	Figure 10	2>1	ORSO/ORT82G5 REF_CLKA Select for Quad A (located below the LEDs and J54)	[1-2]
J50	Figure 10	2>1	ORSO/ORT82G5 REF_CLKB Select, for Quad B (located below the LEDs and J54)	[2-3]
J51	Figure 11	4x2	VDD select for DIP Switches	[1-2]
J52	Figure 12	1x2	Enables ORCAstra Parallel Port Interface (located above J68)	None
J141	Figure 12	3x12	Configures ORCAstra Parallel Port or USB Interface	[2,3][5-6][8-9] [11-12][14-15] [17-18][20-21][23-24]
J61	Figure 14	1x2	ispPAC Input (jumper shorts to ground)	None
J62	Figure 14	1x2	ispPAC Input (jumper shorts to ground)	None
J63	Figure 14	1x2	ispPAC Input (jumper shorts to ground)	None
J64	Figure 14	1x2	ispPAC Input (jumper shorts to ground)	None
J140	Figure 14	1x2	5V connection to evaluation board – remove jumper to configure ispPAC (located to the right of J58 and left of SW8)	[1-2]
J65	Figure 15	4x2	VDDIO0 Select, ORSO/ORT82G5 I/O	[1-8]
J66	Figure 15	4x2	VDDIO1 Select, ORSO/ORT82G5 I/O	[1-8]
J67	Figure 15	4x2	VDDIO2 Select, ORSO/ORT82G5 I/O	[1-5]
J68	Figure 15	4x2	VDDIO6 Select, ORSO/ORT82G5 I/O	[1-5]
J69	Figure 15	4x2	VDDIO5 Select, ORSO/ORT82G5 I/O	[1-5]
J70	Figure 16	2>1	External/Internal Power Select, 3.3V	[1-2]
J71	Figure 16	2>1	External/Internal Power Select, analog 1.5V	[1-2]
J74	Figure 16	2>1	External/Internal Power Select, 2.5V	[1-2]
J76	Figure 16	2>1	External/Internal Power Select, 1.5V	[1-2]
J77	Figure 16	2>1	External/Internal Power Select, 1.8V	[1-2]
J81	Figure 17	4x2	Input Configure, ORCA Primary Clock 0 Test	[1-2] [7-8]
J84	Figure 17	4x2	Input Configure, ORCA Primary Clock 1 Test	[1-2] [7-8]
J86	Figure 17	4x2	Input Configure, ORCA PLL Clock 0 Test	[1-2] [7-8]
J90	Figure 17	4x2	Input Configure, ORCA PLL Clock 1 Test	[1-2] [7-8]
J92	Figure 17	4x2	Input Configure, ORCA PLL Clock 6 Test	[1-2] [7-8]

Table 3. General Purpose Headers (Continued)

Jack Number	Related Schematic	Size	Function	Default Connection
J96	Figure 17	4x2	Input Configure, ORCA PLL Clock 7 Test	[1-2] [7-8]
J98	Figure 18	2>1	External/Internal Power Select, VDD_OB (located left of J69)	[1-2]
J100	Figure 18	2>1	External/Internal Power Select, VDD_IB (located left of J69)	[1-2]
J102	Figure 18	2>1	External/Internal Power Select, VDDA (located left of J69)	[1-2]
JP1	Figure 20	2x2	Pushbutton/FPGA GDXRESET Select	None
J116	Figure 21	1x2	ispGDX2 Manual Tristate (jumper tristates ispGDX2), located above J124	None
J117	Figure 22	4x2	VCC Select, ispGDX2	[2-4]
J118	Figure 22	2>1	External/Internal Power Select, ispGDX2 VCC	[1-2]
J120	Figure 23	4x2	VCCO0 Select, ispGDX2	[1-5]
J121	Figure 23	4x2	VCCO5 Select, ispGDX2	[1-5]
J122	Figure 23	4x2	VCCO6 Select, ispGDX2	[1-5]
J123	Figure 23	4x2	VCCO1 Select, ispGDX2	[1-5]
J124	Figure 23	4x2	VCCO2 Select, ispGDX2	[1-5]
J125	Figure 23	4x2	VCCO3 Select, ispGDX2	[1-5]
J126	Figure 23	4x2	VCCO4 Select, ispGDX2	[1-5]
J127	Figure 23	4x2	VCCJ Select (JTAG voltage)	[1-5]
J128	Figure 23	4x2	VCCO7 Select, ispGDX2	[1-5]
J129	Figure 23	2>1	External/Internal Power Select, ispGDX2 VCCP (located above J131)	[1-2] ²
J130	Figure 23	4x2	VCCA Select, ispGDX2 (located to the left of J131)	[2-6] ²

1. Errata for Jacks J41 and J42 is as follows: To select an external clock source via SMA connections, remove default jumpers on J41 and J42 and add a connection between J42[1] to J41[2]. This can be accomplished using a 0.25 pin socket 6" patch cord (Pomona P/N 5948 or similar).

2. Lattice recommends VCCP0 and VCCP1 be connected to the appropriate voltage supply, even when the PLL and sysHSI circuits will not be used.

J54 and TP1

This evaluation board has wiring for a 12x3 header (J54) to support SERDES testing, and a test point (TP1) for observing the ATMOUT_A signal (see Figure 13). Both are located next to the PASB RESET pushbutton. In general, this header location is not populated.

TP2 through TP9

The evaluation board has wiring for 8 test points (TP2 through TP9) for observing the operation of the ispPAC PWR1208 Power Sequencer (see Figure 14).

SMA Connectors

The following SMA connectors are used on the evaluation board (see Figure 1).

Table 4. ORSO/ORT82G5 Quad A Serial I/O (see Figure 7)

Jack Number	I/O Name
J14	HDIN_AA
J13	HDIP_AA
J16	HDIN_AB
J15	HDIP_AB
J18	HDIN_AC
J17	HDIP_AC
J20	HDIN_AD
J 19	HDIP_AD
J10	HDOUTN_AA
J7	HDOUTP_AA
J6	HDOUTN_AB
J5	HDOUTP_AB
J9	HDOUTN_AC
J8	HDOUTP_AC
J12	HDOUTN_AD
J11	HDOUTP_AC

Table 5. ORSO/ORT82G5 Quad B Serial I/O (see Figure 8)

Jack Number	I/O Name
HDIN_BA	J22
HDIP_BA	J23
HDIN_BB	J25
HDIP_BB	J26
HDIN_BC	J29
HDIP_BC	J30
HDIN_BD	J33
HDIP_BD	J34
HDOUTN_BA	J21
HDOUTP_BA	J24
HDOUTN_BB	J27
HDOUTP_BB	J28
HDOUTN_BB	J31
HDOUTP_BB	J32
HDOUTN_BB	J35
HDOUTP_BB	J36

Note: Outputs for channels AA and BA have on-board bias_T's to the VDD_OB supply. Channels AB and AC are AC coupled with 100ohm pull-up resistors to VDD_OB. The remaining output channels and all input channels are DC coupled.

Table 6. Clock SMA Connectors

Jack Number	Related Schematic	Function
J38	Figure 9	External System Clock Input_P
J40	Figure 9	External System Clock Input_N
J43	Figure 10	ORSO/ORT External Ref Clk A_P Input
J44	Figure 10	ORSO/ORT External Ref Clk A_N Input
J46	Figure 10	ORSO/ORT External Ref Clk B_P Input
J47	Figure 10	ORSO/ORT External Ref Clk B_N Input
J48	Figure 10	Trigger (Clock) Out_P
J49	Figure 10	Trigger (Clock) Out_N

Notes:

1. On-board header connections determine the clock source for the FPSC. The FPSC reference clocks may be provided by the onboard oscillator, a common external clock source, or multiple external clocks.
2. If an external clock source is used, it must be a differential clock.
3. The trigger outputs are DC coupled in the default configuration. They can be converted to AC coupling by replacing resistors R204 and R215 with 0.01 μ F surface mount capacitors.

Table 7. OECA/PLL Clock Test SMA Connectors (see Figure 17)

Jack Number	Function
J80	True Input, PLL Clock 0 Test
J82	Complementary Input, PLL Clock 0 Test
J83	True Input, Primary Clock 0 Test
J85	True Input, PLL Clock 1 Test
J87	Complementary Input, Primary Clock 0 Test
J88	Complementary Input, PLL Clock 1 Test
J89	True Input, Primary Clock 1 Test
J91	True Input, PLL Clock 6 Test
J93	Complementary Input, Primary Clock 1 Test
J94	Complementary Input, PLL Clock 6 Test
J95	True Input, PLL Clock 7 Test
J97	Complementary Input, PLL Clock 7 Test

Table 8. ispGDX2 SMA Connectors (see Figure 20)

Jack Number	Function
J104	Negative Clock Out, SS_CLKOUT0N
J105	Positive Clock Out, SS_CLKOUT0P
J106	Positive Clock In, SS_CLKIN1P
J107	Negative Clock Out, SS_CLKIN1N
J108	Positive Serial Data In, HSI2A_SINP
J109	Negative Serial Data In, HSI2A_SINN
J110	Positive Serial Data Out, HSI2A_SOUTP
J111	Negative Serial Data Out, HSI2A_SOUTN
J112	Positive Serial Data Out, HSI4B_SOUTP
J113	Negative Serial Data Out, HSI4B_SOUTN
J114	Positive Serial Data In, HSI4B_SINP
J115	Negative Serial Data In, HSI4B_SINN

Table 9. Backplane Test SMA Connectors (see Figure 24 and areas marked “stripline” in Figure 1)

Jack Number		Connection
J132	J133	40" backplane, 8 mil coplanar stripline
J134	J135	40" backplane, 8 mil coplanar stripline
J136	J137	24" backplane, 8 mil coplanar stripline
J138	J139	24" backplane, 8 mil coplanar stripline

All connections have 100Ω balanced impedance between pairs.

Logic Analyzer Connections

The Logic Analyzer connections are connectors for Agilent P/N 01650-63203 isolation adapters or an equivalent. As shown in Figure 1, each connector has an associated LED that lights when a proper connection is made. See Figure 1 and Figure 8.

This 10x2 connector is used for ORSO/ORT82G5 Quad B SERDES testing (PSCHAR).

Table 10. Logic Analyzer Connectors

Pin	Signal	Signal	Pin
1	Ground via D3	N/C	2
3	PSCHAR_XCK	ATM_OUT_B	4
5	PSCHAR_CV	PSCHAR_BYTSYNC	6
7	PSCHAR_CKIO1	PSCHAR_WDSYNC	8
9	PSCHAR_CKIO0	PSCHAR_LDIO9	10
11	PSCHAR_LDIO8	PSCHAR_LDIO7	12
13	PSCHAR_LDIO6	PSCHAR_LDIO5	14
15	PSCHAR_LDIO4	PSCHAR_LDIO3	16
17	PSCHAR_LDIO2	PSCHAR_LDIO1	18
19	PSCHAR_LDIO0	Ground	20

LA2 and LA3

These 10x2 ORCA to ispGDX2 bus analyzer connectors are used for clock, control, status and reset signals for the ispGDX2 device (see Figure 20). Each pin is also connected to a general purpose I/O pin in the ORSO/ORT82G5 FPGA logic.

Table 11. LA2 Signals

Pin	Signal
1	Ground via D19
2	N/C
3	N/C
4	CAL
5	GOE0
6	CSLOCK4
7	SYDT2A
8	SYDT4BF
9	CDRLOCK2A
10	LOSS4B
11	RECCLK2A
12	EXLOSS4B
13	EXLOSS2A
14	RECCLK4B
15	LOSS2A
16	CDRLOCK4B
17	SYDT2AF
18	STDT4B
19	CSLOCK2
20	Ground

Table 12. LA3 Signals

Pin	Signal
1	Ground via D20
2	N/C
3	N/C
4	N/C
5	N/C
6	N/C
7	GOE1
8	CDRRST2A
9	GOE2
10	CDRRST4B
11	GOE3
12	FIFO_EMPTY
13	SEL0
14	FIFO_FULL4B
15	SEL1
16	GCLKCE3
17	SEL2
18	GCLKCE2
19	SEL3
20	Ground

LA4 and LA5

These 10x2 ORCA to ispGDX2 bus analyzer connectors are used for TX data, RX data and general purpose I/O signals for the ispGDX2 device (see Figure 21). Each pin is also connected to a general purpose I/O pin in the ORSO/ORT82G5 FPGA logic.

Table 13. LA4 Signals

Pin	Signal
1	Ground via D21
2	N/C
3	N/C
4	GP_5
5	GP_4
6	GP_3
7	GP_2
8	GP_1
9	GP_0
10	TXD9
11	TXD8
12	TXD7
13	TXD6
14	TXD5
15	TXD4
16	TXD3
17	TXD2
18	TXD1
19	TXD0
20	Ground

Table 14. LA5 Signals

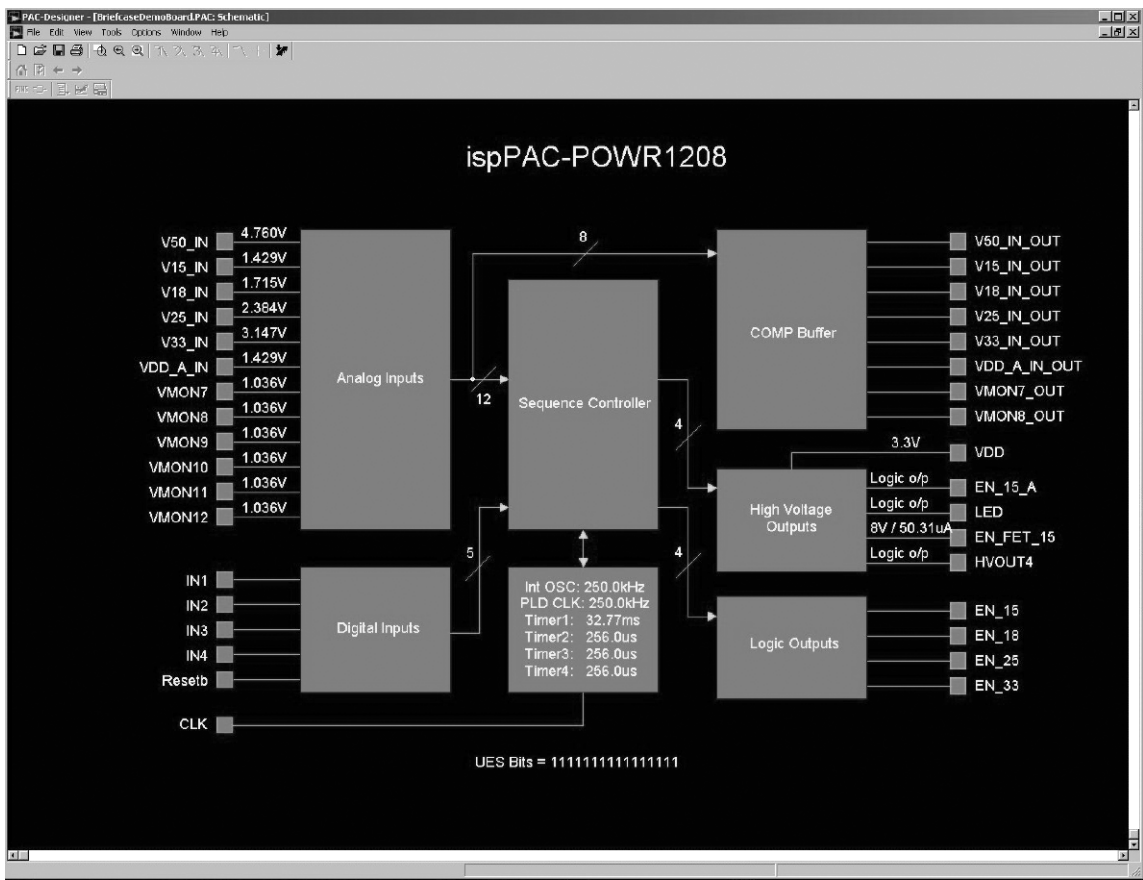
Pin	Signal
1	Ground via D22
2	N/C
3	N/C
4	GP_11
5	GP_10
6	GP_9
7	GP_8
8	GP_7
9	GP_6
10	RXD9
11	RXD8
12	RXD7
13	RXD6
14	RXD5
15	RXD4
16	RXD3
17	RXD2
18	RXD1
19	RXD0
20	Ground

Power Supply Notes

The evaluation board includes five on-board regulated power supplies that operate from an external 5V supply. Headers are used to allow a choice of voltage for the on-board voltage buses, and to control the relays for either on-chip or off-chip power for each voltage level. Each supply is fused and has an associated LED indicating that the voltage is present (see Figure 1). The fuses are Littelfuse Alarm Indicating Fuses, 0481 Series (F1 is Digikey P/N F725 and the other four fuses are Digikey P/N F723).

The evaluation board also includes an ispPAC-POWR1208 power control device. Programming files for this device can be developed using Lattice PAC-Designer® software. The top level PAC-Designer screen used for the default programming of the ispPAC-POWR1208 device is shown in Figure 3.

Figure 3. PAC-Designer Configuration Interface for ispPAC-POWR1208



As provided, the device is programmed to provide power in the sequence shown in Figure 4.

Figure 4. Default Power Sequence for ispPAC-POWR1208 Used on the Evaluation Board

PAC-Designer - [BriefcaseDemoBoard.PAC: Sequence Controller]			
File Edit View Tools Options Window Help			
PIHS			
Step	Sequencer Instruction	Int...	Comment
Step 0	Wait for V50_IN	no	Wait for 5V to rise
Step 1	EN_15 = 1,	no	Turn on 1.5V bricks
Step 2	Wait for 32.77ms using timer 1	no	wait a while
Step 3	EN_FET_15 = 1,	no	ENABLE 1.5V Pass FET
Step 4	Wait for V15_IN	no	Wait for 1.5V rail to rise
Step 5	EN_33 = 1,	no	Turn on 3.3V bricks
Step 6	Wait for V33_IN	no	Wait for 3.3V rail to rise
Step 7	EN_15_A = 1,	no	Turn on VDDA (1.5V 'A')
Step 8	Wait for VDD_A_IN	no	Wait for VDD_A to rise (1.5V)
Step 9	EN_18 = 1, EN_25 = 1,	no	Turn on 1.8V & 2.5V rails
Step 10	Wait for V50_IN AND V15_IN AND V18_IN AND V25_IN AND V33_I...	no	Wait for everything up
Step 11	LED = 0,	no	Light LED (assert LOW)
	<end-of-program>	no	

Turret Connectors

The following turret connectors are available for monitoring the power buses on the evaluation board.

Table 15. Turret Connectors

Turret Number	Related Schematic	Connected to – Power Bus
T1	Figure 14	5V
T2	Figure 14	Ground
T3	Figure 14	Ground
T4	Figure 14	Ground
T5	Figure 16	3.3V, relay side of fuse
T6	Figure 16	Analog 1.5V, relay side of fuse
T7	Figure 16	3.3V, LED side of fuse
T8	Figure 16	Analog 1.5V, LED side of fuse
T9	Figure 16	2.5V, relay side of fuse
T10	Figure 16	2.5V, LED side of fuse
T11	Figure 16	1.5V, relay side of fuse
T12	Figure 16	1.8V, relay side of fuse
T13	Figure 16	1.5V, LED side of fuse
T14	Figure 16	1.8V, LED side of fuse

Banana Jack Connectors

The following banana jack connectors are available for supplying power to the evaluation board from an external source.

Table 16. Banana Jack Connectors

Jack Number	Related Schematic	Color	Function
J55	Figure 14	Red	5V external supply (VDD5)
J56	Figure 14	Black	Ground (GND)
J57	Figure 14	Black	Ground (GND)
J59	Figure 14	Black	Ground (GND)
J72	Figure 16	Red	Analog 1.5V external supply (VDDA)
J73	Figure 16	Red	3.3V external supply (VDD33)
J75	Figure 16	Red	2.5V external supply (VDD25)
J78	Figure 16	Red	1.5V external supply (VDD15)
J79	Figure 16	Red	1.8V external supply (VDD18)
J99	Figure 18	Red	VDD_OB external supply (located beneath DIP switches)
J101	Figure 18	Red	VDD_IB external supply (located beneath DIP switches)
J103	Figure 18	Red	VDDA external supply (located beneath DIP switches)
J119	Figure 22	Red	ispGDX2 VCC external supply
J131	Figure 23	Red	ispGDX2 VCCP (analog) external supply

J58

A 2.5 mm male power jack (J58) is provided for connection to the 5V wall power adapter (Condor SA-054A00-1-206IP or equivalent). See Figure 14.

Diodes

The following diodes are used on the evaluation board.

Table 17. Diodes

Diode Number	Related Schematic	Type	Function/Indication
D1	Figure 6	Red LED	ORSO/ORT82G5 Configuration INIT
D2	Figure 6	Green LED	ORSO/ORT82G5 Configuration DONE
D3	Figure 8	Yellow LED	ORSO/ORT82G5 SERDES Test LA Pod OK
D4	Figure 11 ¹	Quad Red LED	Outputs from ORSO/ORT82G5 FPGA Logic
D5	Figure 11 ¹	Quad Red LED	Outputs from ORSO/ORT82G5 FPGA Logic
D6	Figure 11 ¹	Quad Red LED	Outputs from ORSO/ORT82G5 FPGA Logic
D7	Figure 11 ¹	Quad Red LED	Outputs from ORSO/ORT82G5 FPGA Logic
D8	Figure 12	1N4148	Voltage dropping diode, parallel port input
D9	Figure 12	Green LED	USB Interface Active
D10	Figure 14	Green LED	5V (VDD5) present on evaluation board
D11	Figure 14	1N4148	ispPAC VDD bias network
D12	Figure 14	Green LED	ispPAC Configuration Done
D13	Figure 14	1N5226	ispPAC VDD bias network, Zener
D14	Figure 16	Green LED	3.3V (VDD33) present on evaluation board
D23	Figure 16	Green LED	Analog 1.5V (VDDA) present on evaluation board
D16	Figure 16	Green LED	2.5V (VDD25) present on evaluation board
D24	Figure 16	Green LED	1.5V (VDD15) present on evaluation board
D25	Figure 16	Green LED	1.8V (VDD18) present on evaluation board
D19	Figure 20	Yellow LED	ORCA to ispGDX2 Test LA Pod 2 OK
D20	Figure 20	Yellow LED	ORCA to ispGDX2 Test LA Pod 3 OK
D21	Figure 21	Yellow LED	ORCA to ispGDX2 Test LA Pod 4 OK
D22	Figure 21	Yellow LED	ORCA to ispGDX2 Test LA Pod 5 OK

1. Also see LED and DIP table (Table 19).

Switches

The following switches are used on the evaluation board.

Table 18. Switches

Switch Number	Related Schematic	Type	Function
SW1	Figure 6	Momentary PB	ORSO/ORT82G5 RESETN
SW2	Figure 6	Momentary PB	ORSO/ORT82G5 PRGMN
SW3[A:D]	Figure 11 ^{1,2}	Quad DIP	Switch Inputs to ORSO/ORT82G5 FPGA Logic
SW4[A:D]	Figure 11 ^{1,2}	Quad DIP	Switch Inputs to ORSO/ORT82G5 FPGA Logic
SW5[A:D]	Figure 11 ^{1,2}	Quad DIP	Switch Inputs to ORSO/ORT82G5 FPGA Logic
SW6[A:D]	Figure 11 ^{1,2}	Quad DIP	Switch Inputs to ORSO/ORT82G5 FPGA Logic
SW7	Figure 13	Momentary PB	ORSO/ORT82G5 PASB_RESETN (SERDES Test)
SW8	Figure 14	SPDT	Disconnects +5 volts from evaluation board
SW11	Figure 14	Momentary PB	PWR1208 RESET
SW9	Figure 20	Momentary PB	GDX-RESET4B
SW10	Figure 20	Momentary PB	GDX-RESET2A

1. Also see the LED and DIP table (Table 19).

2. For the Quad DIP switches, "off" is toward the banana jacks.

LED and DIP Connections to ORSO/ORT82G5

Table 19. LED and DIP Connectors

FPGA Logic Options from ORSO/ORT82G5		FPGA Logic Inputs to ORSO/ORT82G5	
FPSC Pin	LED	DIP Switch	FPSC Pin
C21	D4 - Pin 2	SW3A	AL18
E18	D4 - Pin 4	SW3B	AN21
E19	D4 - Pin 6	SW3C	AM21
D19	D4 - Pin 8	SW3D	AN22
D20	D5 - Pin 2	SW4A	AK18
B24	D5 - Pin 4	SW4B	AN23
C23	D5 - Pin 6	SW4C	AP26
C22	D5 - Pin 8	SW4D	AK19
C24	D6 - Pin 2	SW5A	AL21
A27	D6 - Pin 4	SW5B	AM23
B27	D6 - Pin 6	SW5C	AN25
B25	D6 - Pin 8	SW5D	AL22
B26	D7 - Pin 2	SW6A	AL23
A28	D7 - Pin 4	SW6B	AN27
D22	D7 - Pin 6	SW6C	AM25
E22	D7 - Pin 8	SW6D	AP29

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
ORT82G5, ispGDX256, and ispPAC Power Manager 1208 Briefcase Board	ORT82G5-G2-PAC-EV	
ORSO82G5 Evaluation Board	ORSO82G5-G2-PAC-EV	

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

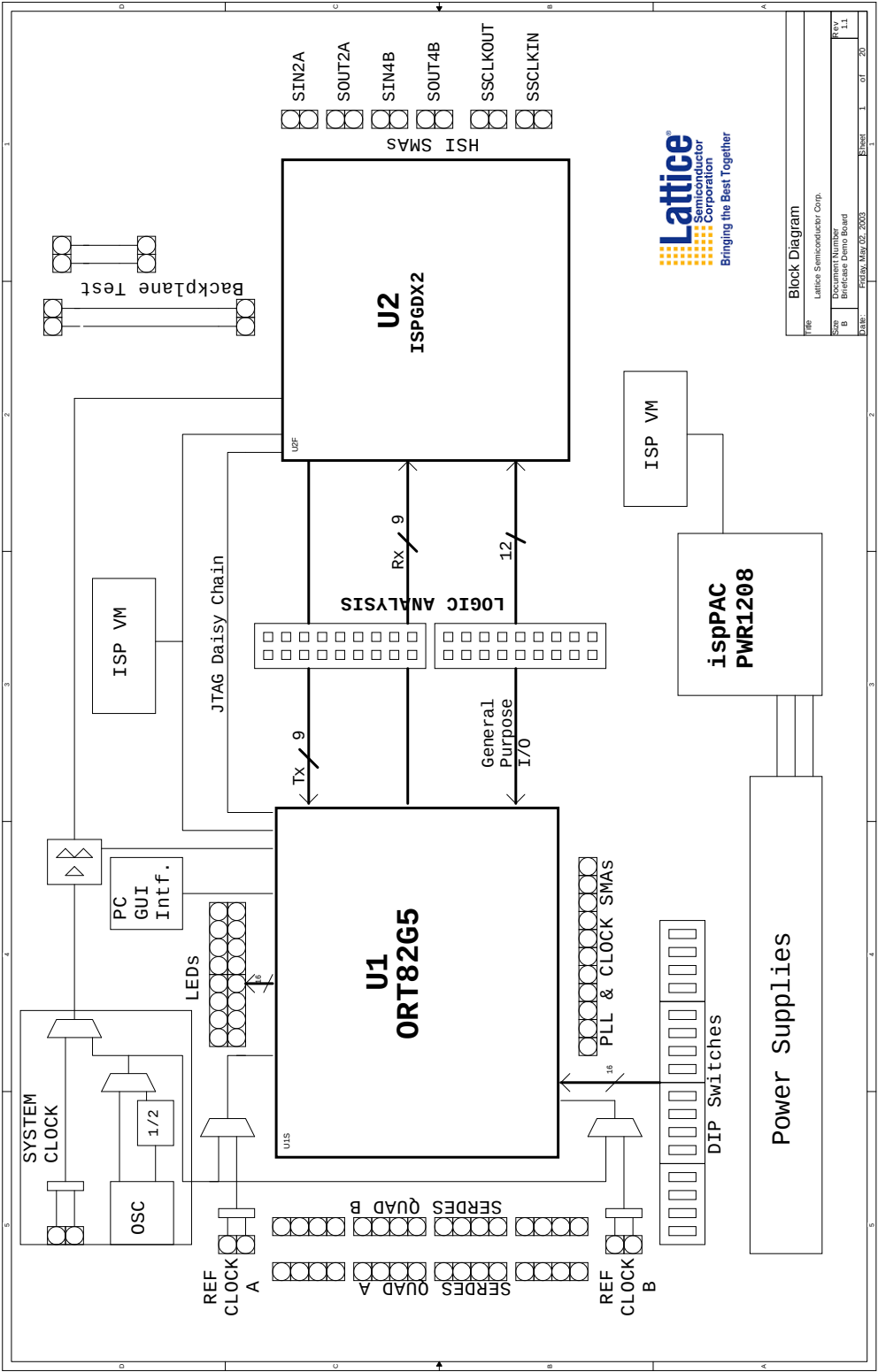
Date	Version	Change Summary
March 2003	01.0	Initial release.
March 2007	01.1	Added Ordering Information section.

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Appendix A. Schematics

The current schematics for the High-Speed SERDES Briefcase Board are given in this appendix.

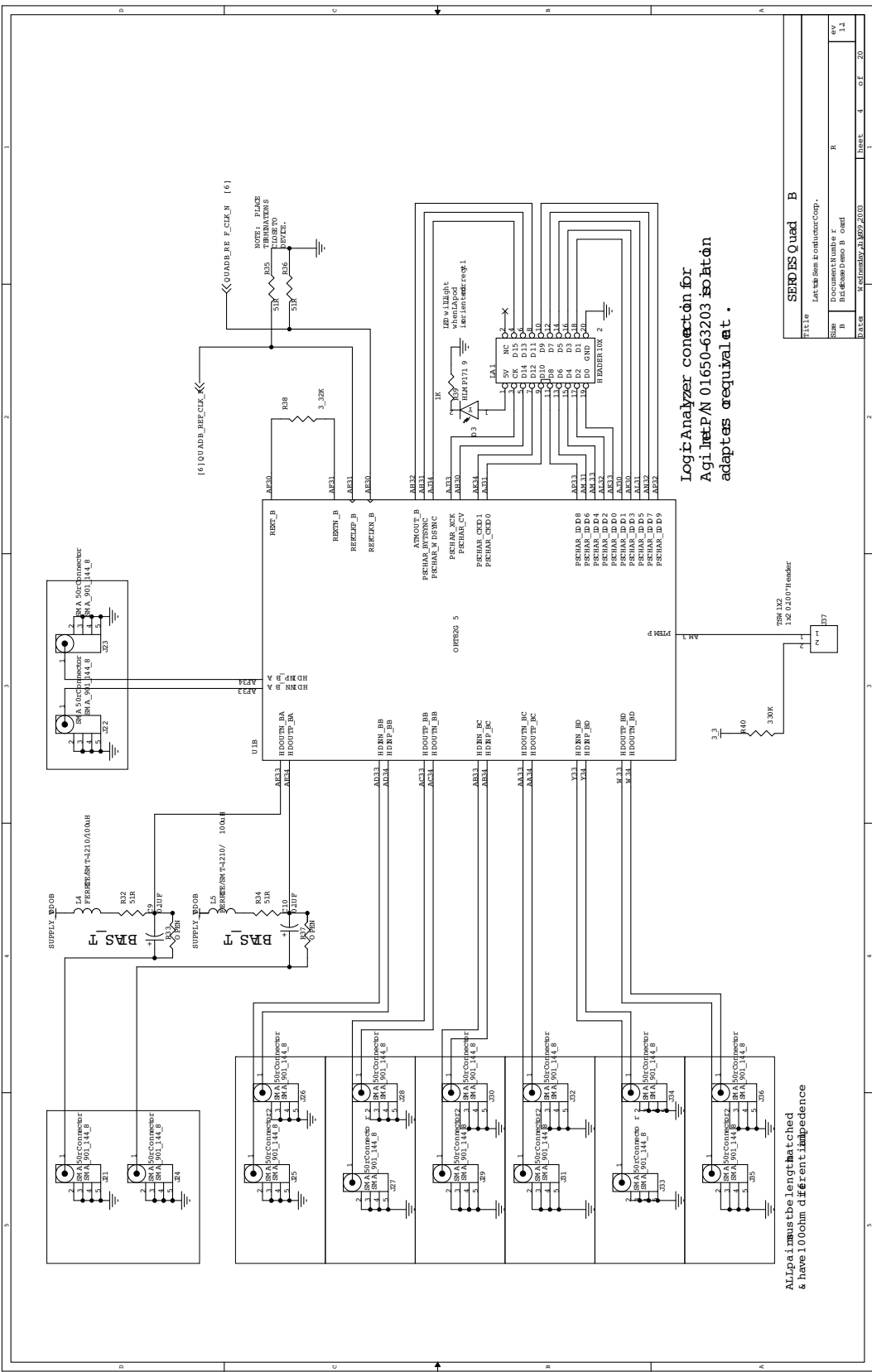
Figure 5. Lattice High-Speed SERDES Briefcase Board Schematic



Configuration			
Title	Lattice Semiconductor Corp.		
Size	Document Number		
B	Briefcase Demo Board		
Rev	1.1		
Date	Friday, May 02, 2003		
Sheet	2	01	20

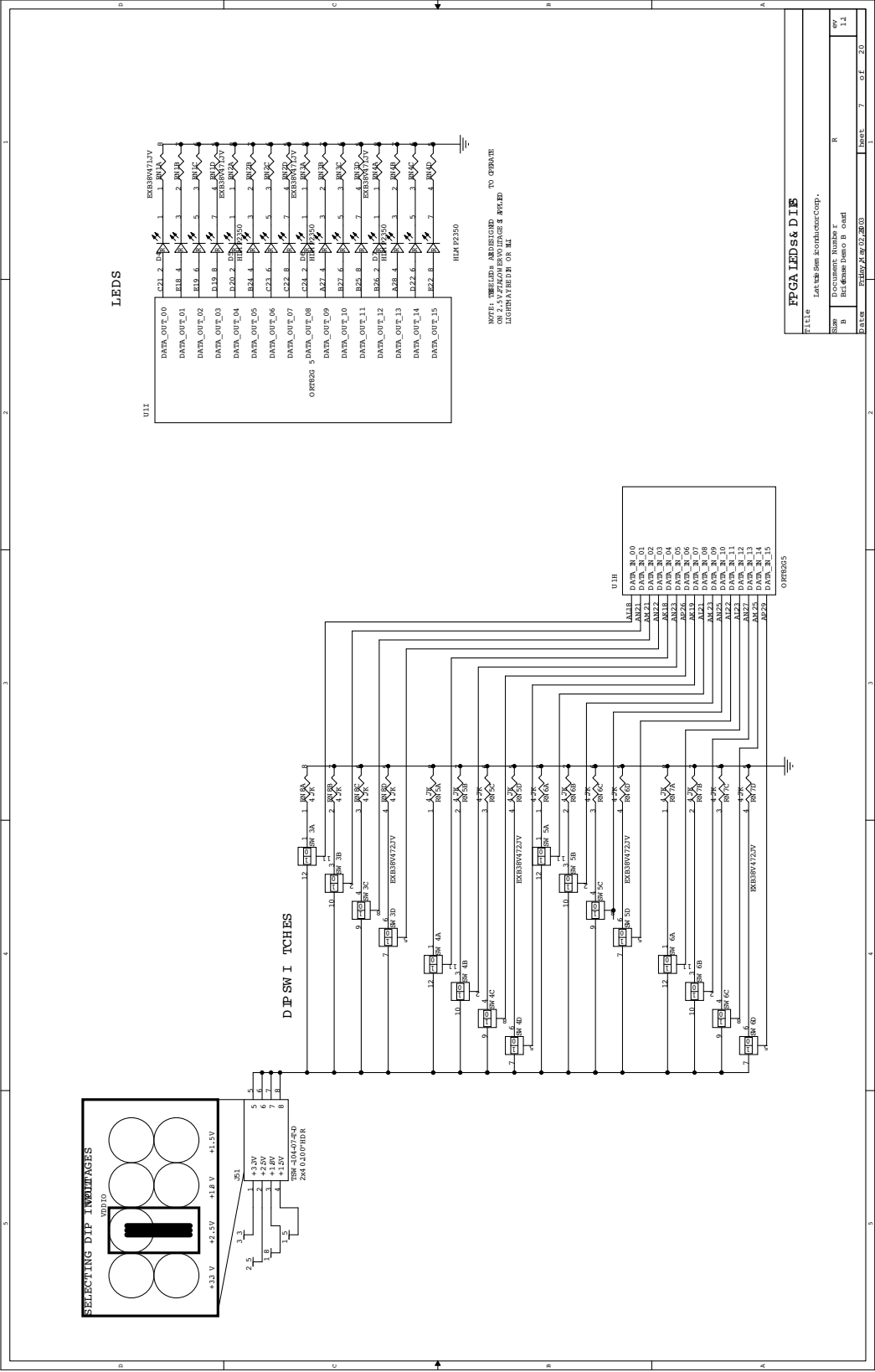
[illegible]

Figure 8. Lattice High-Speed SERDES Briefcase Board Schematic



[illegible]

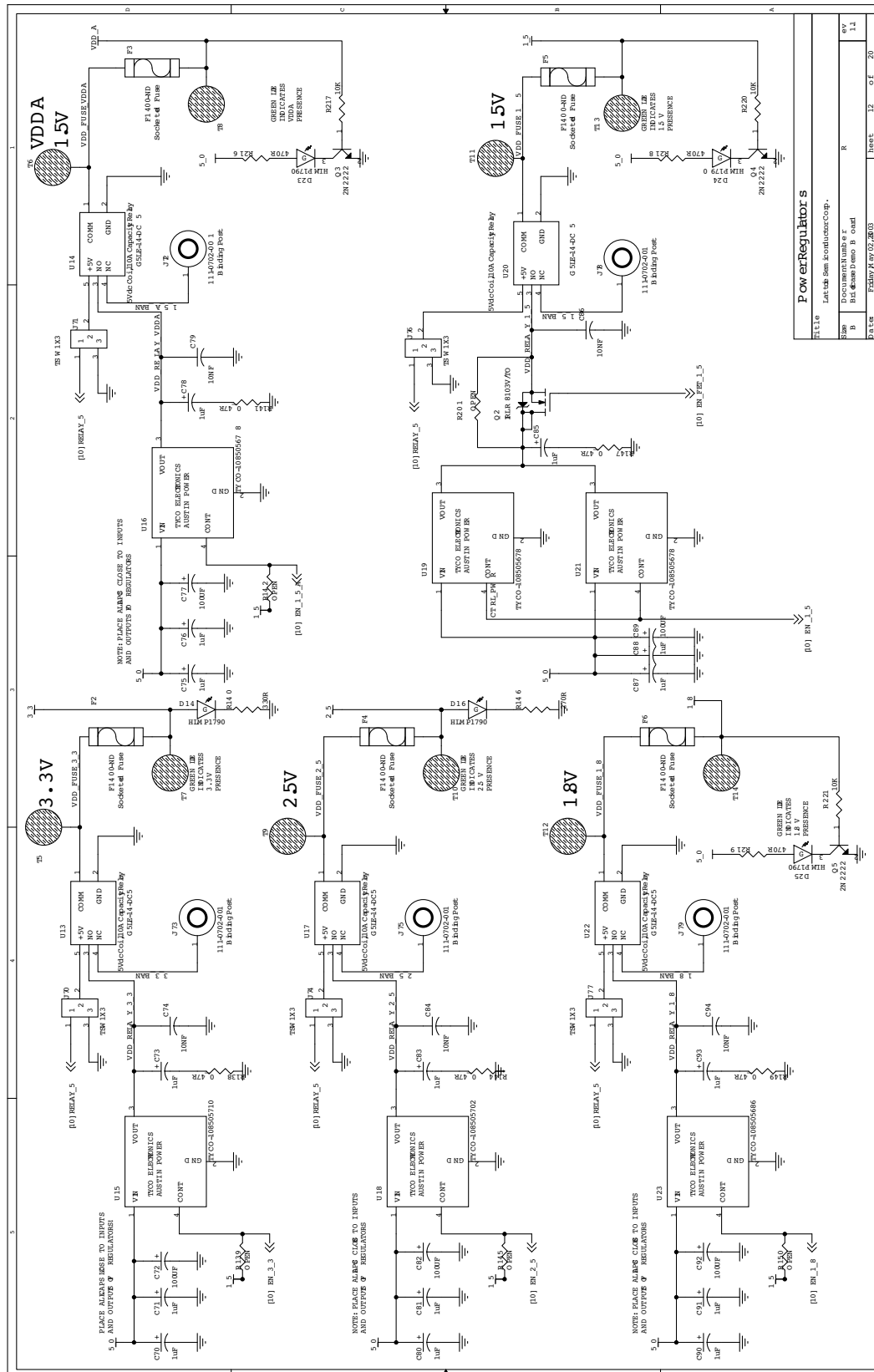
Figure 11. Lattice High-Speed SERDES Briefcase Board Schematic



The schematic diagram illustrates the SERDES Test circuit. It features a MAX6817N comparator (U11) configured as a differential line driver/receiver. The circuit is powered by a 3.3V supply (VCC_1) with a 10nF capacitor (C3) and a 3.3k resistor (R1) to ground. The input is connected to a 3.3V supply through a 3.3k resistor (R1). The output is connected to a 3.3V supply through a 3.3k resistor (R1). The circuit also includes a 3.3V supply (VCC_2) and a 3.3V supply (VCC_3). The circuit is labeled 'SERDES Test' and 'MAX6817N'.

[illegible]

Figure 16. Lattice High-Speed SERDES Briefcase Board Schematic



[illegible]

Figure 18. Lattice High-Speed SERDES Briefcase Board Schematic

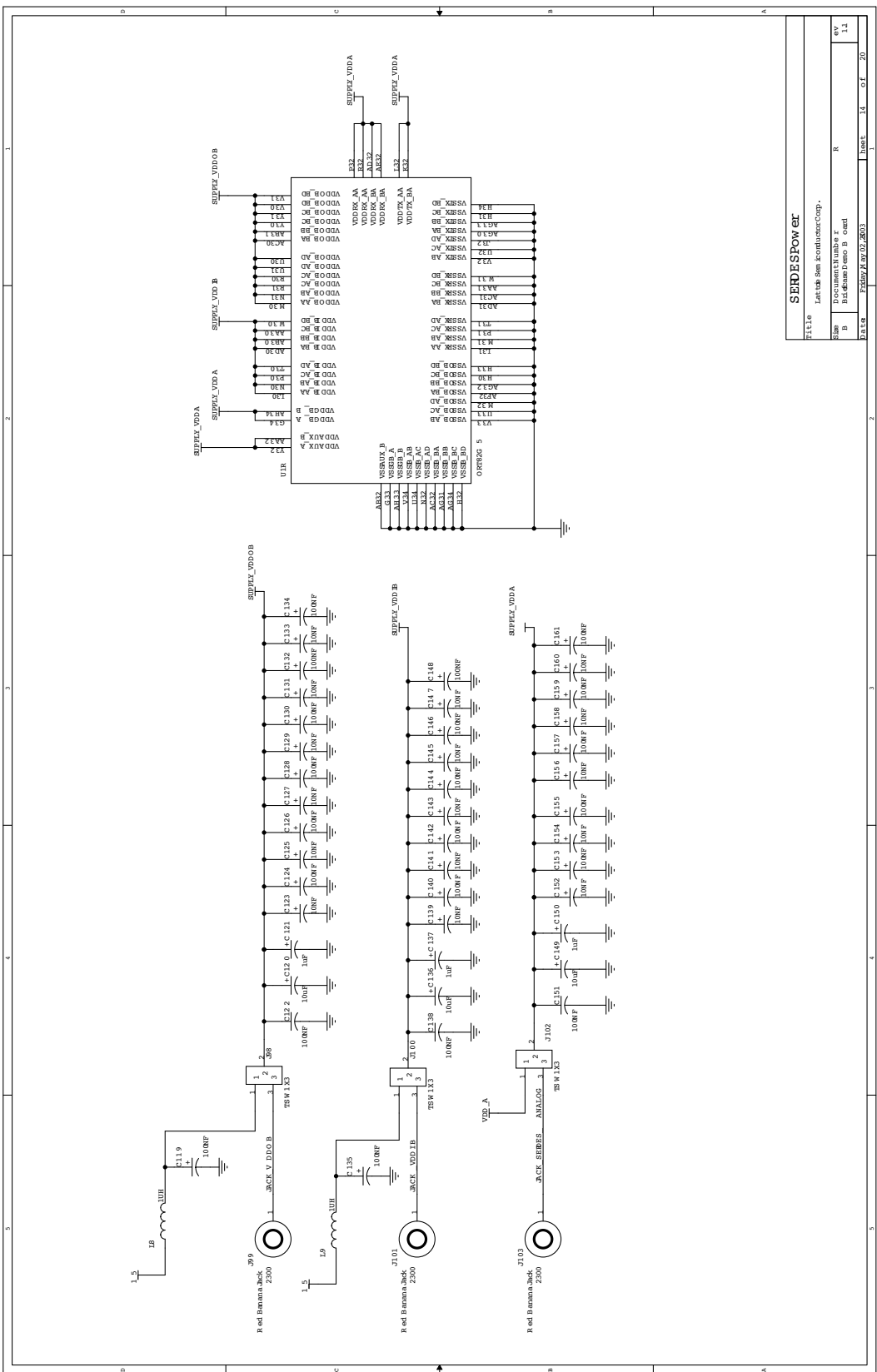
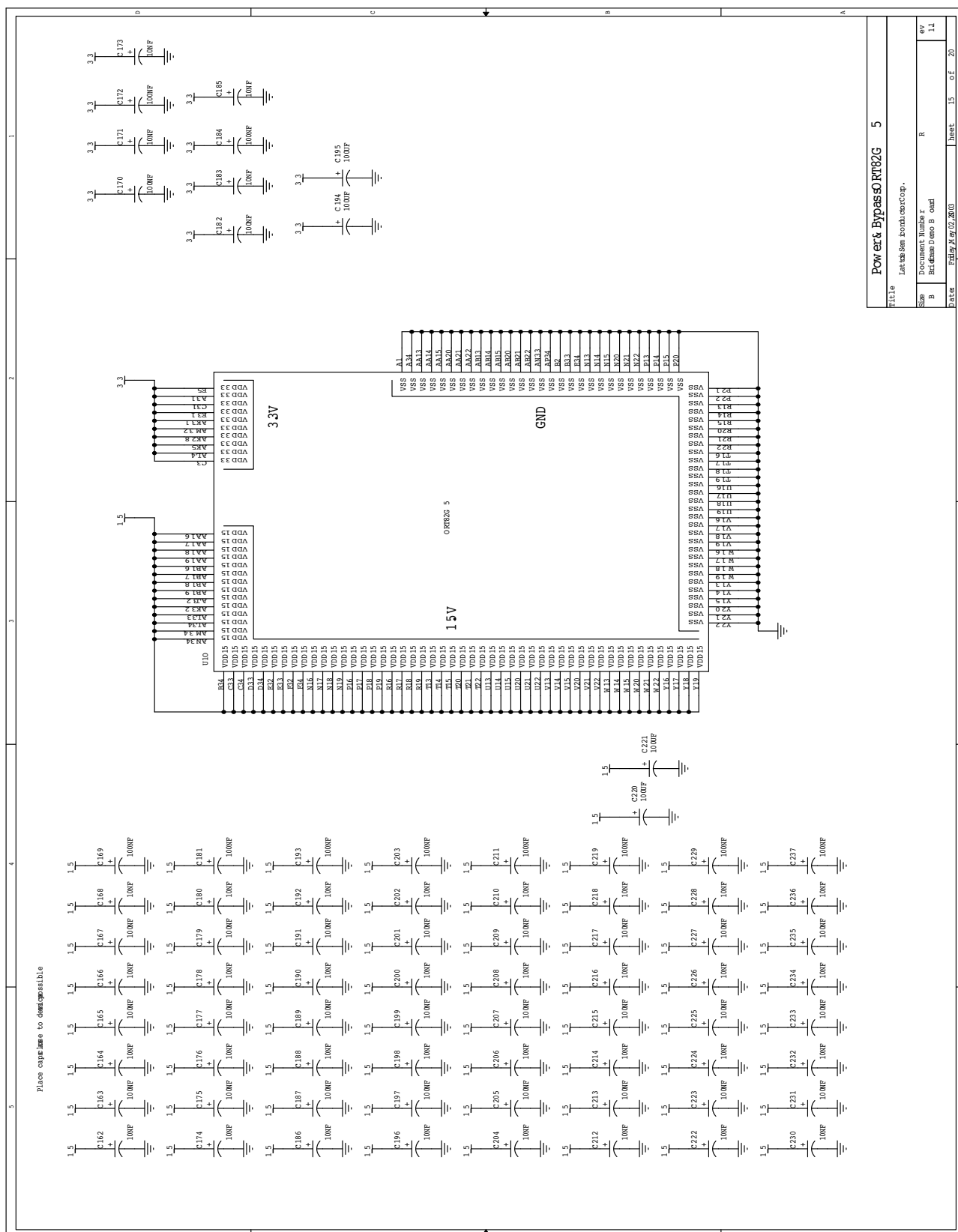


Figure 19. Lattice High-Speed SERDES Briefcase Board Schematic



Logix Analyzer connections for Agilent P/N 01650-63203 to be adapted as required

LED #111 Light
When Lit
LED #111 Light
When Lit
LED #111 Light
When Lit

ALL pairs must be lengthed to 100 Ohm differential impedance

ALL Traces must be 50 Ohm impedance

U2B

U2C

U2D

U2E

U2F

U2G

U2H

U2I

U2J

U2K

U2L

U2M

U2N

U2O

U2P

U2Q

U2R

U2S

U2T

U2U

U2V

U2W

U2X

U2Y

U2Z

U2AA

U2AB

U2AC

U2AD

U2AE

U2AF

U2AG

U2AH

U2AI

U2AJ

U2AK

U2AL

U2AM

U2AN

U2AO

U2AP

U2AQ

U2AR

U2AS

U2AT

U2AU

U2AV

U2AW

U2AX

U2AY

U2AZ

U2BA

U2BB

U2BC

U2BD

U2BE

U2BF

U2BG

U2BH

U2BI

U2BJ

U2BK

U2BL

U2BM

U2BN

U2BO

U2BP

U2BQ

U2BR

U2BS

U2BT

U2BU

U2BV

U2BW

U2BX

U2BY

U2BZ

U2CA

U2CB

U2CC

U2CD

U2CE

U2CF

U2CG

U2CH

U2CI

U2CJ

U2CK

U2CL

U2CM

U2CN

U2CO

U2CP

U2CQ

U2CR

U2CS

U2CT

U2CU

U2CV

U2CW

U2CX

U2CY

U2CZ

U2DA

U2DB

U2DC

U2DD

U2DE

U2DF

U2DG

U2DH

U2DI

U2DJ

U2DK

U2DL

U2DM

U2DN

U2DO

U2DP

U2DQ

U2DR

U2DS

U2DT

U2DU

U2DV

U2DW

U2DX

U2DY

U2DZ

U2EA

U2EB

U2EC

U2ED

U2EE

U2EF

U2EG

U2EH

U2EI

U2EJ

U2EK

U2EL

U2EM

U2EN

U2EO

U2EP

U2EQ

U2ER

U2ES

U2ET

U2EU

U2EV

U2EW

U2EX

U2EY

U2EZ

U2FA

U2FB

U2FC

U2FD

U2FE

U2FF

U2FG

U2FH

U2FI

U2FJ

U2FK

U2FL

U2FM

U2FN

U2FO

U2FP

U2FQ

U2FR

U2FS

U2FT

U2FU

U2FV

U2FW

U2FX

U2FY

U2FZ

U2GA

U2GB

U2GC

U2GD

U2GE

U2GF

U2GG

U2GH

U2GI

U2GJ

U2GK

U2GL

U2GM

U2GN

U2GO

U2GP

U2GQ

U2GR

U2GS

U2GT

U2GU

U2GV

U2GW

U2GX

U2GY

U2GZ

U2HA

U2HB

U2HC

U2HD

U2HE

U2HF

U2HG

U2HH

U2HI

U2HJ

U2HK

U2HL

U2HM

U2HN

U2HO

U2HP

U2HQ

U2HR

U2HS

U2HT

U2HU

U2HV

U2HW

U2HX

U2HY

U2HZ

U2IA

U2IB

U2IC

U2ID

U2IE

U2IF

U2IG

U2IH

U2II

U2IJ

U2IK

U2IL

U2IM

U2IN

U2IO

U2IP

U2IQ

U2IR

U2IS

U2IT

U2IU

U2IV

U2IW

U2IX

U2IY

U2IZ

U2JA

U2JB

U2JC

U2JD

U2JE

U2JF

U2JG

U2JH

U2JI

U2JJ

U2JK

U2JL

U2JM

U2JN

U2JO

U2JP

U2JQ

U2JR

U2JS

U2JT

U2JU

U2JV

U2JW

U2JX

U2JY

U2JZ

U2KA

U2KB

U2KC

U2KD

U2KE

U2KF

U2KG

U2KH

U2KI

U2KJ

U2KK

U2KL

U2KM

U2KN

U2KO

U2KP

U2KQ

U2KR

U2KS

U2KT

U2KU

U2KV

U2KW

U2KX

U2KY

U2KZ

U2LA

U2LB

U2LC

U2LD

U2LE

U2LF

U2LG

U2LH

U2LI

U2LJ

U2LK

U2LL

U2LM

U2LN

U2LO

U2LP

U2LQ

U2LR

U2LS

U2LT

U2LU

U2LV

U2LW

U2LX

U2LY

U2LZ

U2MA

U2MB

U2MC

U2MD

U2ME

U2MF

U2MG

U2MH

U2MI

U2MJ

U2MK

U2ML

U2MM

U2MN

U2MO

U2MP

U2MQ

U2MR

U2MS

U2MT

U2MU

U2MV

U2MW

U2MX

U2MY

U2MZ

U2NA

U2NB

U2NC

U2ND

U2NE

U2NF

U2NG

U2NH

U2NI

U2NJ

U2NK

U2NL

U2NM

U2NN

U2NO

U2NP

U2NQ

U2NR

U2NS

U2NT

U2NU

U2NV

U2NW

U2NX

U2NY

U2NZ

U2OA

U2OB

U2OC

U2OD

U2OE

U2OF

U2OG

U2OH

U2OI

U2OJ

U2OK

U2OL

U2OM

U2ON

U2OO

U2OP

U2OQ

U2OR

U2OS

U2OT

U2OU

U2OV

U2OW

U2OX

U2OY

U2OZ

U2PA

U2PB

U2PC

U2PD

U2PE

U2PF

U2PG

U2PH

U2PI

U2PJ

U2PK

U2PL

U2PM

U2PN

U2PO

U2PP

U2PQ

U2PR

U2PS

U2PT

U2PU

U2PV

U2PW

U2PX

U2PY

U2PZ

U2QA

U2QB

U2QC

U2QD

U2QE

U2QF

U2QG

U2QH

U2QI

U2QJ

U2QK

U2QL

U2QM

U2QN

U2QO

U2QP

U2QQ

U2QR

U2QS

U2QT

U2QU

U2QV

U2QW

U2QX

U2QY

U2QZ

U2RA

U2RB

U2RC

U2RD

U2RE

U2RF

U2RG

U2RH

U2RI

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U2RO

U2RP

U2RQ

U2RR

U2RS

U2RT

U2RU

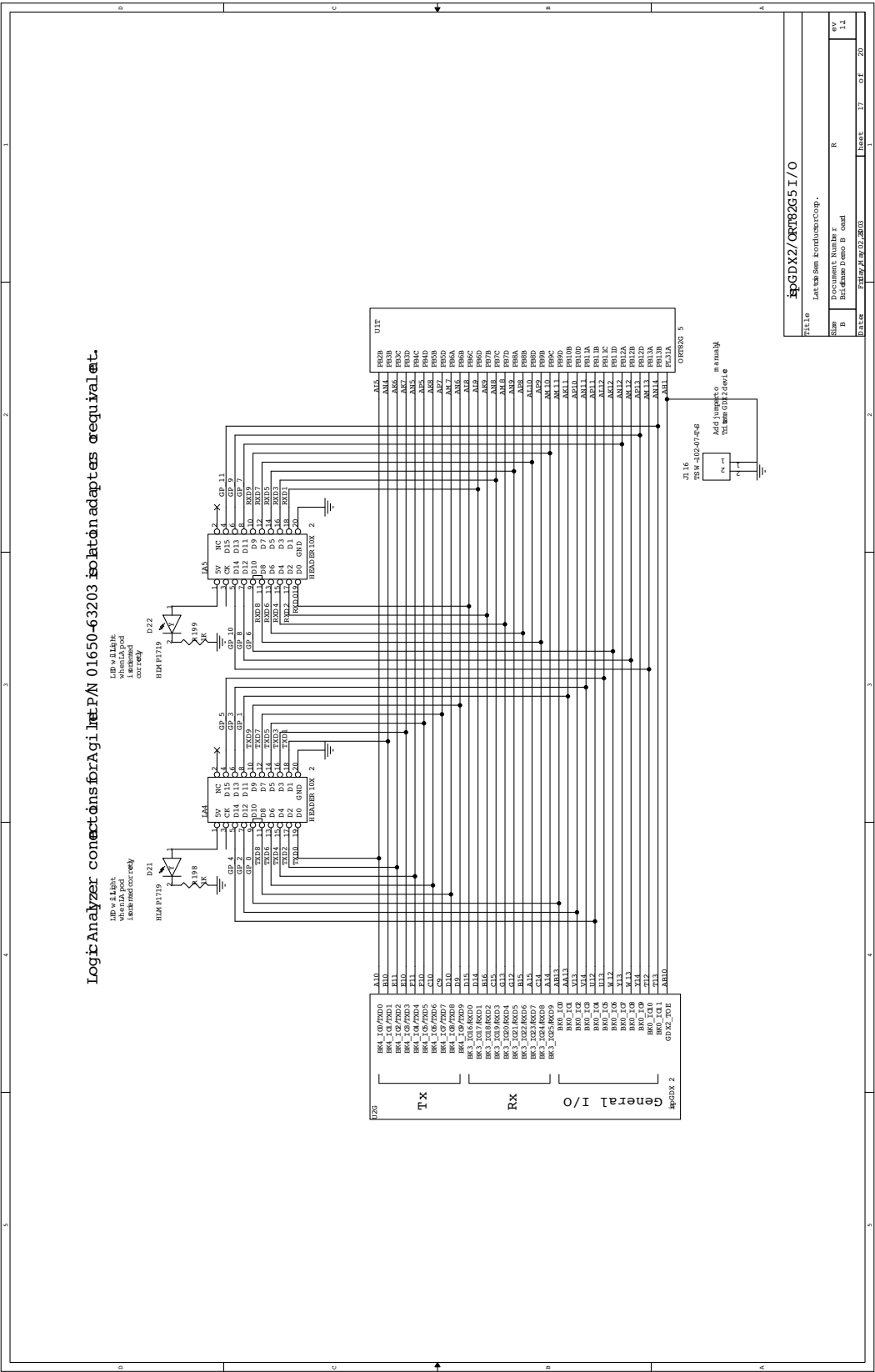
U2RV

U2RW

U2RX

U2RY

Figure 21. Lattice High-Speed SERDES Briefcase Board Schematic



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[illegible]

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