# Am27C100

## 1Megabit (131,072 x 8-Bit) ROM Compatible CMOS EPROM

Advanced Micro Devices

## DISTINCTIVE CHARACTERISTICS

- **EIAJ 32-pin DIP package**
- **Pinout compatible with 28-pin ROM**
- **Fast access time**
  - 100 ns
- **Low power consumption**
  - 100 µA typical standby current
- **High speed Flashrite™ programming**
- **Single + 5 V power supply**
- **± 10% power supply tolerance available**
- **Latch-up protected to 100 mA from –1 V to $V_{CC}$ + 1 V**

## GENERAL DESCRIPTION

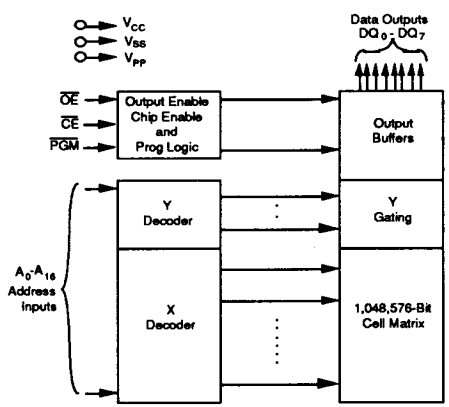
The Am27C100 is a 1 megabit ultraviolet erasable programmable read-only memory. The 32 pin EIAJ pinout is compatible with 28 pin megabit ROMs. The memory is organized as 128K words by 8 bits per word, operates from a single + 5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and plastic one time programmable (OTP) packages.

Any byte can be accessed in less than 120 ns, allowing operation with many high-performance microprocessors without any WAIT states. The Am27C100 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C100 supports AMD's Flashrite programming algorithm (0.1 ms pulses) resulting in typical programming times of less than 30 seconds.

## BLOCK DIAGRAM

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## PRODUCT SELECTOR GUIDE

| Family Part No. | Am27C100 | | | | |
|---|---|---|---|---|---|
| **Ordering Part Number:** $V_{CC}$ ± 5% | -105 | -125 | -155 | | -255 |
| $V_{CC}$ ± 10% | | -120 | -150 | -200 | |
| Max. Access Time (ns) | 100 | 120 | 150 | 200 | 250 |
| $\overline{CE}$ ($\overline{E}$) Access Time (ns) | 100 | 120 | 150 | 200 | 250 |
| $\overline{OE}$ ($\overline{G}$) Access Time (ns) | | 50 | 65 | 75 | 100 |

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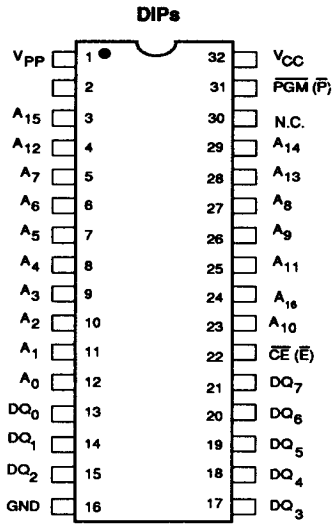
## CONNECTION DIAGRAM

### Top View

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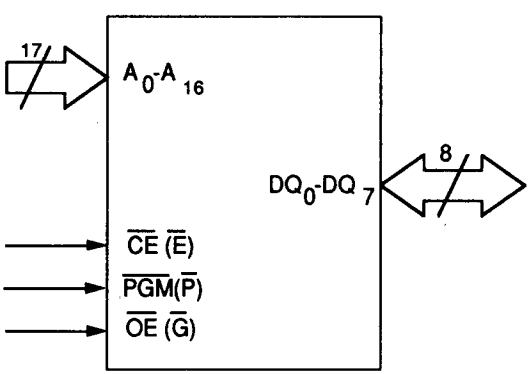
**Note:**
1. JEDEC nomenclature is in parentheses.

## LOGIC SYMBOL

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## PIN DESCRIPTION

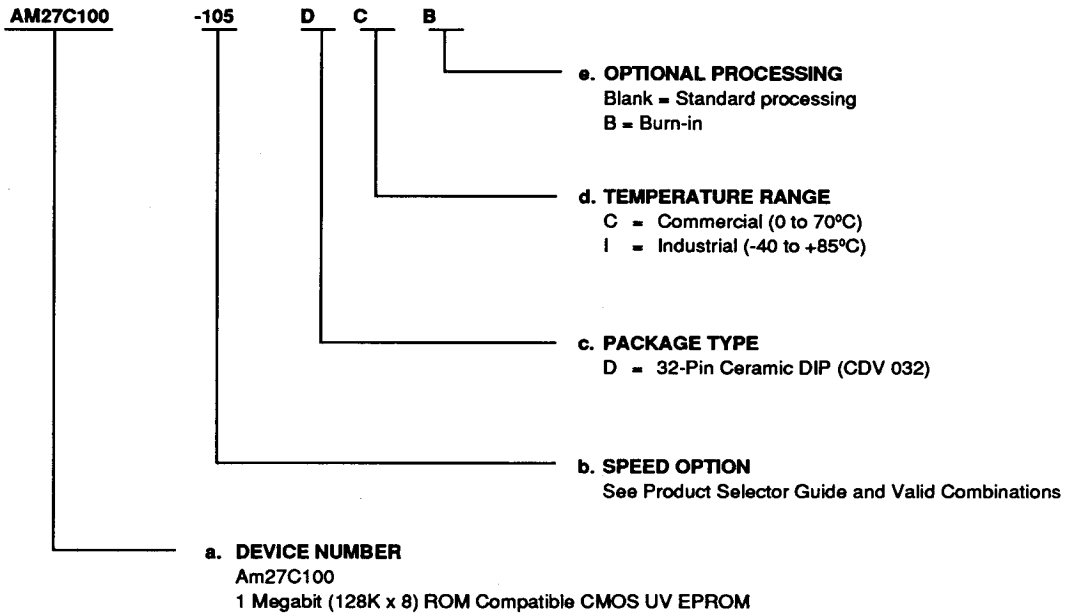
| | | |
|---|---|---|
| $A_0$–$A_{16}$ | = | Address Inputs |
| $\overline{CE}$ ($\overline{E}$) | = | Chip Enable Input |
| $DQ_0$–$DQ_7$ | = | Data Input/Outputs |
| $\overline{OE}$ ($\overline{G}$) | = | Output Enable Input |
| $\overline{PGM}$ ($\overline{P}$) | = | Program Enable Input |
| $V_{CC}$ | = | $V_{CC}$ Supply Voltage |
| $V_{PP}$ | = | Program Supply Voltage |
| GND | = | Ground |
| NC | = | No Internal Connect |

## ORDERING INFORMATION

### Standard Information

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

**a. Device Number**
**b. Speed Option**
**c. Package Type**
**d. Temperature Range**
**e. Optional Processing**




| Valid Combinations | |
|---|---|
| AM27C100-105 | DC, DCB |
| AM27C100-120 | DC, DCB, DI, DIB |
| AM27C100-125 | |
| AM27C100-150 | |
| AM27C100-155 | |
| AM27C100-200 | |
| AM27C100-255 | |

**Valid Combinations**

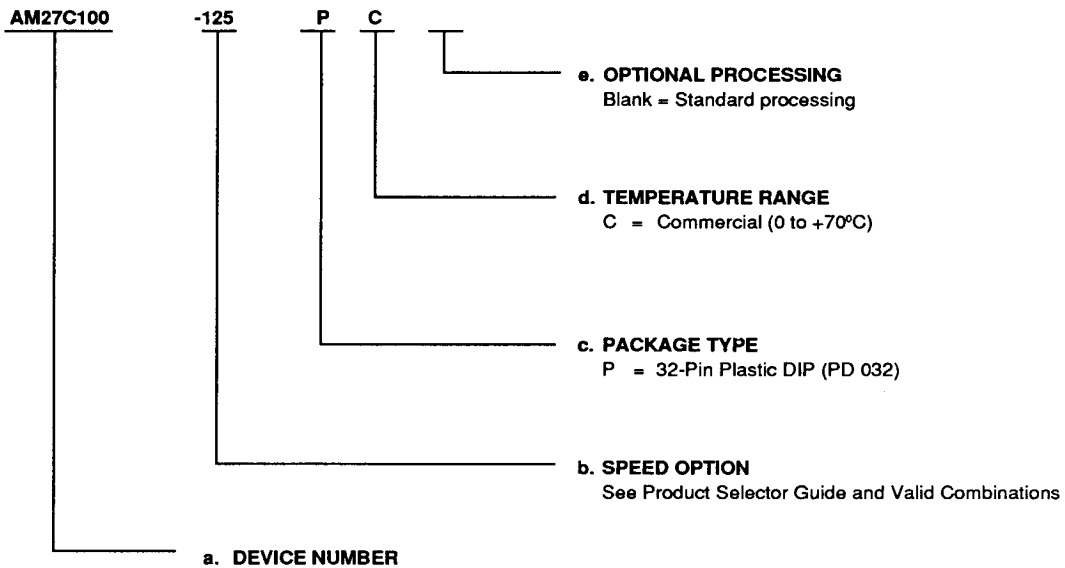
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

## ORDERING INFORMATION

### OTP Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

**a. Device Number**
**b. Speed Option**
**c. Package Type**
**d. Temperature Range**
**e. Optional Processing**




| Valid Combinations | |
|---|---|
| AM27C100-125 | PC |
| AM27C100-155 | |
| AM27C100-200 | |
| AM27C100-255 | |

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

## FUNCTIONAL DESCRIPTION

### Erasing the Am27C100

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C100 to an ultraviolet light source. A dosage of 15 W seconds/cm² is required to completely erase an Am27C100. This dosage can be obtained by exposure to an ultraviolet Lamp-wavelength of 2537 Angstroms (Å)–with intensity of 12,000 µW/cm² for 15 to 20 minutes. The Am27C100 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C100, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C100 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

### Programming the Am27C100

Upon delivery, or after each erasure, the Am27C100 has all 1,048,576 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27C100 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the $V_{PP}$ pin, $\overline{CE}$ and $\overline{PGM}$ is at $V_{IL}$, and $\overline{OE}$ is at $V_{IH}$.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite programming algorithm (shown in Figure 1) reduces programming time by using initial 100 µs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the EPROM.

The Flashrite programming algorithm programs and verifies at $V_{CC}$ = 6.25 V and $V_{PP}$ = 12.75 V. After the final address is completed, all bytes are compared to the original data with $V_{CC} = V_{PP} = 5.25$ V.

### Program Inhibit

Programming of multiple Am27C100s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C100s may be common. A TTL low-level program pulse applied to an Am27C100 $\overline{CE}$ input with $V_{PP}$ = 12.75 ± 0.25 V, $\overline{PGM}$ is LOW, and $\overline{OE}$ HIGH will program that Am27C100. A high-level $\overline{CE}$ input inhibits the other Am27C100s from being programmed.

### Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at $V_{IL}$, $\overline{PGM}$ at $V_{IH}$, and $V_{PP}$ between 12.5 V and 13.0 V.

### Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C100.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line $A_9$ of the Am27C100. Two identifier bytes may then be sequenced from the device outputs by toggling address line $A_0$ from $V_{IL}$ to $V_{IH}$. All other address lines must be held at $V_{IL}$ during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code, and byte 1($A_0 = V_{IH}$), the device identifier code. For the Am27C100, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB ($DQ_7$) defined as the parity bit.

### Read Mode

The Am27C100 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time ($t_{ACC}$) is equal to the delay from $\overline{CE}$ to output ($t_{CE}$). Data is available at the outputs $t_{OE}$ after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

### Standby Mode

The Am27C100 has a CMOS standby mode which reduces the maximum $V_{CC}$ current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at $V_{CC}$ ± 0.3 V. The Am27C100 also has a TTL-standby mode which reduces the maximum $V_{CC}$ current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at $V_{IH}$. When in stand-by mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

### Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

**System Applications**

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between $V_{CC}$ and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between $V_{CC}$ and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

## MODE SELECT TABLE

| Mode \ Pins | | $\overline{CE}$ | $\overline{OE}$ | $\overline{PGM}$ | $A_9$ | $A_9$ | $V_{PP}$ | Outputs |
|---|---|---|---|---|---|---|---|---|
| Read | | $V_{IL}$ | $V_{IL}$ | X | X | X | X | $D_{OUT}$ |
| Output Disable | | $V_{IL}$ | $V_{IH}$ | X | X | X | X | Hi-Z |
| Standby (TTL) | | $V_{IH}$ | X | X | X | X | X | Hi-Z |
| Standby (CMOS) | | $V_{CC} \pm 0.3$ V | X | X | X | X | X | Hi-Z |
| Program | | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X | X | $V_{PP}$ | $D_{IN}$ |
| Program Verify | | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | X | $V_{PP}$ | $D_{OUT}$ |
| Program Inhibit | | $V_{IH}$ | X | X | X | X | $V_{PP}$ | Hi-Z |
| Auto Select (Note 3) | Manufacturer Code | $V_{IL}$ | $V_{IL}$ | X | $V_{IL}$ | $V_H$ | X | 01H |
| | Device Code | $V_{IL}$ | $V_{IL}$ | X | $V_{IH}$ | $V_H$ | X | 0DH |

**Notes:**

1. $V_H = 12.0 \text{ V} \pm 0.5 \text{ V}$
2. X = Either $V_{IH}$ or $V_{IL}$
3. $A_1 - A_8 = A_{10} - A_{16} = V_{IL}$
4. See DC Programming Characteristics for $V_{PP}$ voltage during programming.

## ABSOLUTE MAXIMUM RATINGS

**Storage Temperature**

| | |
|---|---|
| OTP products | –65 to 125°C |
| All other products | –65 to 150°C |
| Ambient Temperature with Power Applied | –55 to +125°C |

**Voltage with Respect to Ground:**

| | |
|---|---|
| All pins except $A_9$, $V_{PP}$, and $V_{CC}$ (Note 1) | –0.6 to $V_{CC}$ +0.6 V |
| $A_9$ and $V_{PP}$ (Note 2) | –0.6 to 13.5 V |
| $V_{CC}$ | –0.6 to 7.0 V |

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

**Notes:**

1. During transitions, the inputs may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to $V_{CC}$ + 2.0 V for periods up to 20 ns.
2. During transitions, $A_9$ and $V_{PP}$ may overshoot GND to –2.0 V for periods of up to 20 ns. $A_9$ and $V_{PP}$ must not exceed 13.5 V for any period of time.

## OPERATING RANGES

**Commercial (C) Devices**

| | |
|---|---|
| Case Temperature ($T_C$) | 0 to +70°C |

**Industrial (I) Devices**

| | |
|---|---|
| Case Temperature ($T_C$) | –40 to +85°C |

**Supply Read Voltages:**

| | |
|---|---|
| $V_{CC}$ for Am27C100-XX5 | +4.75 to + 5.25 V |
| $V_{CC}$ for Am27C100-XX0 | +4.50 to +5.50 V |

*Operating ranges define those limits between which the*

## DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 4, 5, and 8)

**TTL and NMOS Inputs**

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -400\ \mu A$ | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 2.1$ mA | | 0.45 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | $V_{CC} + 0.5$ | V |
| $V_{IL}$ | Input LOW Voltage | | −0.5 | +0.8 | V |
| $I_{LI}$ | Input Load Current | $V_{IN} = 0$ V to $+ V_{CC}$ | | 1.0 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT} = 0$ V to $+ V_{CC}$ | | 10 | µA |
| $I_{CC1}$ | $V_{CC}$ Active Current (Note 5) | $\overline{CE} = V_{IL}$, f =5 MHz (Open Outputs) $I_{OUT} = 0$ mA | | 30 | mA |
| $I_{CC2}$ | $V_{CC}$ Standby Current | $\overline{CE} = V_{IH}$ | | 1.0 | mA |
| $I_{PP1}$ | $V_{PP}$ Current During Read (Note 6) | $\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$ | | 100 | µA |

**CMOS Inputs**

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -400\ \mu A$ | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 2.1$ mA | | 0.45 | V |
| $V_{IH}$ | Input HIGH Voltage | | $V_{CC} - 0.3$ | $V_{CC} + 0.3$ | V |
| $V_{IL}$ | Input LOW Voltage | | −0.5 | +0.8 | V |
| $I_{LI}$ | Input Load Current | $V_{IN} = 0$ V to $+ V_{CC}$ | | 1.0 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT} = 0$ V to $+ V_{CC}$ | | 10 | µA |
| $I_{CC1}$ | $V_{CC}$ Active Current (Note 5) | $\overline{CE} = V_{IL}$, f = 5 MHz $I_{OUT} = 0$ mA (Open Outputs) | | 30 | mA |
| $I_{CC2}$ | $V_{CC}$ Standby Current | $\overline{CE} = V_{CC} \pm 0.3$ V | | 100 | µA |
| $I_{PP1}$ | $V_{PP}$ Current During Read (Note 6) | $\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$ | | 100 | µA |

## CAPACITANCE (Notes 2, 3, and 7)

| Parameter Symbol | Parameter Description | Test Conditions | CDV032 | | Unit |
|---|---|---|---|---|---|
| | | | Typ. | Max. | |
| $C_{IN}$ | Address Input Capacitance | $V_{IN}$ = 0 V | 12 | 14 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 V | 14 | 17 | pF |

**Notes:**

1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$, and removed simultaneously or after $V_{PP}$.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled, not 100% tested.
4. **Caution:** the Am27C100 must not be removed from (or inserted into) a socket when $V_{CC}$ or $V_{PP}$ is applied.
5. $I_{CC1}$ is tested with $\overline{OE}$ = $V_{IH}$ to simulate open outputs.
6. Maximum active power usage is the sum of $I_{CC}$ and $I_{PP}$.
7. $T_A$ = +25°C, f = 1 MHz.
8. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on input pins may overshoot to $V_{CC}$ + 2.0 V for periods less than 20 ns.

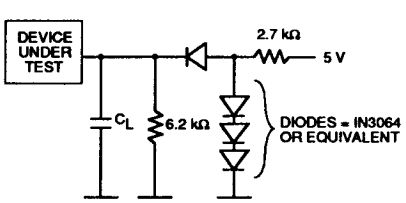
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3, and 4)

| Parameter Symbols | | Parameter Description | Test Condition | | Am27C100 | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Standard | | | | -105 | -120, -125 | -150, -155 | -200 | -255 | |
| $t_{AVQV}$ | $t_{ACC}$ | Address to Output Delay | $\overline{CE} = \overline{OE} = V_{IL}$ | Min. | | – | – | – | – | ns |
| | | | | Max. | 100 | 120 | 150 | 200 | 250 | |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable to Output Delay | $\overline{OE} = V_{IL}$ | Min. | | – | – | – | – | ns |
| | | | | Max. | 100 | 120 | 150 | 200 | 250 | |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable to Output Delay | $\overline{CE} = V_{IL}$ | Min. | | – | – | – | – | ns |
| | | | | Max. | 50 | 50 | 65 | 75 | 100 | |
| $t_{EHQZ}$ | $t_{DF}$ | Chip Enable HIGH or Output Enable HIGH, Whichever Comes First, to Output Float | | Min. | | 0 | 0 | 0 | 0 | ns |
| $t_{GHQZ}$ | (Note 2) | | | Max. | 35 | 35 | 35 | 40 | 40 | |
| $t_{AXQX}$ | $t_{OH}$ | Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, Whichever Occurred First | | Min. | 0 | 0 | 0 | 0 | 0 | ns |
| | | | | Max. | | – | – | – | – | |

**Notes:**

1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$, and removed simultaneously or after $V_{PP}$.
2. This parameter is only sampled, not 100% tested.
3. **Caution:** The Am27C100 must not be removed from (or inserted into) a socket or board when $V_{pp}$ or $V_{cc}$ is applied.
4. Output Load: 1 TTL gate and $C_L$ = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 to 2.4 V
   Timing Measurement Reference Level - Inputs: 0.8 to 2.0 V
   Outputs: 0.8 to 2.0V

## SWITCHING TEST CIRCUIT




$C_L$ = 100 pF including jig capacitance.

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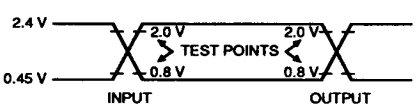
## SWITCHING TEST WAVEFORM




AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns.

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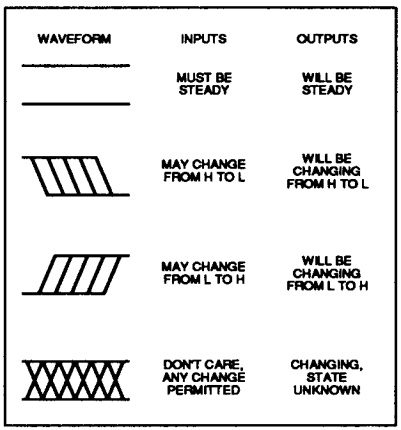
## KEY TO SWITCHING WAVEFORMS

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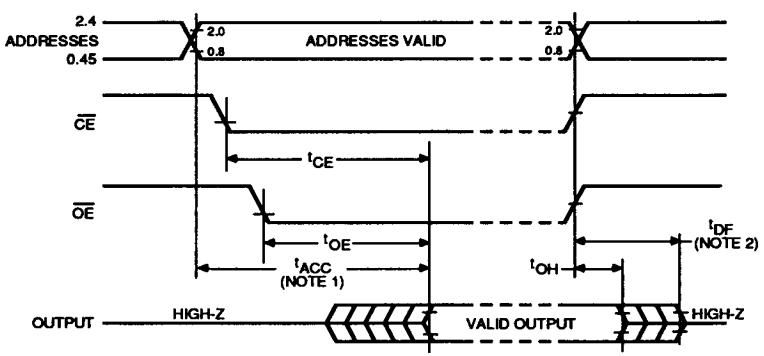
## SWITCHING WAVEFORMS

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**Notes:**

1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{ACC}$.
2. $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

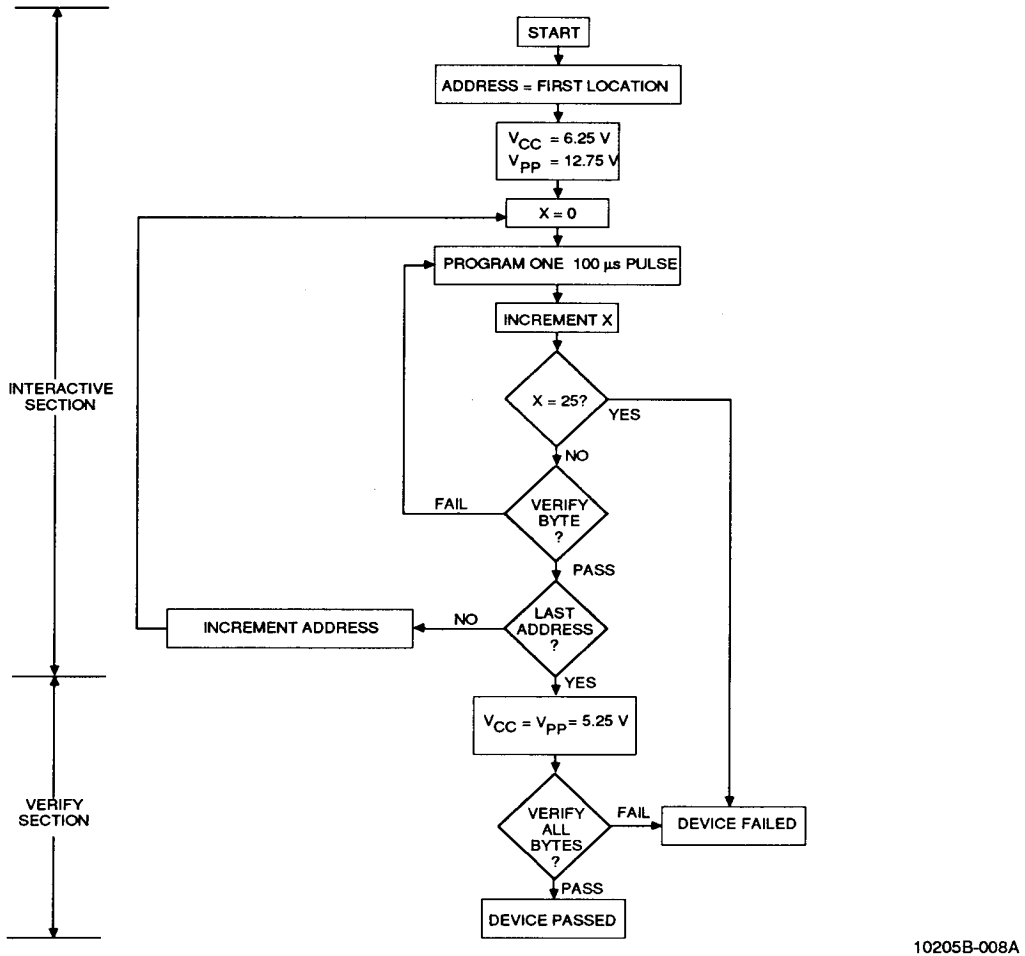



**Figure 1. Flashrite Programming Flow Chart**

## DC PROGRAMMING CHARACTERISTICS ($T_A$ = +25°C ± 5°C) (Notes 1, 2, and 3)

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Current (All Inputs) | $V_{IN} = V_{IL}$ or $V_{IH}$ | | 10.0 | µA |
| $V_{IL}$ | Input LOW Level (All Inputs) | | – 0.3 | 0.8 | V |
| $V_{IH}$ | Input HIGH Level | | 2.0 | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output LOW Voltage During Verify | $I_{OL}$ = 2.1 mA | | 0.45 | V |
| $V_{OH}$ | Output HIGH Voltage During Verify | $I_{OH}$ = – 400 µA | 2.4 | | V |
| $V_H$ | $A_9$ Auto Select Voltage | | 11.5 | 12.5 | V |
| $I_{CC}$ | $V_{CC}$ Supply Current (Program & Verify) | | | 50 | mA |
| $I_{PP}$ | $V_{PP}$ Supply Current (Program) | CE = $V_{IL}$, $\overline{OE}$ = $V_{IH}$ | | 30 | mA |
| $V_{CC}$ | Supply Voltage | | 6.00 | 6.50 | V |
| $V_{PP}$ | Programming Voltage | | 12.5 | 13.0 | V |

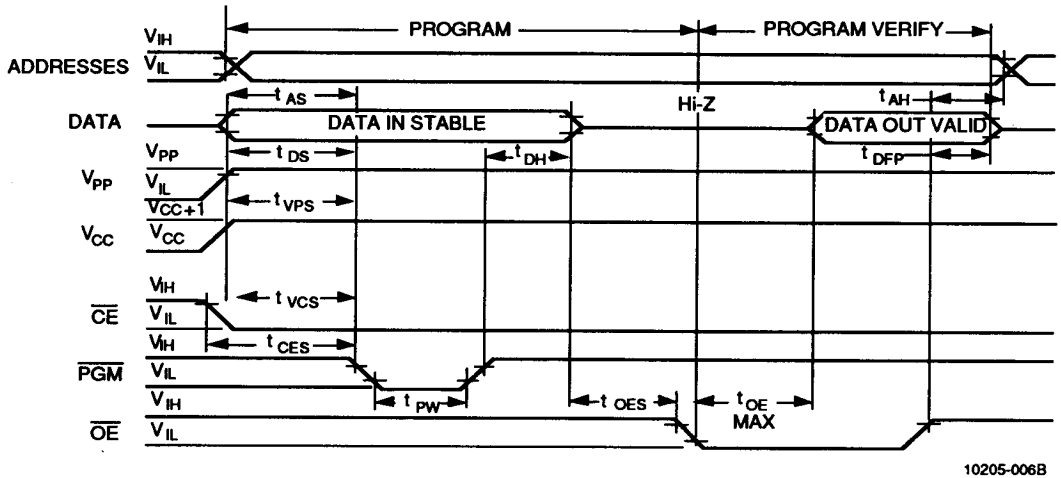
## SWITCHING PROGRAMMING CHARACTERISTICS ($T_A$ = +25°C ± 5°C) (Notes 1, 2, and 3)

| Parameter Symbol | | Parameter Description | Min. | Max. | Unit |
|---|---|---|---|---|---|
| JEDEC | Standard | | | | |
| $t_{AVEL}$ | $t_{AS}$ | Address Setup Time | 2 | | µs |
| $t_{DZGL}$ | $t_{OES}$ | $\overline{OE}$ Setup Time | 2 | | µs |
| $t_{DVEL}$ | $t_{DS}$ | Data Setup Time | 2 | | µs |
| $t_{GHAX}$ | $t_{AH}$ | Address Hold Time | 0 | | µs |
| $t_{EHDX}$ | $t_{DH}$ | Data Hold Time | 2 | | µs |
| $t_{GHQZ}$ | $t_{DFP}$ | Output Enable to Output Float Delay | 0 | 130 | ns |
| $t_{VPS}$ | $t_{VPS}$ | $V_{PP}$ Setup Time | 2 | | µs |
| $t_{ELEH1}$ | $t_{PW}$ | $\overline{PGM}$ Program Pulse Width | 95 | 105 | µs |
| $t_{VCS}$ | $t_{VCS}$ | $V_{CC}$ Setup Time | 2 | | µs |
| $t_{ELPL}$ | $t_{CES}$ | $\overline{CE}$ Setup Time | 2 | | µs |
| $t_{GLQV}$ | $t_{OE}$ | Data Valid from $\overline{OE}$ | | 150 | ns |

**Notes:**

1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$, and removed simultaneously or after $V_{PP}$.
2. When programming the Am27C100, a 0.1 µF capacitor is required across $V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.
3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

## Flashrite PROGRAMMING ALGORITHM WAVEFORM (Notes 1 and 2)




**Notes:**

1. The input timing reference level is 0.8 V for $V_{IL}$ ans 2.0 V for a $V_{IH}$.
2. $t_{OE}$ and $t_{DFB}$ are characteristics of the device but must be accommodated by the programmer.