

SN54ALS874B, SN54ALS876A, SN54AS874, SN54AS876 SN74ALS874B, SN74ALS876A, SN74AS874, SN74AS876 DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

D2661, APRIL 1982 — REVISED MAY 1986

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Choice of True or Inverting Logic
'ALS874B, 'AS874 True Outputs
'ALS876A, 'AS876 Inverting Outputs
- Asynchronous Clear
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

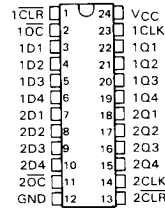
These dual four-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The edge-triggered flip-flops enter data on the low-to-high transition of the clock. The 'ALS874B and 'AS874 have CLR inputs and noninverting Q outputs; the 'ALS876A and 'AS876 have PRE inputs and inverting Q outputs. In each case, taking this input low causes the four Q or Q outputs to go low independently of the clock.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS' and SN74AS' devices are characterized for operation from 0°C to 70°C.

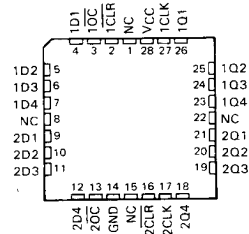
SN54ALS874B, SN54AS874 . . . JT PACKAGE
SN74ALS874B, SN74AS874 . . . DW OR NT PACKAGE

(TOP VIEW)



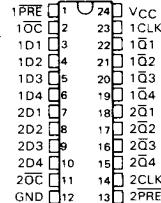
SN54ALS874B, SN54AS874 . . . FK PACKAGE
SN74ALS874B, SN74AS874 . . . FN PACKAGE

(TOP VIEW)



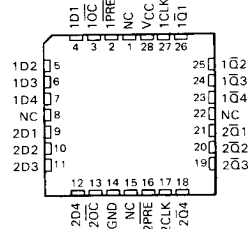
SN54ALS876A, SN54AS876 . . . JT PACKAGE
SN74ALS876A, SN74AS876 . . . DW OR NT PACKAGE

(TOP VIEW)



SN54ALS876A, SN54AS876 . . . FK PACKAGE
SN74ALS876A, SN74AS876 . . . FN PACKAGE

(TOP VIEW)



NC—No internal connection

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ALS and AS Circuits

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**SN54ALS874B, SN54ALS876A, SN54AS874, SN54AS876
SN74ALS874B, SN74ALS876A, SN74AS874, SN74AS876
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS**

FUNCTION TABLES

'ALS874B, 'AS874 (EACH FLIP-FLOP)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	CLK	D	Q
L	L	X	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

'ALS876A, 'AS876 (EACH FLIP-FLOP)

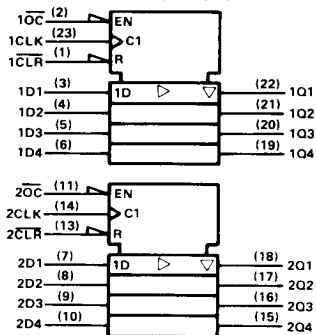
INPUTS				OUTPUT
OC	$\overline{PRE}$	CLK	D	$\overline{Q}$
L	L	X	X	L
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

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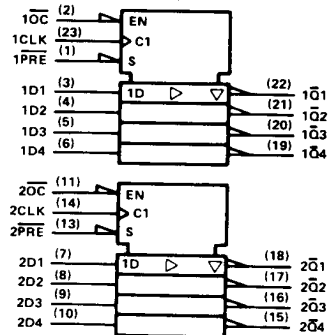
ALS and AS Circuits

logic symbols†

'ALS874B, 'AS874



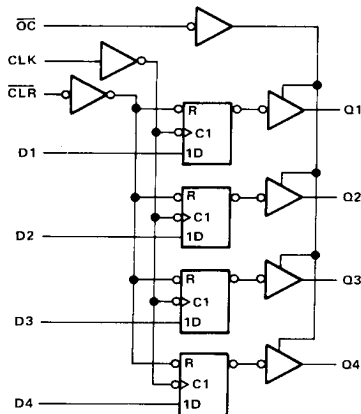
'ALS876A, 'AS876



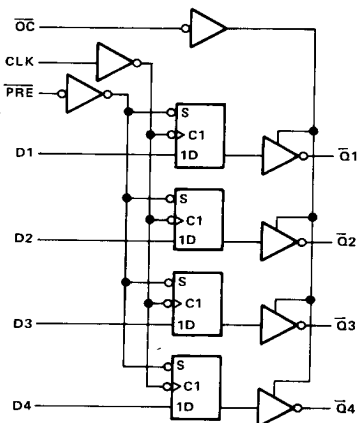
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617.12.

logic diagrams (positive logic)

'ALS874B, 'AS874 (EACH QUAD FLIP-FLOP)



'ALS876A, 'AS876 (EACH QUAD FLIP-FLOP)



Pin numbers shown are for DW, JT, and NT packages.

SN54ALS874B, SN54ALS876A
SN74ALS874B, SN74ALS876A
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54ALS874B, SN54ALS876A	-55°C to 125°C
SN74ALS874B, SN74ALS876A	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

			SN54ALS874B			SN74ALS874B			UNIT
			SN54ALS876A			SN74ALS876A			
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.7			0.8			V
I _{OH}	High-level output current		-1			-2.6			mA
I _{OL}	Low-level output current		12			24			mA
f _{clock}	Clock frequency		0	25		0	30		MHz
t _w	Pulse duration	PRE or CLR low	10			10			ns
		CLK high	20			16.5			
		CLK low	20			16.5			
t _{su}	Setup time before CLK↑	Data	15			15			ns
		PRE or CLR inactive	10			10			
t _h	Hold time, data after CLK↑		4			0			ns
T _A	Operating free-air temperature		-55			125			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS874B SN54ALS876A		SN74ALS874B SN74ALS876A		UNIT
				MIN	TYP†	MAX	MIN	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA		-1.2		-1.2		V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA		V _{CC} - 2		V _{CC} - 2		V
		V _{CC} = 4.5 V, I _{OH} = -1 mA		2.4 3.3				
		V _{CC} = 4.5 V, I _{OH} = -2.6 mA				2.4 3.2		
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 12 mA		0.25 0.4		0.25 0.4		V
		V _{CC} = 4.5 V, I _{OL} = 24 mA				0.35 0.5		
I _{OZH}		V _{CC} = 5.5 V, V _O = 2.7 V		20		20		μA
I _{OZL}		V _{CC} = 5.5 V, V _O = 0.4 V		-20		-20		μA
I _I		V _{CC} = 5.5 V, V _I = 7 V		0.1		0.1		mA
I _{IH}		V _{CC} = 5.5 V, V _I = 2.7 V		20		20		μA
I _{IL}		V _{CC} = 5.5 V, V _I = 0.4 V		-0.2		-0.2		mA
I _O [‡]		V _{CC} = 5.5 V, V _O = 2.25 V		-30 -112		-30 -112		mA
I _{CC}	'ALS874B	V _{CC} = 5.5 V	Output high	14	21	14	21	mA
			Outputs low	19	30	19	30	
			Outputs disabled	20	32	20	32	
	'ALS876A		Outputs high	14	21	14	21	
			Outputs low	18	29	18	29	
			Outputs disabled	20	31	20	31	

†All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN54ALS874B, SN54ALS876A
SN74ALS874B, SN74ALS876A
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

'ALS874B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX			UNIT
			'ALS874B			SN54ALS874B		SN74ALS874B	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX
f _{max}			40	50		25		30	MHz
t _{PLH}	CLK	Any Q	8	10		4	15	4	14
t _{PHL}			8	13		4	15	4	14
t _{PHL}	CLR	Any Q	11	14		5	20	5	17
t _{PZH}	OC	Any Q	9	12		4	21	4	18
t _{PZL}			11	15		4	21	4	18
t _{PHZ}	OC	Any Q	6	8		2	12	2	10
t _{PLZ}			5.7	8		3	15	3	12

'ALS876A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25°C			V _{CC} = 4.5 C to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX			UNIT
			'ALS876A			SN54ALS876A		SN74ALS876A	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX
f _{max}			40	50		25		30	MHz
t _{PLH}	CLK	Any Q̄	8	11		4	15	4	14
t _{PHL}			9	12		4	15	4	14
t _{PHL}	PRE	Any Q̄	10	16		6	22	6	19
t _{PZH}	OC	Any Q̄	10	13		4	21	4	18
t _{PZL}			11	15		4	21	4	18
t _{PHZ}	OC	Any Q̄	6	8		2	12	2	10
t _{PLZ}			7	10		3	15	3	13

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS874, SN54AS876, SN74AS874, SN74AS876

DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Operating free-air temperature range: SN54AS874, SN54AS876	-55°C to 125°C
SN74AS874, SN74AS876	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

			SN54AS874 SN54AS876			SN74AS874 SN74AS876			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				-12			-15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency		0		100	0		125	MHz
t_w	Pulse duration	PRE or CLR low	4			2			ns
		CLK high	4			3			
		CLK low	5			4			
t_{su}	Setup time before CLK†	Data	2.5			2			ns
		PRE or CLR inactive	5			4			
t_h	Hold time, data after CLK†		1			1			ns
T_A	Operating free-air temperature		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS874 SN54AS876			SN74AS874 SN74AS876			UNIT					
				MIN	TYP†	MAX	MIN	TYP†	MAX						
V _{IK}		V _{CC} = 4.5 V,	I _I = -18 mA	-1.2			-1.2			V					
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA		V _{CC} - 2			V _{CC} - 2			V					
		V _{CC} = 4.5 V, I _{OH} = -12 mA		2.4	3.2										
		V _{CC} = 4.5 V, I _{OH} = -15 mA					2.4	3.3							
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 32 mA		0.25			0.4			V					
		V _{CC} = 4.5 V, I _{OL} = 48 mA					0.35								
I _{OZH}		V _{CC} = 5.5 V, V _O = 2.7 V		50			50			μA					
I _{OZL}		V _{CC} = 5.5 V, V _O = 0.4 V		-50			-50			μA					
I _I		V _{CC} = 5.5 V, V _I = 7 V		0.1			0.1			mA					
I _{IH}		V _{CC} = 5.5 V, V _I = 2.7 V		20			10			μA					
I _{IL}		D All other		V _{CC} = 5.5 V, V _I = 0.4 V		-3		-2		mA					
						-0.5		-0.5							
I _O ‡		V _{CC} = 5.5 V, V _O = 2.25 V		-30		-112		-30		-112	mA				
I _{CC}		V _{CC} = 5.5 V		Output high		82		133		82		133	mA		
				Outputs low		92		149		92		149			
				Outputs disabled		100		160		100		160			
				AS876		Outputs high		88		142		88		142	
						Outputs low		94		150		94		150	
						Outputs disabled		100		160		100		160	

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN54AS874, SN54AS876, SN74AS874, SN74AS876
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

AS874 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 4.5 V to 5.5 V, CL = 50 pF, R1 = 500 Ω, R2 = 500 Ω, TA = MIN to MAX				UNIT
			SN54AS874		SN74AS874		
			MIN	MAX	MIN	MAX	
fmax			100		125		MHz
tPLH	CLK	Any Q	3	11.5	3	8.5	ns
tPHL			4	12.5	4	10.5	
tPHL	CLR	Any Q	4	11	4	9.5	ns
tPZH	OC	Any Q	2	8	2	7	ns
tPZL			3	11.5	3	10.5	
tPHZ	OC	Any Q	2	7	2	6	ns
tPLZ			2	8.5	2	7.5	

AS876 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX				UNIT
			SN54AS876		SN74AS876		
			MIN	MAX	MIN	MAX	
f _{max}			100		125		MHz
t _{PLH}	CLK	Any $\overline{Q}$	3	11.5	3	8.5	ns
t _{PHL}			4	12.5	4	10.5	
t _{PHL}	$\overline{PRE}$	Any $\overline{Q}$	4	11	4	9.5	ns
t _{PZH}	$\overline{OC}$	Any $\overline{Q}$	2	8	2	7	ns
t _{PZL}			3	11.5	3	10.5	
t _{PHZ}	$\overline{OC}$	Any $\overline{Q}$	2	7	2	6	ns
t _{PLZ}			2	7	2	6	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.