# P4C198/P4C198L, P4C198A/P4C198AL ULTRA HIGH SPEED 16K x 4 STATIC CMOS RAMS

## FEATURES

- **Full CMOS, 6T Cell**
- **High Speed (Equal Access and Cycle Times)**
  - **– 10/12/15/20/25 ns (Commercial)**
  - **– 12/15/20/25/35 ns (Industrial)**
  - **– 15/20/25/35/45 ns (Military)**
- **Low Power Operation (Commercial/Military)**
  - **– 715 mW Active – 12/15**
  - **– 550/660 mW Active – 20/25/35/45/55**
  - **– 193/220 mW Standby (TTL Input)**
  - **– 83/110 mW Standby (CMOS Input) P4C198/198A**
  - **– 9 mW Standby (CMOS Input) P4C198L/198AL (Military)**
- **5V ± 10% Power Supply**
- **Data Retention, 10 μA Typical Current from 2.0V P4C198L/198AL (Military)**
- **Output Enable & Chip Enable Control Functions**
  - **– Single Chip Enable P4C198**
  - **– Dual Chip Enable P4C198A**
- **Common Inputs and Outputs**
- **Fully TTL Compatible Inputs and Outputs**
- **Standard Pinout (JEDEC Approved)**
  - **– 24-Pin 300 mil DIP**
  - **– 24-Pin 300 mil SOJ (P4C198 only)**
  - **– 28-Pin 350 x 550 mil LCC (P4C198 only)**

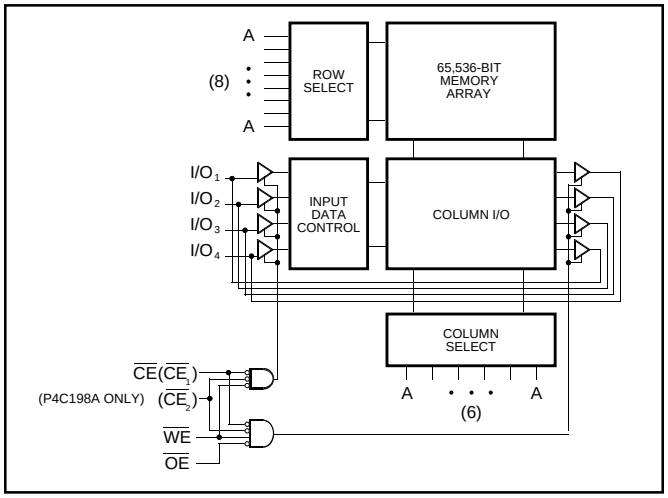
## DESCRIPTION

The P4C198/L and P4C198A/L are 65,536-bit ultra high-speed static RAMs organized as 16K x 4. Each device features an active low Output Enable control to eliminate data bus contention. The P4C198/L also have an active low Chip Enable (the P4C198A/L have two Chip Enables, both active low) for easy system expansion. The CMOS memories require no clocks or refreshing and have equal access and cycle times. Inputs are fully TTL-compatible. The RAMs operate from a single 5V ± 10% tolerance power supply. Data integrity is maintained with supply voltages down to 2.0V. Current drain is typically 10 μA from a 2.0V supply.

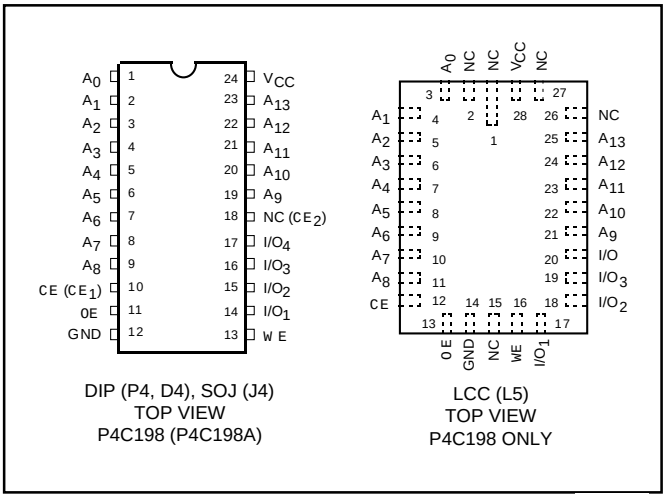
Access times as fast as 12 nanoseconds are available, permitting greatly enhanced system operating speeds. CMOS is used to reduce power consumption to a low 715 mW active, 193 mW standby.

The P4C198/L and P4C198A/L are available in 24-pin 300 mil DIP and SOJ, and 28-pin 350 x 550 mil LCC packages providing excellent board level densities.

## FUNCTIONAL BLOCK DIAGRAM




## PIN CONFIGURATIONS




DIP (P4, D4), SOJ (J4)
TOP VIEW
P4C198 (P4C198A)

LCC (L5)
TOP VIEW
P4C198 ONLY

## MAXIMUM RATINGS[1]

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Power Supply Pin with Respect to GND | –0.5 to +7 | V |
| $V_{TERM}$ | Terminal Voltage with Respect to GND (up to 7.0V) | –0.5 to $V_{CC}$ +0.5 | V |
| $T_A$ | Operating Temperature | –55 to +125 | °C |

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_{BIAS}$ | Temperature Under Bias | –55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $P_T$ | Power Dissipation | 1.0 | W |
| $I_{OUT}$ | DC Output Current | 50 | mA |

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade(2) | Ambient Temperature | GND | $V_{CC}$ |
|---|---|---|---|
| Military | –55°C to +125°C | 0V | 5.0V ± 10% |
| Commercial | 0°C to +70°C | 0V | 5.0V ± 10% |
| Industrial | –40°C to +85°C | 0V | 5.0V ± 10% |

## CAPACITANCES[4]

$V_{CC}$ = 5.0V, $T_A$ = 25°C, f = 1.0MHz

| Symbol | Parameter | Conditions | Typ. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 7 | pF |

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

| Symbol | Parameter | Test Conditions | P4C198 / 198A | | P4C198L / 198AL | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $V_{IH}$ | Input High Voltage | | 2.2 | $V_{CC}$ +0.5 | 2.2 | $V_{CC}$ +0.5 | V |
| $V_{IL}$ | Input Low Voltage | | –0.5[3] | 0.8 | –0.5[3] | 0.8 | V |
| $V_{HC}$ | CMOS Input High Voltage | | $V_{CC}$ –0.2 | $V_{CC}$ +0.5 | $V_{CC}$ –0.2 | $V_{CC}$ +0.5 | V |
| $V_{LC}$ | CMOS Input Low Voltage | | –0.5[3] | 0.2 | –0.5(3) | 0.2 | V |
| $V_{CD}$ | Input Clamp Diode Voltage | $V_{CC}$ = Min., $I_{IN}$ = 18 mA | | –1.2 | | –1.2 | V |
| $V_{OL}$ | Output Low Voltage (TTL Load) | $I_{OL}$ = +10 mA, $V_{CC}$ = Min.<br>$I_{OL}$ = +8 mA, $V_{CC}$ = Min. | 0.5 | <br>0.4 | 0.5 | <br>0.4 | V<br>V |
| $V_{OH}$ | Output High Voltage (TTL Load) | $I_{OH}$ = –4 mA, $V_{CC}$ = Min. | 2.4 | | 2.4 | | V |
| $I_{LI}$ | Input Leakage Current | $V_{CC}$ = Max. Mil.<br>$V_{IN}$ = GND to $V_{CC}$ Com'l. | –10<br>–5 | +10<br>+5 | –5<br>n/a | +5<br>n/a | µA |
| $I_{LO}$ | Output Leakage Current | $V_{CC}$ = Max., $\overline{CE}$ = $V_{IH}$, Mil.<br>$V_{OUT}$ = GND to $V_{CC}$ Com'l. | –10<br>–5 | +10<br>+5 | –5<br>n/a | +5<br>n/a | µA |
| $I_{SB}$ | Standby Power Supply Current (TTL Input Levels) | $\overline{CE}_1$, $\overline{CE}_2 \geq V_{IH}$ Mil.<br>$V_{CC}$ = Max ., Ind./Com'l.<br>f = Max., Outputs Open | ——<br>—— | 40<br>35 | ——<br>—— | 40<br>n/a | mA |
| $I_{SB1}$ | Standby Power Supply Current (CMOS Input Levels) | $\overline{CE}_1$, $\overline{CE}_2 \geq V_{IH}$ Mil.<br>$V_{CC}$ = Max., Ind./Com'l.<br>f = 0, Outputs Open<br>$V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$ | ——<br>—— | 20<br>15 | ——<br>—— | 1.5<br>n/a | mA |

n/a = Not Applicable

**Notes:**

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM ratingconditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with $V_{IL}$ and $I_{IL}$ not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20ns.
4. This parameter is sampled and not 100% tested.

## POWER DISSIPATION CHARACTERISTICS VS. SPEED

| Symbol | Parameter | Temperature Range | –10 | –12 | –15 | –20 | –25 | –35 | –45 | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Dynamic Operating Current* | Commercial | 180 | 170 | 160 | 155 | 150 | N/A | N/A | mA |
| | | Industrial | N/A | 180 | 170 | 160 | 155 | 150 | N/A | mA |
| | | Military | N/A | N/A | 170 | 160 | 155 | 150 | 145 | mA |

*$V_{CC}$ = 5.5V. Tested with outputs open. f = Max. Switching inputs are 0V and 3V.

198: $\overline{CE}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$

198A: $CE_1$ = $V_{IL}$, $CE_2$ = $V_{IL}$. $\overline{OE}$ = $V_{IH}$

## DATA RETENTION CHARACTERISTICS (P4C198L/P4C198AL Military Temperature Only)

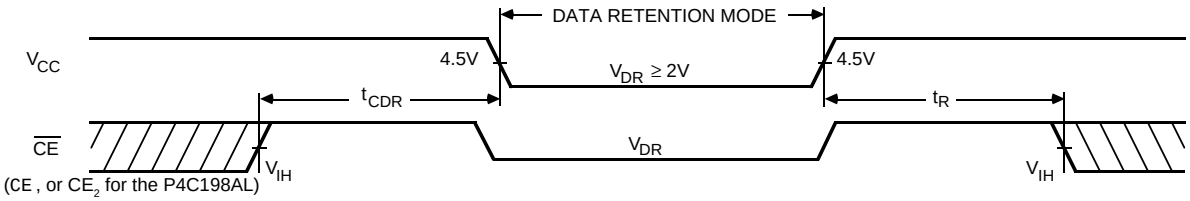
| Symbol | Parameter | Test Condition | Min | Typ.* $V_{CC}$= 2.0V | Typ.* $V_{CC}$= 3.0V | Max $V_{CC}$= 2.0V | Max $V_{CC}$= 3.0V | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | 2.0 | | | | | V |
| $I_{CCDR}$ | Data Retention Current | $\overline{CE}$ ≥$V_{CC}$ – 0.2V, $V_{IN}$ ≥ $V_{CC}$ – 0.2V or $V_{IN}$ ≤ 0.2V | | 10 | 15 | 600 | 900 | µA |
| $t_{CDR}$ | Chip Deselect to Data Retention Time | | 0 | | | | | ns |
| $t_R$ † | Operation Recovery Time | | $t_{RC}$ § | | | | | ns |

*$T_A$ = +25°C

§$t_{RC}$ = Read Cycle Time

†This parameter is guaranteed but not tested.

## DATA RETENTION WAVEFORM

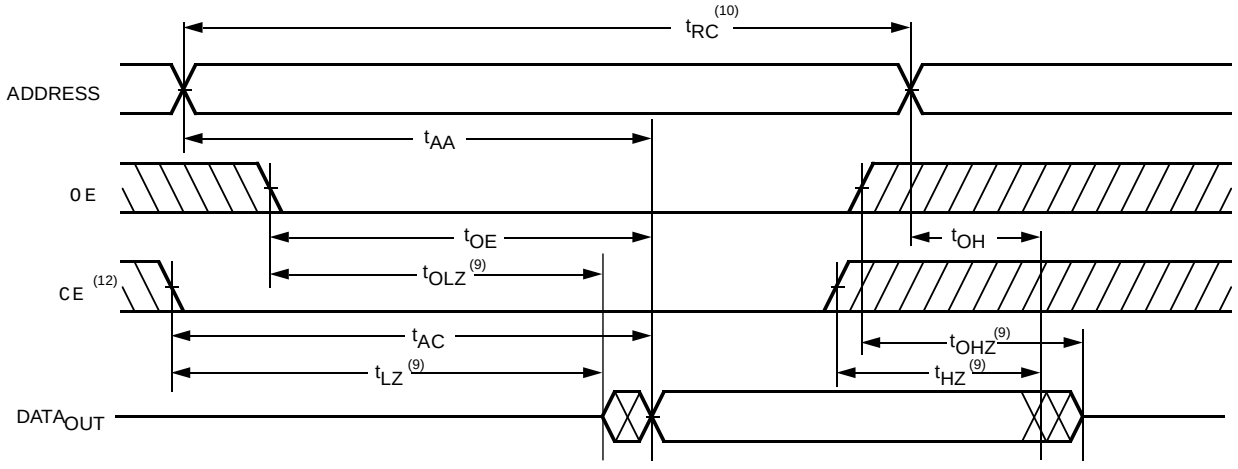


## AC CHARACTERISTICS—READ CYCLE

($V_{CC}$ = 5V ± 10%, All Temperature Ranges)[2]

| Sym. | Parameter | -10 | | -12 | | -15 | | -20 | | -25 | | -35 | | -45 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{RC}$ | Read Cycle Time | 10 | | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | | ns |
| $t_{AA}$ | Address Access Time | | 10 | | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | ns |
| $t_{AC}$ | Chip Enable Access Time | | 10 | | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | ns |
| $t_{OH}$ | Output Hold from Address Change | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | ns |
| $t_{LZ}$ | Chip Enable to Output in Low Z | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | ns |
| $t_{HZ}$ | Chip Disable to Output in High Z | | 6 | | 7 | | 8 | | 10 | | 10 | | 14 | | 15 | ns |
| $t_{OE}$ | Output Enable Low to Data Valid | | 6 | | 7 | | 9 | | 12 | | 15 | | 25 | | 30 | ns |
| $t_{OLZ}$ | Output Enable to Output in Low Z | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | ns |
| $t_{OHZ}$ | Output Disable to Output in High Z | | 6 | | 7 | | 9 | | 9 | | 10 | | 14 | | 15 | ns |
| $t_{PU}$ | Chip Enable to Power Up Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{PD}$ | Chip Disable to Power Down Time | | 10 | | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | ns |

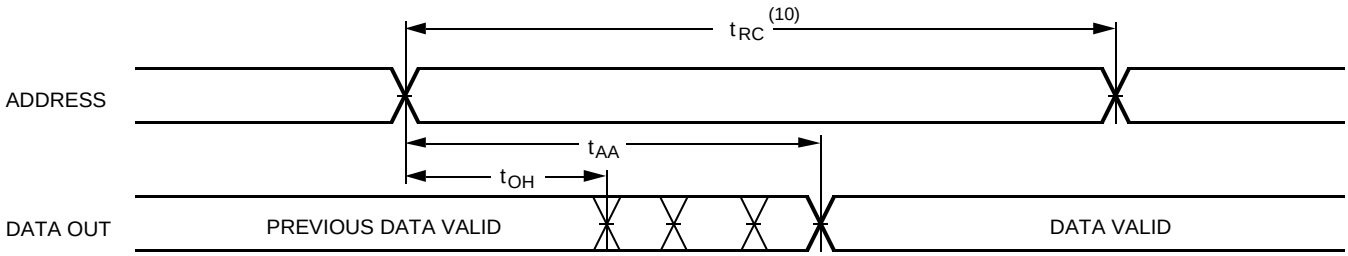
## READ CYCLE NO.1 (0 E controlled)[5]



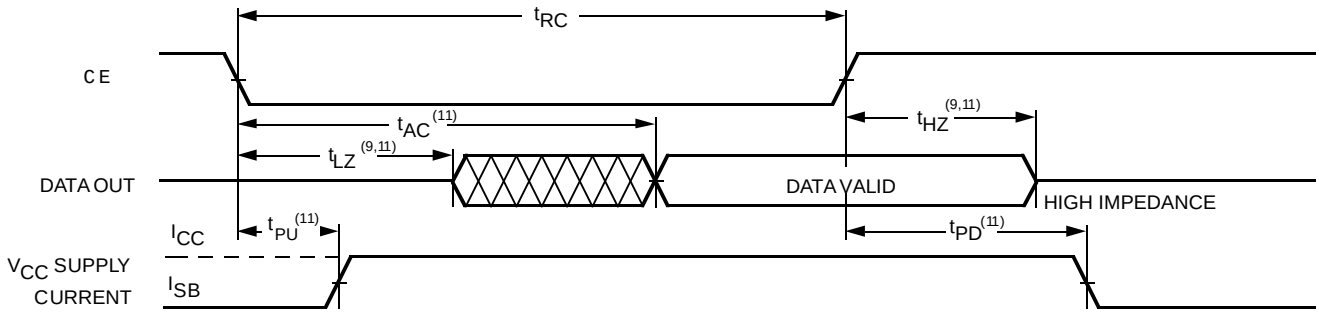

**Notes:**

5. WE is HIGH for READ cycle.

## READ CYCLE NO. 2 (ADDRESS Controlled)[5,6]




## READ CYCLE NO. 3 (CE[12] Controlled)[5,7,8]




**Notes:**

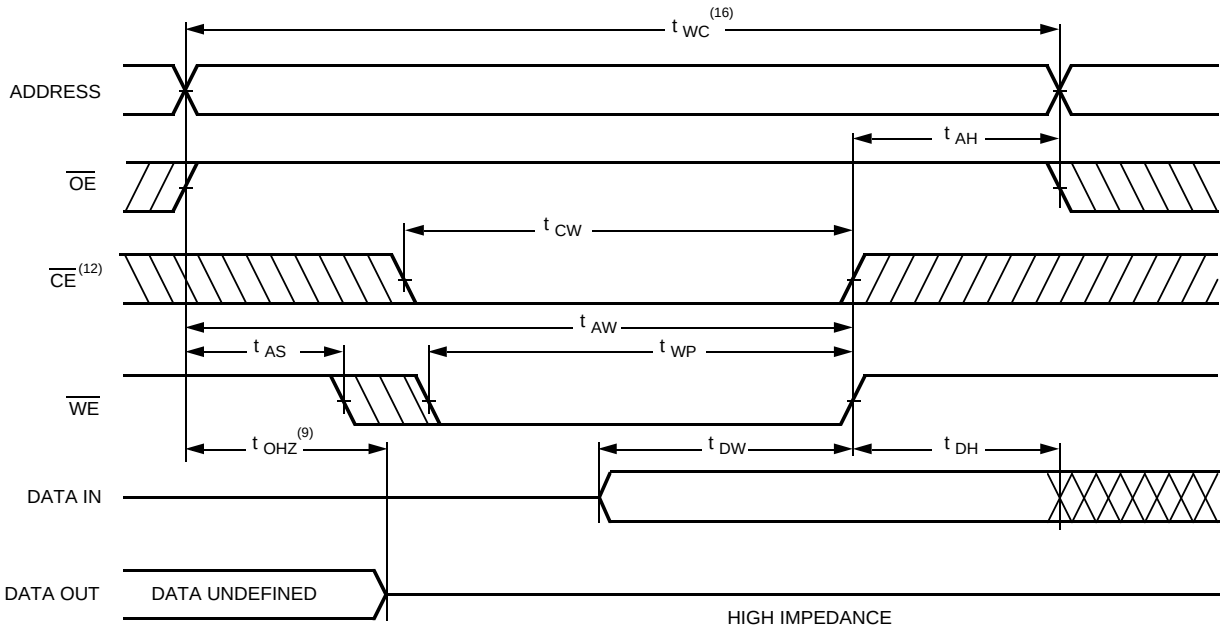
6. $\overline{CE}$ ($\overline{CE}_1$ $CE_2$ for P4C198A/L) and $\overline{OE}$ are LOW READ cycle.
7. $\overline{OE}$ is LOW for the cycle.
8. ADDRESS must be valid prior to, or coincident with $\overline{CE}$ ($\overline{CE}_1$ and $CE_2$ for P4C198A/L) transition LOW.
9. Transition is measured ± 200mV from steady state voltage prior to change, with loading as specified in Figure 1.
10. Read Cycle Time is measured from the last valid address to the first transitioning address.
11. Transitions caused by a chip enable control have similar delays irrespective of whether $\overline{CE}_1$ or $CE_2$ causes them (P4C198A/L).
12. $\overline{CE}_1$, $CE_2$ for P4C198A/L.

## AC CHARACTERISTICS—WRITE CYCLE

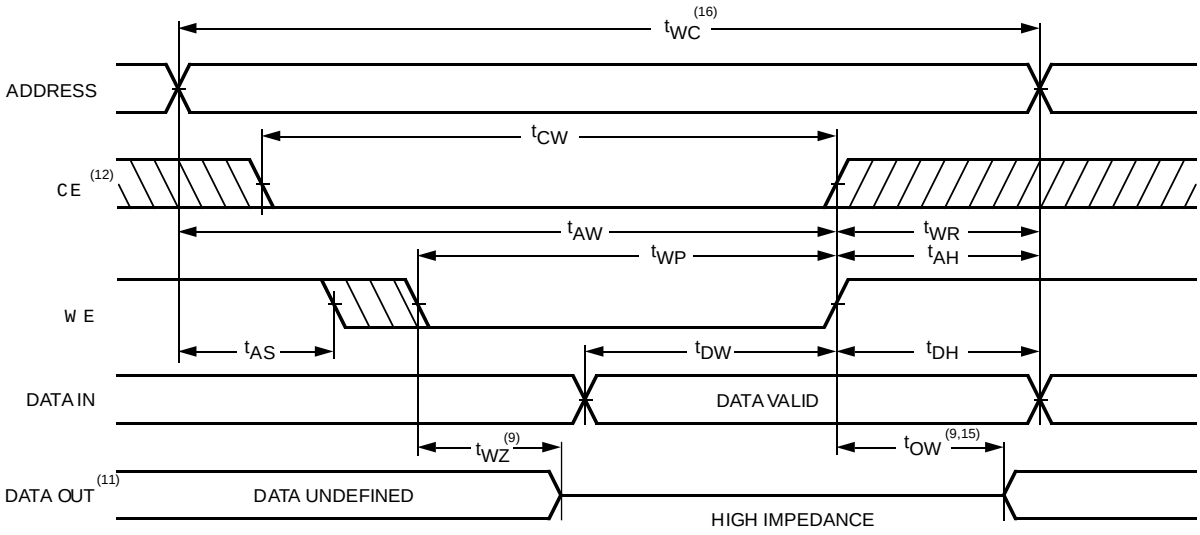
($V_{CC}$ = 5V ± 10%, All Temperature Ranges)[2]

| Sym. | Parameter | -10 | | -12 | | -15 | | -20 | | -25 | | -35 | | -45 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{WC}$ | Write Cycle Time | 10 | | 12 | | 13 | | 15 | | 20 | | 30 | | 40 | | ns |
| $t_{CW}$ | Chip Enable Time to End of Write | 7 | | 8 | | 10 | | 15 | | 20 | | 30 | | 35 | | ns |
| $t_{AW}$ | Address Valid to End of Write | 8 | | 8 | | 10 | | 15 | | 20 | | 25 | | 35 | | ns |
| $t_{AS}$ | Address Set-up Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WP}$ | Write Pulse Width | 8 | | 9 | | 10 | | 12 | | 20 | | 25 | | 35 | | ns |
| $t_{AH}$ | Address Hold Time from End of Write | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{DW}$ | Data Valid to End of Write | 7 | | 6 | | 7 | | 10 | | 13 | | 15 | | 20 | | ns |
| $t_{DH}$ | Data Hold Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WZ}$ | Write Enable to Output in High Z | | 7 | | 6 | | 7 | | 8 | | 10 | | 10 | | 15 | ns |
| $t_{OW}$ | Output Active from End of Write | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |

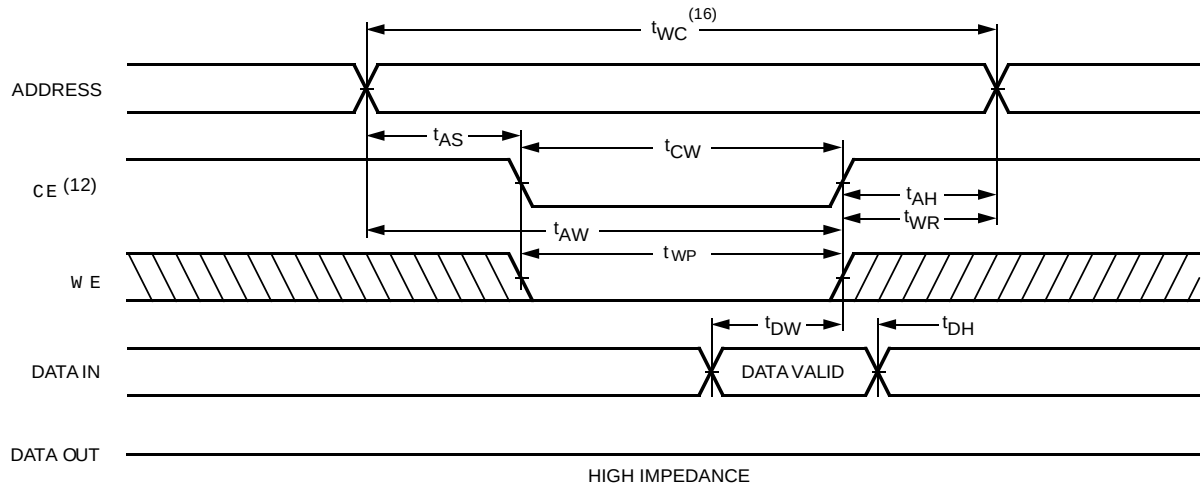
## WRITE CYCLE NO. 1 (With 0 E high)



## WRITE CYCLE NO. 2 (WE CONTROLLED)[13,14]




## WRITE CYCLE NO. 3 (CE[12] CONTROLLED)[13,14]




**Notes:**

13. CE (CE$_1$, CE$_2$ for P4C198A/L) and WE must be LOW for WRITE cycle.
14. OE is LOW for this WRITE cycle.
15. If CE (CE$_1$ or CE$_2$ for P4C198A/L) goes HIGH simultaneously with WE HIGH, the output remains in a high impedance state.
16. Write Cycle Time is measured from the last valid address to the first transitioning address.

## TRUTH TABLES

**P4C198/L**

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | Mode | Output |
|---|---|---|---|---|
| H | X | X | Standby | High Z |
| L | H | H | Output Inhibit | High Z |
| L | H | L | READ | $D_{OUT}$ |
| L | L | X | WRITE | $D_{IN}$ |

**P4C198A/L**

| $CE_1$ | $CE_2$ | $\overline{WE}$ | $\overline{OE}$ | Mode | Output |
|---|---|---|---|---|---|
| H | X | X | X | Standby | High Z |
| X | H | X | X | Standby | High Z |
| L | L | H | H | Output Inhibit | High Z |
| L | L | H | L | READ | $D_{OUT}$ |
| L | L | L | X | WRITE | $D_{IN}$ |

## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise and Fall Times | 3ns |
| Input Timing Reference Level | 1.5V |
| Output Timing Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

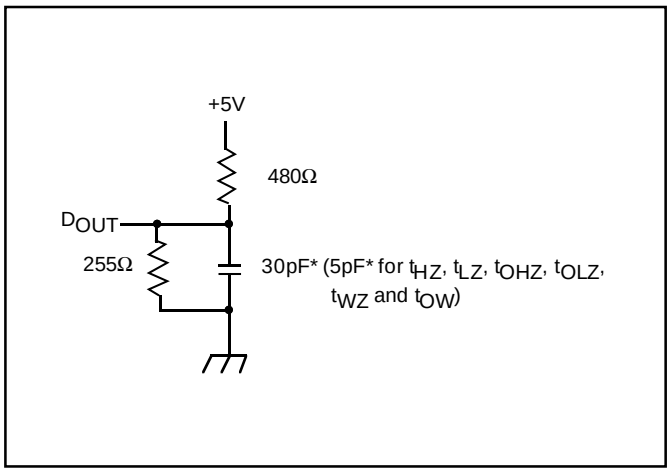



**Figure 1. Output Load**

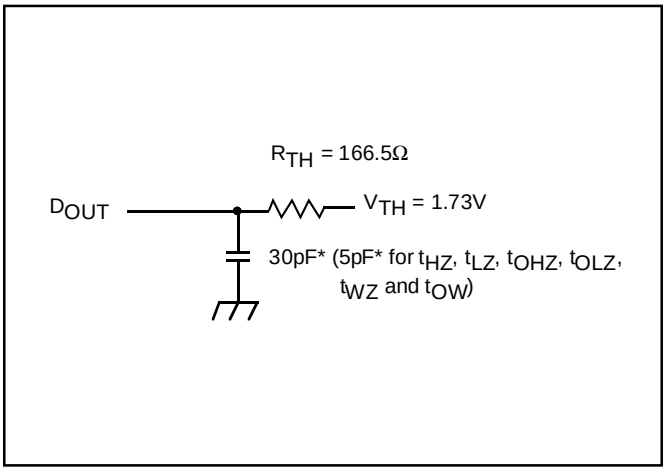



**Figure 2. Thevenin Equivalent**

* including scope and test fixture.

**Note:**
Because of the ultra-high speed of the P4C198/L and P4C198A/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the $V_{CC}$ and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between $V_{CC}$ and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with $D_{OUT}$ to match 166Ω (Thevenin Resistance).

## PACKAGE SUFFIX

| Package Suffix | Description |
|---|---|
| P | Plastic DIP, 300 mil wide standard |
| J | Plastic SOJ, 300 mil wide standard |
| L | Leadless Chip Carrier (ceramic) |
| D | CERDIP, 300 mil wide standard |

## TEMPERATURE RANGE SUFFIX

| Temperature Range Suffix | Description |
|---|---|
| C | Commercial Temperature Range, 0°C to +70°C. |
| I | Industrial Temperature Range –40°C to +85°C. |
| M | Military Temperature Range, –55°C to +125°C. |
| MB | Mil. Temp. with MIL-STD-883D Class B compliance |

## ORDERING INFORMATION

P4C 198
P4C 198A l — ss p t

- t — Temperature Range
- p — Package Code
- ss — Speed (Access/Cycle Time)
- l — Low Power Designator: Blank = None, L = Low Power
- 198 / 198A — Device Number
- P4C — Static RAM Prefix

l = Ultra-low standby power designator L, if needed.
ss = Speed (access/cycle time in ns), e.g., 25, 35
p = Package code, i.e., P, J, L, D.
t = Temperature range, i.e., C, M, MB.

The P4C198 and P4C198A are available to Standardized Military Drawings 5962-86859, 5962-89891 and 5962-89892.

## SELECTION GUIDE

The P4C198 and P4C198A are available in the following temperature, speed and package options.

| Temperature Range | Speed (ns) / Package | 10 | 12 | 15 | 20 | 25 | 35 | 45 |
|---|---|---|---|---|---|---|---|---|
| Commercial | Plastic DIP | –10PC | –12PC | –15PC | –20PC | –25PC | N/A | N/A |
| | Plastic SOJ (P4C198 Only) | –10JC | –12JC | –15JC | –20JC | –25JC | N/A | N/A |
| Industrial | Plastic DIP | N/A | –12PI | –15PI | –20PI | –25PI | –35PI | N/A |
| | Plastic SOJ (P4C198 Only) | N/A | –12JI | –15JI | –20JI | –25JI | –35JI | N/A |
| Military Temp. | CERDIP | N/A | N/A | –15DM | –20DM | –25DM | –35DM | –45DM |
| | LCC (P4C198 Only) | N/A | N/A | –15LM | –20LM | –25LM | –35LM | –45LM |
| Military Processed* | CERDIP | N/A | N/A | –15DMB | –20DMB | –25DMB | –35DMB | –45DMB |
| | LCC (P4C198 Only) | N/A | N/A | –15LMB | –20LMB | –25LMB | –35LMB | –45LMB |

* Military temperature range with MIL-STD-883, Class B processing.
N/A = Not available