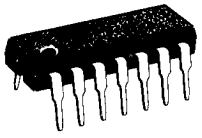
MN74HC74/MN74HC74S

Dual D-Type Flip-Flops with Preset and Clear

■ Description

MN74HC74/MN74HC74S contain two D-type flip-flop circuits with preset and clear. Each flip-flop has independent clear, preset, data, clock input and complementary Q and $\overline{Q}$ outputs. Input data is transferred to the output on the positive-going edge of the clock pulse. Preset and clear operate at low level regardless of the clock. Adoption of the silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to CMOS, and an operation speed of LS TTL. Each output can directly drive LS TTL 10-inputs. A resistor and diode are provided between the V_{DD} and V_{SS} to protect the input and output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



14-pin plastic DIL package

P-2

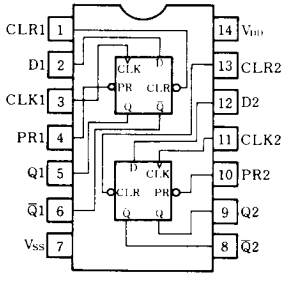
14-pin Panaflat package (SO-14D)

■ Truth table

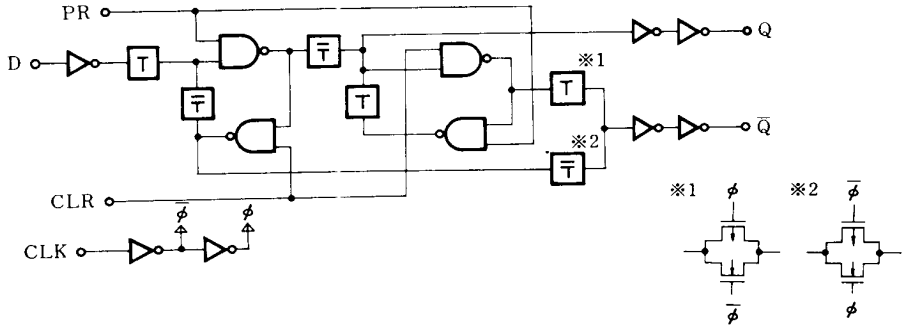
Input				Output	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	×	×	H	L
H	L	×	×	L	H
L	L	×	×	H*	H*
H	H	↗	H	H	L
H	H	↗	L	L	H
H	H	L	×	Q_0	$\overline{Q}_0$

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. ↗: Rise of positive direction
3. Q_0: Q level prior to determination of input condition shown in table
4. $\overline{Q}_0$: Q level prior to determination of input condition shown in table
5. H*: When preset and clear are low, Q and $\overline{Q}$ are HIGH; however, when preset and clear simultaneously change to HIGH, requirements of Q and $\overline{Q}$ cannot be predicted.

Pin configuration (top view)



■ Logic diagram (1 gate)



■ Absolute maximum ratings

Item			Sym.	Rating	Unit
Supply voltage			V_{DD}	−0.5～7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{DD}+0.5	V
Input current			I_I	±20	mA
Output current			I_O	±25	mA
Power dissipation	MN74HC74	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/℃	
	MN74HC74S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/℃	
Storage temperature range			T_{stg}	−65～+150	℃
Supply current			I_{DD}, I_{SS}	±50	mA

■ Recommended operating conditions

Item	Sym	Rating	Unit
Operating supply voltage	V_{DD}	1.4～6.0	V
Input voltage	V_I	0～V_{DD}	V
Operating temperature range	T_{opr}	−40～+85	℃
Input rise and fall time	t_r, t_f	0～500	ns

■ DC characteristics (V_{DD}=5V±10%, V_{SS}=0V)

Item	Sym.	Test conditions		Ta=−40℃		Ta=+25℃		Ta=+85℃		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
Quiescent supply current	I_{DD}	V_I=V_{DD} or V_{SS}			4		4		40	μA
High level input voltage	V_{IH}	V_O=V_{DD}−1.0V or 0.5V, $\|I_O\| \leq 1\mu A$	V_{DD}=4.5V	3.15		3.15		3.15		V
			V_{DD}=5.0V	3.50		3.50		3.50		
			V_{DD}=5.5V	3.85		3.85		3.85		
Low level input voltage	V_{IL}	V_O=V_{DD}−1.0V or 0.5V, $\|I_O\| \leq 1\mu A$	V_{DD}=4.5V		0.9		0.9		0.9	V
			V_{DD}=5.0V		1.0		1.0		1.0	
			V_{DD}=5.5V		1.1		1.1		1.1	
Input current	$\pm I_I$	V_I=V_{DD} or V_{SS}			0.3		0.3		1	μA
High level output voltage	V_{OH}	V_I=V_{DD} or V_{SS}, $\|I_O\| \leq 1\mu A$		V_{DD}−0.05		V_{DD}−0.05		V_{DD}−0.05		V
Low level output voltage	V_{OL}	V_I=V_{DD} or V_{SS}, $\|I_O\| \leq 1\mu A$			0.05		0.05		0.05	V
High level output current	I_{OH}	V_I=V_{DD} or V_{SS}, V_O=V_{DD}−0.8V		−6		−5		−4		mA
Low level output current	I_{OL}	V_I=V_{DD} or V_{SS}, V_O=0.4V		6		5		4		mA

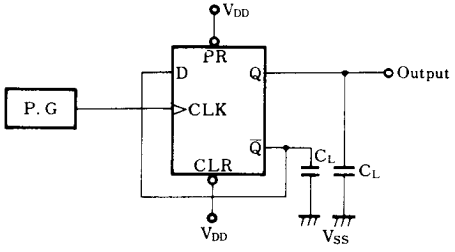
■ AC characteristics (V_{DD}=5V, V_{SS}=0V, Ta=25℃ Input transition time ≦6ns, C_L=50pF)

Item	Sym.	Test conditions	Min.	Typ.	Max.	Unit
Output rise time	t_{TLH}			8	15	ns
Output fall time	t_{THL}			6	15	ns
Minimum data set-up time	t_{su}				20	ns
Maximum clock frequency	f_{max}		30	60		MHz
Propagation time (L→H) CLK→Q,$\bar{Q}$	t_{PLH}			14	25	ns
Propagation time (H→L) CLK→Q,$\bar{Q}$	t_{PHL}			13	25	ns
Propagation time (L→H) PR,CLR→Q,$\bar{Q}$	t_{PLH}			15	25	ns
Propagation time (H→L) PR,CLR→Q,$\bar{Q}$	t_{PHL}			14	25	ns
Minimum clear pulse width	t_{WCD}				25	ns
Minimum preset pulse width	t_{WPD}				25	ns

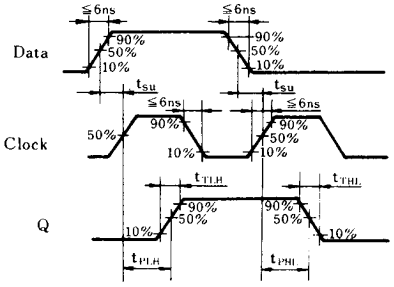
※ Switching time measurement circuit and waveform

〔1〕 t_{TLH}, t_{THL}, t_{su}, f_{max}, t_{PLH}/t_{PHL} (CLK→Q, $\overline{Q}$)

1. Measurement circuit

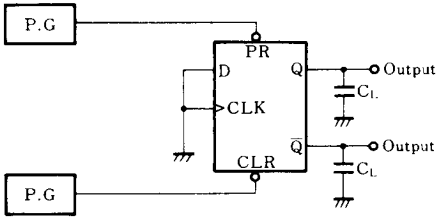


2. Waveforms



〔2〕 t_{PLH}/t_{PHL} (PR, CLR→Q, $\overline{Q}$), t_{WCD}, t_{WPD}

1. Measurement circuit



2. Waveforms