74LV4051

8-channel analog multiplexer/demultiplexer

Rev. 9 — 29 March 2024 | Product data sheet

1. General description

The 74LV4051 is an 8-channel analog multiplexer/demultiplexer with three digital select inputs (S0 to S2), an active-LOW enable input ($\overline{E}$), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z). It is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC4051 and 74HCT4051. With $\overline{E}$ LOW, one of the eight switches is selected (low impedance ON-state) by S0 to S2. With $\overline{E}$ HIGH, all switches are in the high-impedance OFF-state, independent of S0 to S2.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S0 to S2, and $\overline{E}$). The V_{CC} to GND ranges are 1.0 V to 6.0 V. The analog inputs/outputs (Y0 to Y7, and Z) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. V_{CC} - V_{EE} may not exceed 6.0 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

2. Features and benefits

- Optimized for low-voltage applications: 1.0 V to 6.0 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Low ON resistance:
  - 145 Ω (typical) at V_{CC} - V_{EE} = 2.0 V
  - 80 Ω (typical) at V_{CC} - V_{EE} = 3.0 V
  - 60 Ω (typical) at V_{CC} - V_{EE} = 4.5 V
- Logic level translation:
  - To enable 3 V logic to communicate with ±3 V analog signals
- Typical ‘break before make’ built in
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV4051D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV4051PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LV4051BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

nexperia

4. Functional diagram

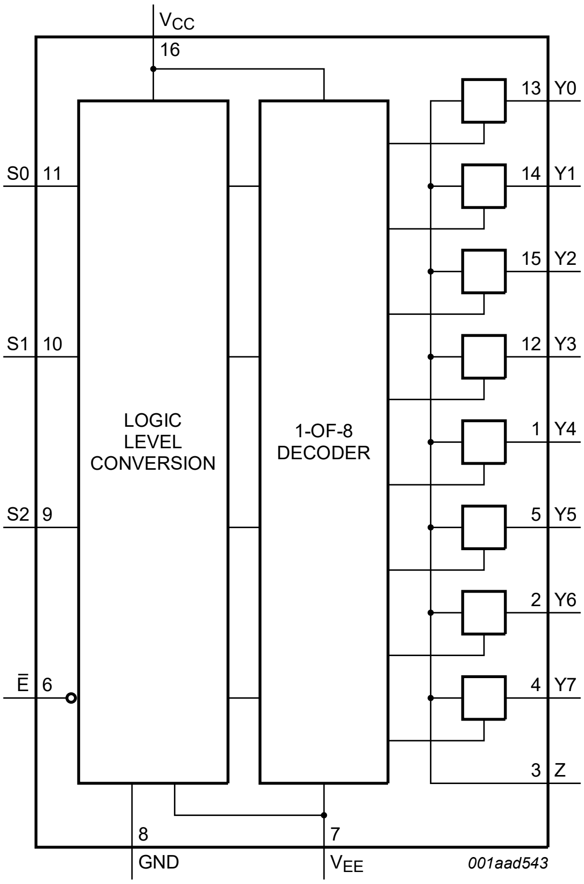


Fig. 1. Functional diagram

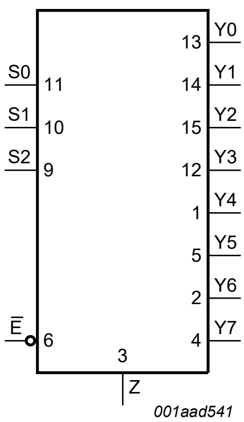


Fig. 2. Logic symbol

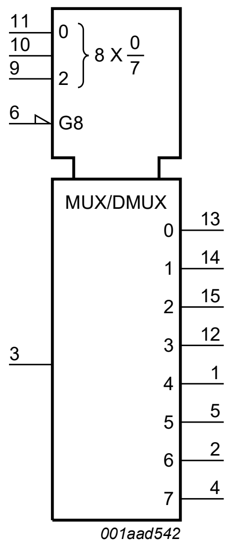


Fig. 3. IEC logic symbol

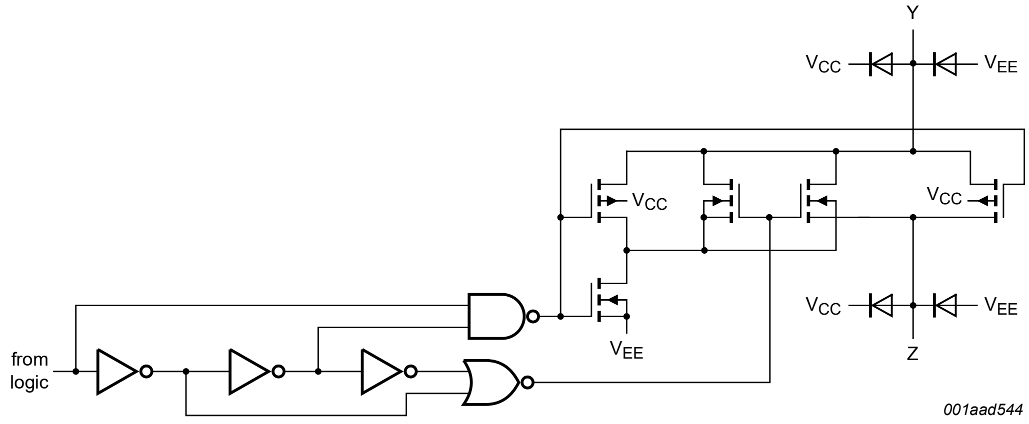
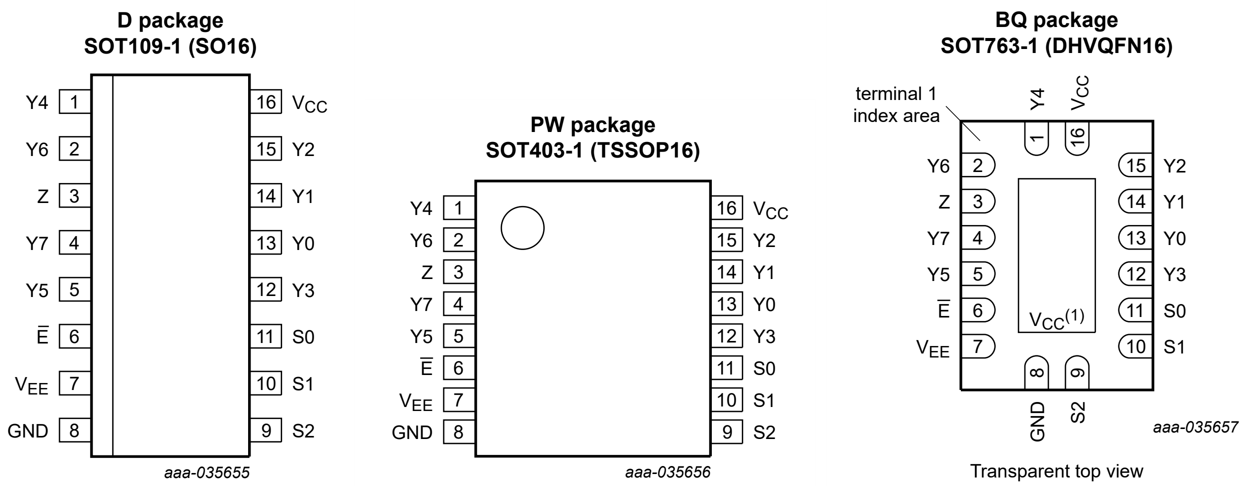


Fig. 4. Schematic diagram (one switch)

5. Pinning information

5.1. Pinning



(1) This is not a supply pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to V_{CC}.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{E}$	6	enable input (active LOW)
V_{EE}	7	supply voltage
GND	8	ground supply voltage
S0, S1, S2	11, 10, 9	select input
Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7	13, 14, 15, 12, 1, 5, 2, 4	independent input or output
Z	3	common output or input
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input				Channel ON
$\overline{E}$	S2	S1	S0	
L	L	L	L	Y0 to Z
L	L	L	H	Y1 to Z
L	L	H	L	Y2 to Z
L	L	H	H	Y3 to Z
L	H	L	L	Y4 to Z
L	H	L	H	Y5 to Z
L	H	H	L	Y6 to Z
L	H	H	H	Y7 to Z
H	X	X	X	switches off

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND = 0 V.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage		[1]	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[2]	-	±20	mA
I_{SK}	switch clamping current	$V_{SW} < -0.5$ V or $V_{SW} > V_{CC} + 0.5$ V	[2]	-	±20	mA
I_{SW}	switch current	$V_{SW} > -0.5$ V or $V_{SW} < V_{CC} + 0.5$ V; source or sink current	[2]	-	±25	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[3]	-	500	mW

[1] To avoid drawing V_{CC} current out of terminal Z, when switch current flows into terminals Yn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminals Yn, and in this case there is no limit for the voltage drop across the switch, but the voltages at Yn and Z may not exceed V_{CC} or V_{EE}.

[2] The minimum input voltage rating may be exceeded if the input current rating is observed.

[3] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	see Fig. 5 [1]	1	3.3	6	V
V_I	input voltage		0	-	V_{CC}	V
V_{SW}	switch voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 1.0 V to 2.0 V	-	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V	-	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V	-	-	100	ns/V

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to 6.0 V, but LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

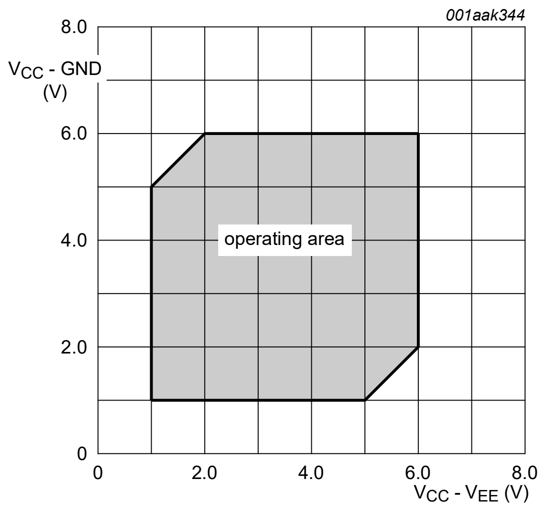


Fig. 5. Guaranteed operating area as a function of the supply voltages

9. Static characteristics

Table 6. Static characteristics

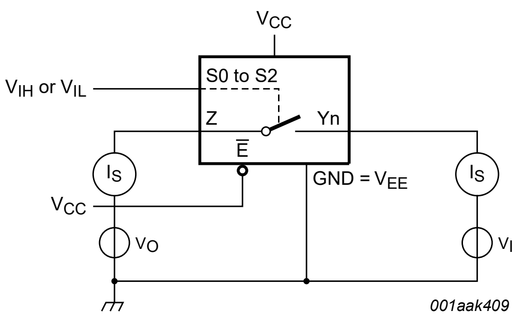
At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V_{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V_{CC} = 4.5 V	3.15	-	-	3.15	-	V
		V_{CC} = 6.0 V	4.20	-	-	4.20	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V_{CC} = 4.5 V	-	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.80	-	1.80	V

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I_I	input leakage current	$V_I = V_{CC}$ or GND						
		$V_{CC} = 3.6$ V	-	-	1.0	-	1.0	μA
		$V_{CC} = 6.0$ V	-	-	2.0	-	2.0	μA
$I_{S(OFF)}$	OFF-state leakage current	$V_I = V_{IH}$ or V_{IL}; see Fig. 6						
		$V_{CC} = 3.6$ V	-	-	1.0	-	1.0	μA
		$V_{CC} = 6.0$ V	-	-	2.0	-	2.0	μA
$I_{S(ON)}$	ON-state leakage current	$V_I = V_{IH}$ or V_{IL}; see Fig. 7						
		$V_{CC} = 3.6$ V	-	-	1.0	-	1.0	μA
		$V_{CC} = 6.0$ V	-	-	2.0	-	2.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A						
		$V_{CC} = 3.6$ V	-	-	20	-	40	μA
		$V_{CC} = 6.0$ V	-	-	40	-	80	μA
ΔI_{CC}	additional supply current	per input; $V_I = V_{CC} - 0.6$ V; $V_{CC} = 2.7$ V to 3.6 V	-	-	500	-	850	μA
C_I	input capacitance		-	3.5	-	-	-	pF
C_{sw}	switch capacitance	independent pins Yn	-	5	-	-	-	pF
		common pin Z	-	25	-	-	-	pF

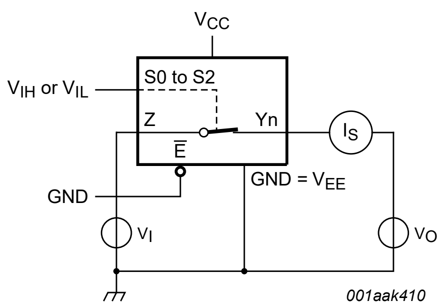
[1] Typical values are measured at $T_{amb} = 25$ °C.

9.1. Test circuits



$V_I = V_{CC}$ or V_{EE} and $V_O = V_{EE}$ or V_{CC}.

Fig. 6. Test circuit for measuring OFF-state leakage current



$V_I = V_{CC}$ or V_{EE} and V_O = open circuit.

Fig. 7. Test circuit for measuring ON-state leakage current

9.2. ON resistance

Table 7. ON resistance

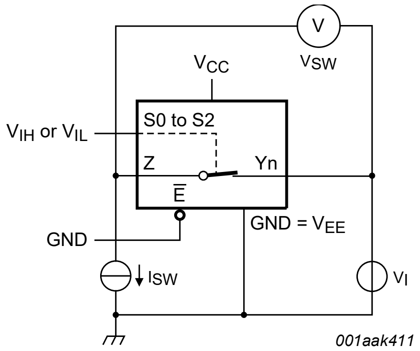
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit and graph see Fig. 8 and Fig. 9.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	V_I = 0 V to V_{CC} - V_{EE}						
		V_{CC} = 1.2 V; I_{SW} = 100 μA [2]	-	-	-	-	-	Ω
		V_{CC} = 2.0 V; I_{SW} = 1000 μA	-	145	325	-	375	Ω
		V_{CC} = 2.7 V; I_{SW} = 1000 μA	-	90	200	-	235	Ω
		V_{CC} = 3.0 V to 3.6 V; I_{SW} = 1000 μA	-	80	180	-	210	Ω
		V_{CC} = 4.5 V; I_{SW} = 1000 μA	-	60	135	-	160	Ω
		V_{CC} = 6.0 V; I_{SW} = 1000 μA	-	55	125	-	145	Ω
ΔR_{ON}	ON resistance mismatch between channels	V_I = 0 V to V_{CC} - V_{EE}						
		V_{CC} = 1.2 V; I_{SW} = 100 μA [2]	-	-	-	-	-	Ω
		V_{CC} = 2.0 V; I_{SW} = 1000 μA	-	5	-	-	-	Ω
		V_{CC} = 2.7 V; I_{SW} = 1000 μA	-	4	-	-	-	Ω
		V_{CC} = 3.0 V to 3.6 V; I_{SW} = 1000 μA	-	4	-	-	-	Ω
		V_{CC} = 4.5 V; I_{SW} = 1000 μA	-	3	-	-	-	Ω
		V_{CC} = 6.0 V; I_{SW} = 1000 μA	-	2	-	-	-	Ω
$R_{ON(rail)}$	ON resistance (rail)	V_I = GND						
		V_{CC} = 1.2 V; I_{SW} = 100 μA [2]	-	225	-	-	-	Ω
		V_{CC} = 2.0 V; I_{SW} = 1000 μA	-	110	235	-	270	Ω
		V_{CC} = 2.7 V; I_{SW} = 1000 μA	-	70	145	-	165	Ω
		V_{CC} = 3.0 V to 3.6 V; I_{SW} = 1000 μA	-	60	130	-	150	Ω
		V_{CC} = 4.5 V; I_{SW} = 1000 μA	-	45	100	-	115	Ω
		V_{CC} = 6.0 V; I_{SW} = 1000 μA	-	40	85	-	100	Ω
$R_{ON(rail)}$	ON resistance (rail)	V_I = V_{CC} - V_{EE}						
		V_{CC} = 1.2 V; I_{SW} = 100 μA [2]	-	250	-	-	-	Ω
		V_{CC} = 2.0 V; I_{SW} = 1000 μA	-	120	320	-	370	Ω
		V_{CC} = 2.7 V; I_{SW} = 1000 μA	-	75	195	-	225	Ω
		V_{CC} = 3.0 V to 3.6 V; I_{SW} = 1000 μA	-	70	175	-	205	Ω
		V_{CC} = 4.5 V; I_{SW} = 1000 μA	-	50	130	-	150	Ω
		V_{CC} = 6.0 V; I_{SW} = 1000 μA	-	45	120	-	135	Ω

[1] All typical values are measured at nominal V_{CC} and at T_{amb} = 25 °C.

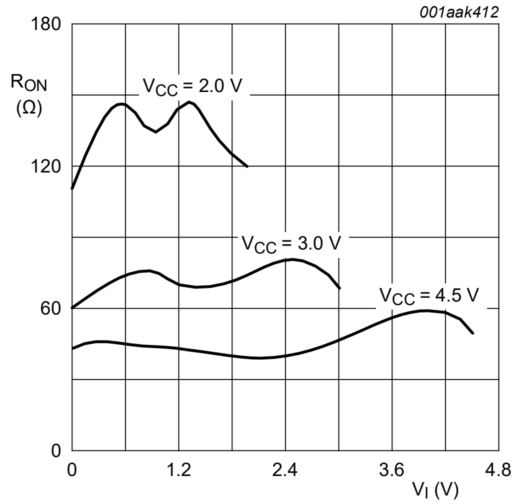
[2] When supply voltages (V_{CC} - V_{EE}) near 1.2 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 1.2 V, it is recommended to use these devices only for transmitting digital signals.

9.3. On resistance test circuit and graph



$R_{ON} = V_{SW} / I_{SW}$.

Fig. 8. Test circuit for measuring R_{ON}



V_I = 0 V to V_{CC} - V_{EE}

Fig. 9. Typical R_{ON} as a function of input voltage

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (GND = V_{EE} = 0 V). For test circuit see Fig. 12.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	Yn to Z, Z to Yn; see Fig. 10 [2]						
		V_{CC} = 1.2 V	-	25	-	-	-	ns
		V_{CC} = 2.0 V	-	9	17	-	20	ns
		V_{CC} = 2.7 V	-	6	13	-	15	ns
		V_{CC} = 3.0 V to 3.6 V	-	5	10	-	12	ns
		V_{CC} = 4.5 V	-	4	9	-	10	ns
		V_{CC} = 6.0 V	-	3	8	-	8	ns

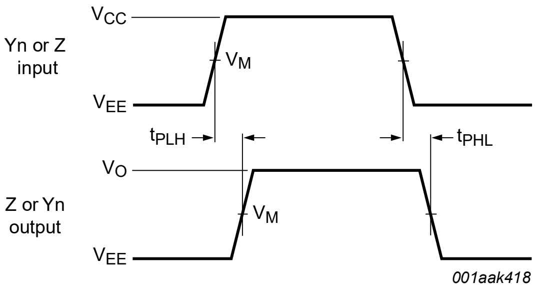
Symbol	Parameter	Conditions		-40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ [1]	Max	Min	Max	
t_{en}	enable time	$\overline{E}$ to Yn, Z; see Fig. 11	[2]						
		V_{CC} = 1.2 V		-	145	-	-	-	ns
		V_{CC} = 2.0 V		-	49	94	-	112	ns
		V_{CC} = 2.7 V		-	36	69	-	83	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF		-	23	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		-	28	55	-	66	ns
		V_{CC} = 4.5 V		-	25	47	-	56	ns
		V_{CC} = 6.0 V		-	19	38	-	43	ns
		Sn to Yn; see Fig. 11	[2]						
		V_{CC} = 1.2 V		-	140	-	-	-	ns
		V_{CC} = 2.0 V		-	48	90	-	107	ns
		V_{CC} = 2.7 V		-	35	66	-	79	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF		-	22	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		-	27	53	-	63	ns
		V_{CC} = 4.5 V		-	24	45	-	54	ns
		V_{CC} = 6.0 V		-	18	34	-	41	ns
t_{dis}	disable time	$\overline{E}$ to Yn, Z; see Fig. 11	[2]						
		V_{CC} = 1.2 V		-	145	-	-	-	ns
		V_{CC} = 2.0 V		-	51	93	-	110	ns
		V_{CC} = 2.7 V		-	38	69	-	82	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF		-	25	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		-	30	56	-	66	ns
		V_{CC} = 4.5 V		-	29	48	-	56	ns
		V_{CC} = 6.0 V		-	21	37	-	44	ns
		Sn to Yn; see Fig. 11	[2]						
		V_{CC} = 1.2 V		-	115	-	-	-	ns
		V_{CC} = 2.0 V		-	41	73	-	90	ns
		V_{CC} = 2.7 V		-	31	54	-	67	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF		-	20	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		-	24	44	-	54	ns
		V_{CC} = 4.5 V		-	22	37	-	46	ns
		V_{CC} = 6.0 V		-	17	29	-	36	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC}	[3]	-	25	-	-	-	pF

[1] All typical values are measured at nominal V_{CC} and at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma((C_L + C_{SW}) \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz, f_o = output frequency in MHz
C_L = output load capacitance in pF
C_{SW} = maximum switch capacitance in pF;
V_{CC} = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

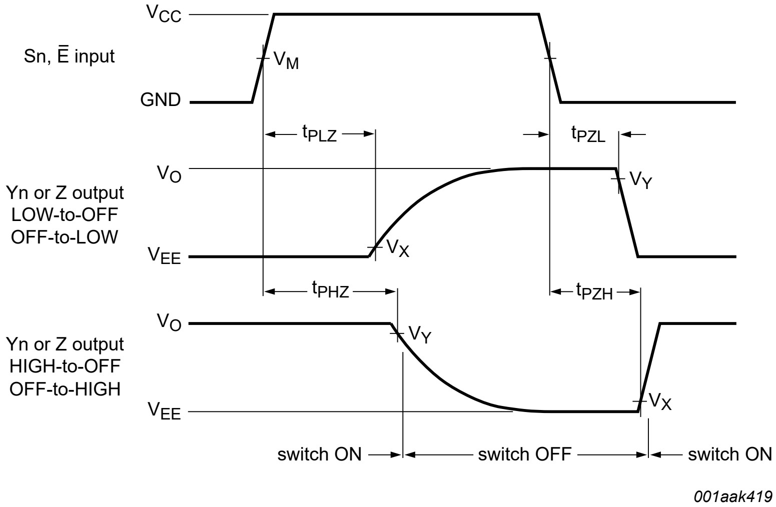
10.1. Waveforms and test circuit



Measurement points are given in Table 9.

V_{EE} and V_O are typical voltage output levels that occur with the output load.

Fig. 10. Propagation delay input (Yn or Z) to output (Z or Yn)



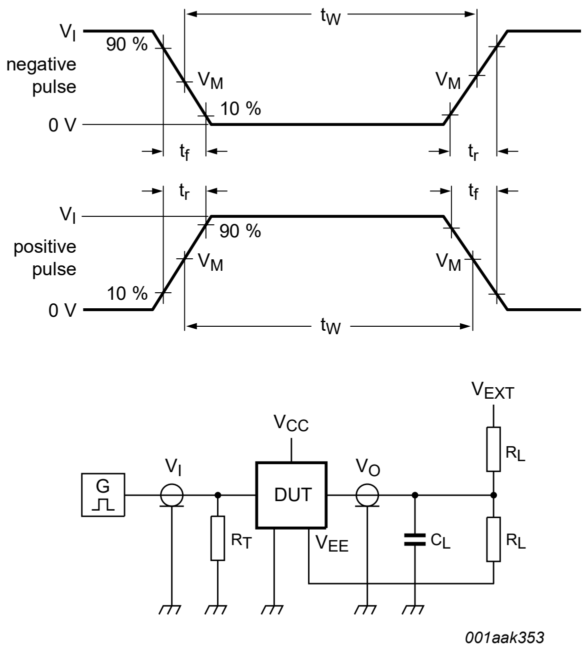
Measurement points are given in Table 9.

V_{EE} and V_O are typical voltage output levels that occur with the output load.

Fig. 11. Enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{EE} + $0.1V_{CC}$	V_O - $0.1V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V	V_{EE} + 0.3 V	V_O - 0.3 V
> 3.6 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{EE} + $0.1V_{CC}$	V_O - $0.1V_{CC}$



Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 12. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
< 2.7 V	V_{CC}	≤ 6 ns	50 pF	1 kΩ	open	V_{EE}	$2V_{CC}$
2.7 V to 3.6 V	2.7 V	≤ 6 ns	15 pF, 50 pF	1 kΩ	open	V_{EE}	$2V_{CC}$
> 3.6 V	V_{CC}	≤ 6 ns	50 pF	1 kΩ	open	V_{EE}	$2V_{CC}$

10.2. Additional dynamic parameters

Table 11. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);
V_I = GND or V_{CC} (unless otherwise specified); t_r = t_f ≤ 6.0 ns; T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	f_i = 1 kHz; C_L = 50 pF; R_L = 10 kΩ; see Fig. 17				
		V_{CC} = 3.0 V; V_I = 2.75 V (p-p)	-	0.8	-	%
		V_{CC} = 6.0 V; V_I = 5.5 V (p-p)	-	0.4	-	%
		f_i = 10 kHz; C_L = 50 pF; R_L = 10 kΩ; see Fig. 17				
		V_{CC} = 3.0 V; V_I = 2.75 V (p-p)	-	2.4	-	%
		V_{CC} = 6.0 V; V_I = 5.5 V (p-p)	-	1.2	-	%
$f_{(-3dB)}$	-3 dB frequency response	C_L = 50 pF; R_L = 50 Ω; see Fig. 13 [1]				
		V_{CC} = 3.0 V	-	180	-	MHz
		V_{CC} = 6.0 V	-	200	-	MHz
$α_{iso}$	isolation (OFF-state)	f_i = 1 MHz; C_L = 50 pF; R_L = 600 Ω; see Fig. 15 [2]				
		V_{CC} = 3.0 V	-	-50	-	dB
		V_{CC} = 6.0 V	-	-50	-	dB
V_{ct}	crosstalk voltage	between digital inputs and switch; f_i = 1 MHz; C_L = 50 pF; R_L = 600 Ω; see Fig. 18 [2]				
		V_{CC} = 3.0 V	-	0.11	-	V
		V_{CC} = 6.0 V	-	0.12	-	V
Xtalk	crosstalk	between switches; f_i = 1 MHz; C_L = 50 pF; R_L = 600 Ω; see Fig. 19				
		V_{CC} = 3.0 V	-	-60	-	dB
		V_{CC} = 6.0 V	-	-60	-	dB

[1] Adjust f_i voltage to obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 50 Ω).
[2] Adjust f_i voltage to obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 600 Ω).

10.3. Test circuits

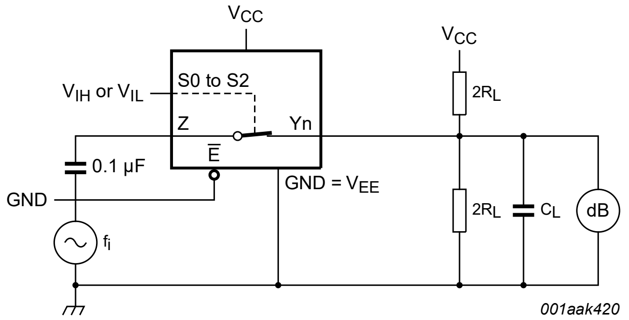
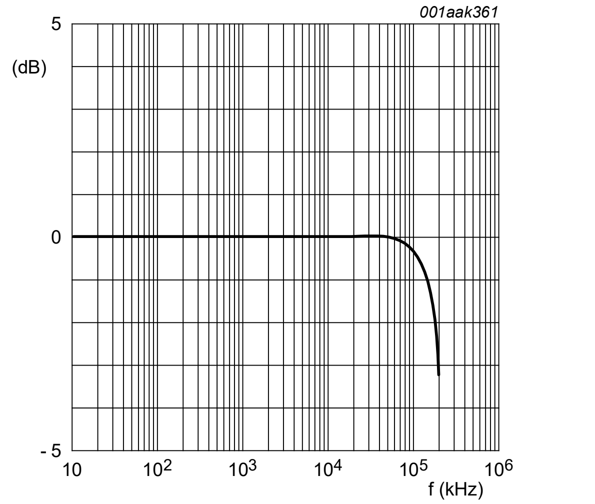


Fig. 13. Test circuit for measuring frequency response



V_{CC} = 3.0 V; GND = 0 V; V_{EE} = -3.0 V; R_L = 50 Ω; R_{SOURCE} = 1 kΩ.

Fig. 14. Typical frequency response

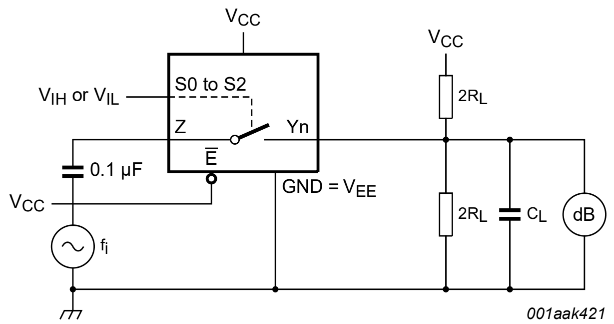
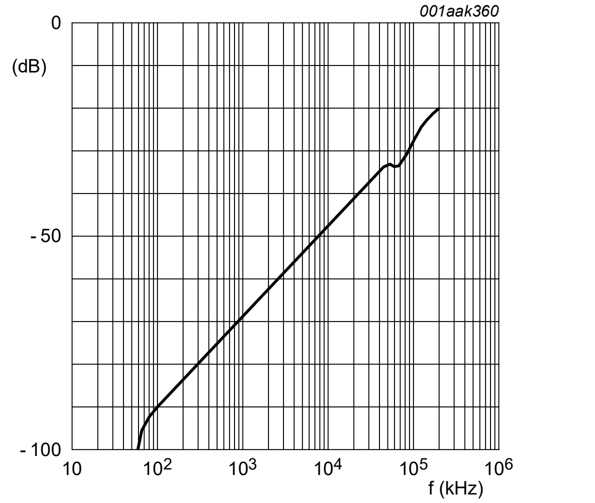


Fig. 15. Test circuit for measuring isolation (OFF-state)



V_{CC} = 3.0 V; GND = 0 V; V_{EE} = -3.0 V; R_L = 50 Ω; R_{SOURCE} = 1 kΩ.

Fig. 16. Typical isolation (OFF-state) as function of frequency

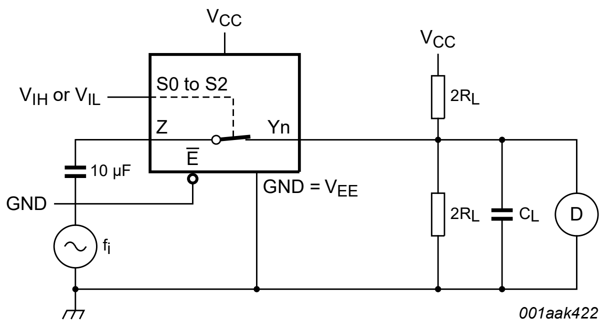
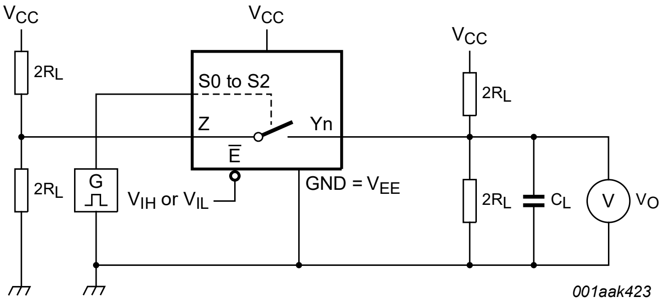
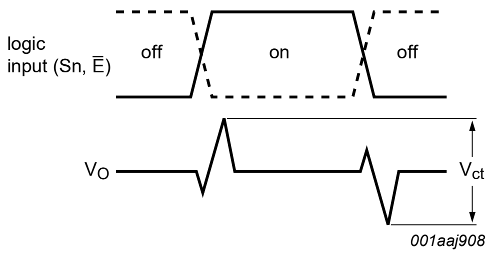


Fig. 17. Test circuit for measuring total harmonic distortion



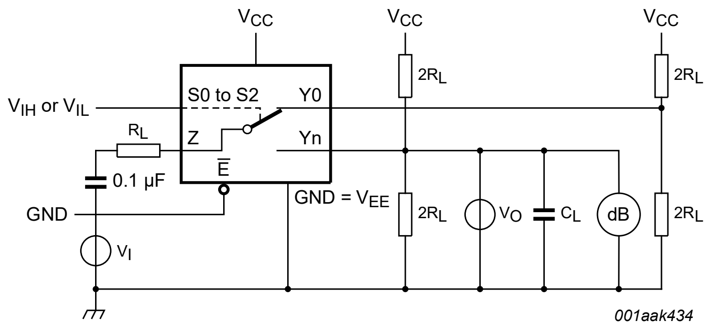
a. Test circuit



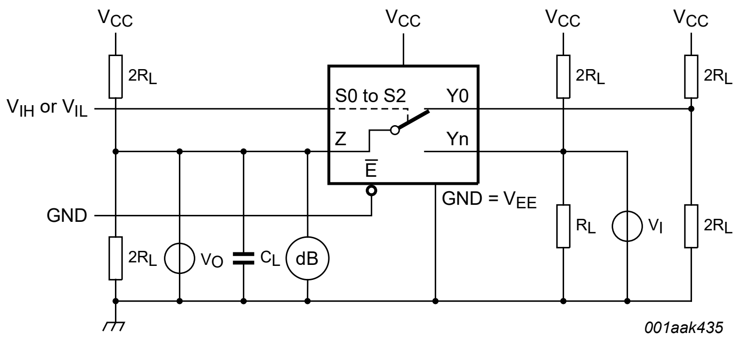
b. Input and output pulse definitions

V_I may be connected to Sn or $\overline{E}$.

Fig. 18. Test circuit for measuring crosstalk voltage between digital inputs and switch



a. Switch closed condition

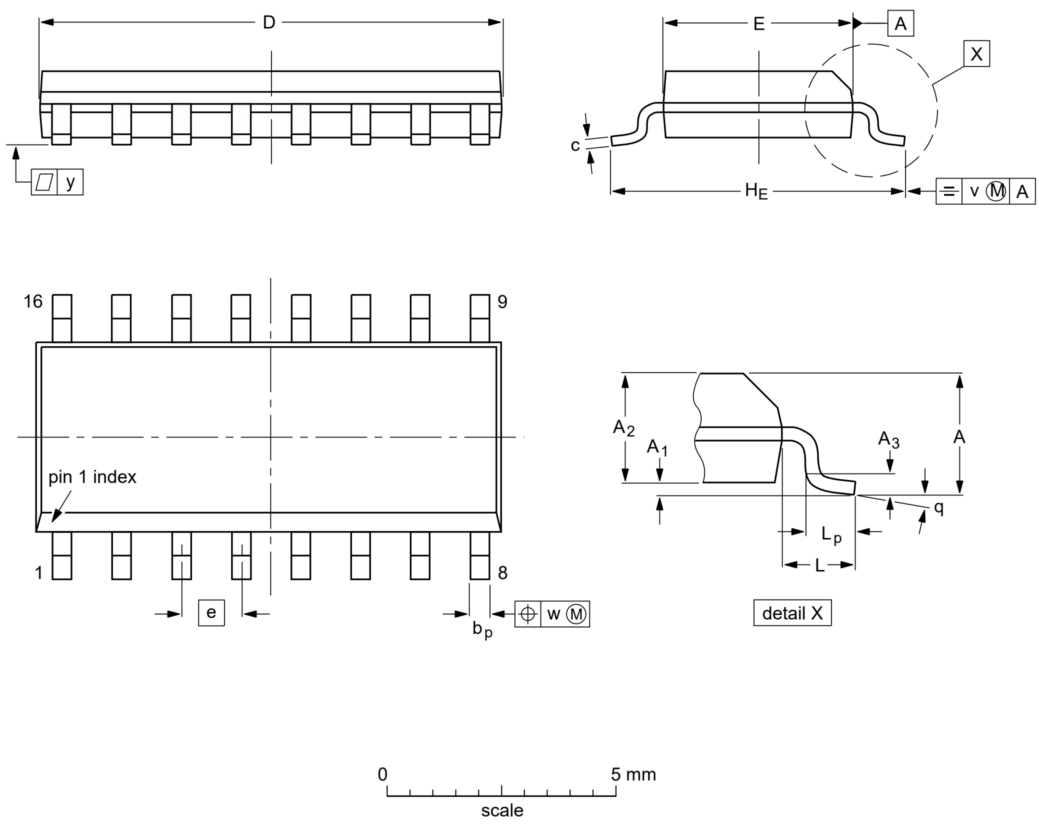


b. Switch open condition

Fig. 19. Test circuit for measuring crosstalk between switches

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

Note

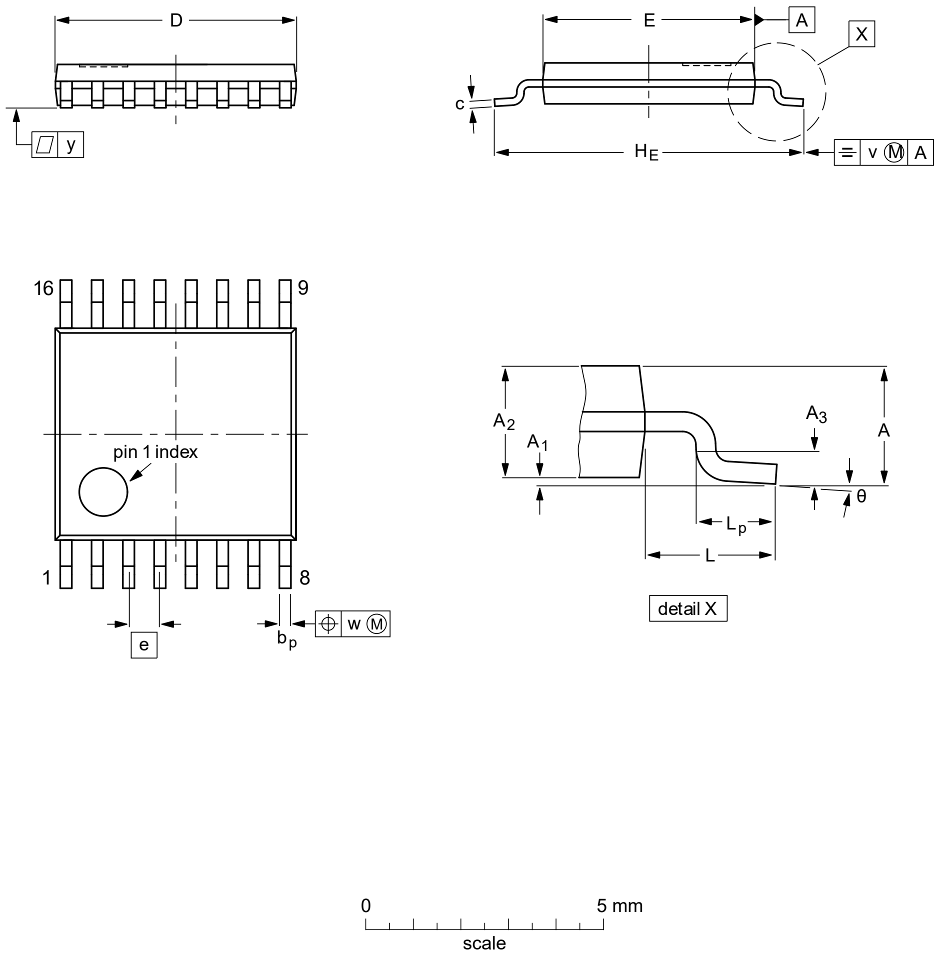
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 20. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

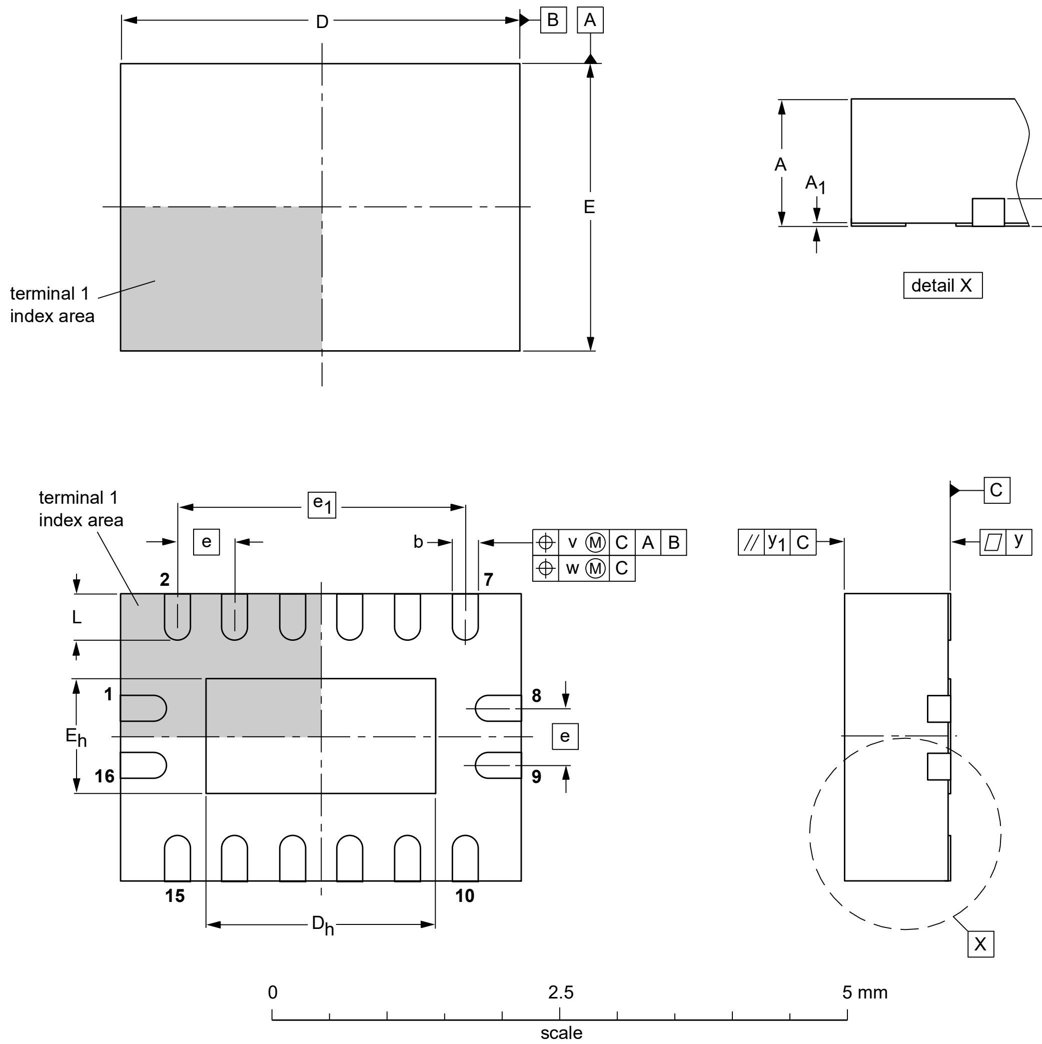
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 21. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig. 22. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV4051 v.9	20240329	Product data sheet	-	74LV4051 v.8
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 20 and Fig. 21: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74LV4051 v.8	20210716	Product data sheet	-	74LV4051 v.7
Modifications:	• Type number 74LV4051DB (SOT338-1/SSOP16) removed. • Section 7: Derating values for P_{tot} total power dissipation updated.			
74LV4051 v.7	20181009	Product data sheet	-	74LV4051 v.6
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74LV4051 v.6	20160317	Product data sheet	-	74LV4051 v.5
Modifications:	• Type number 74LV4051N (SOT38-4) removed.			
74LV4051 v.5	20140917	Product data sheet	-	74LV4051 v.4
Modifications:	• #unique_6/unique_6_Connect_42_image_nz2_pj2_x1c: Figure note added for DHVQFN16 package			
74LV4051 v.4	20090810	Product data sheet	-	74LV4051 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Added type number 74LV4051BQ (DHVQFN16 package)			
74LV4051 v.3	19960623	Product specification	-	74LV4051 v.2
74LV4051 v.2	19970715	Product specification	-	74LV4051 v.1

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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