FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LV32 a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT32.

The 74LV32 provides the 2-input OR function.

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF V_{CC} = 3.3 V	6	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	16	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV32N	14	DIL	plastic	DIL14/SOT27
74LV32D	14	SO	plastic	SO14/SOT108A
74LV32DB	14	SSOP	plastic	SSOP14/SOT337
74LV32PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

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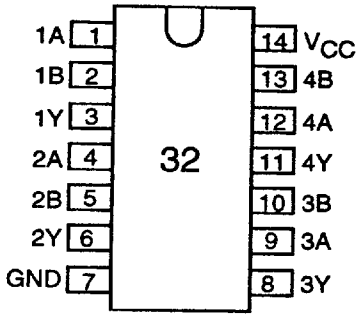

Fig.1 Pin configuration.

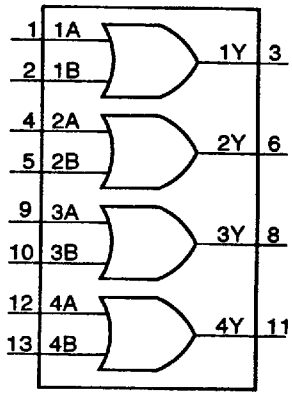

Fig.2 Logic symbol.

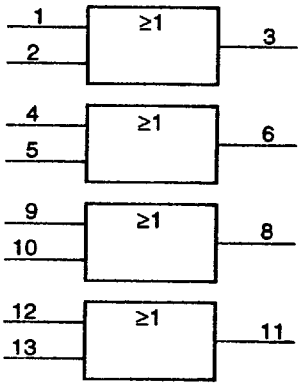

Fig.3 IEC Logic symbol.

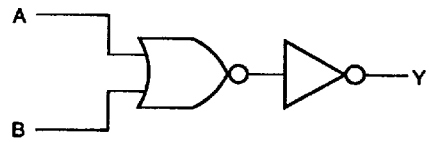

Fig.4 Logic diagram (one gate).

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DC CHARACTERISTICS FOR 74LV32

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74LV32

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	–	40	–	–	–	ns	1.2	Fig.5
		–	14	29	–	34		2.0	
		–	10	22	–	25		2.7	
		–	8*	17	–	20		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

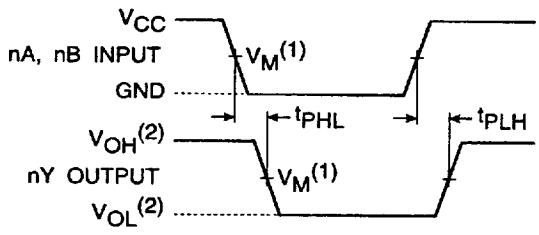

Fig. 5 Waveforms showing the input (nA, nB) to output (nY) propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

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