

FEATURES

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

DESCRIPTION

This 18-bit buffer and line driver is designed for 1.65-V to 3.6-V V_{CC} operation.

This SN74ALVCH16825 improves the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as two 9-bit buffers or one 18-bit buffer. It provides true data.

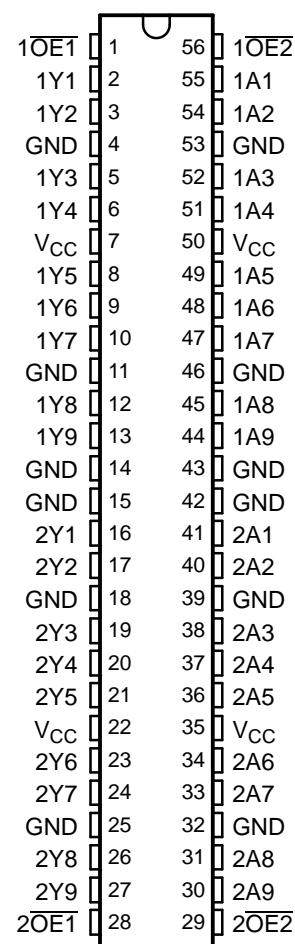
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all nine affected outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH16825 is characterized for operation from -40°C to 85°C.

DGG OR DL PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each 9-bit section)

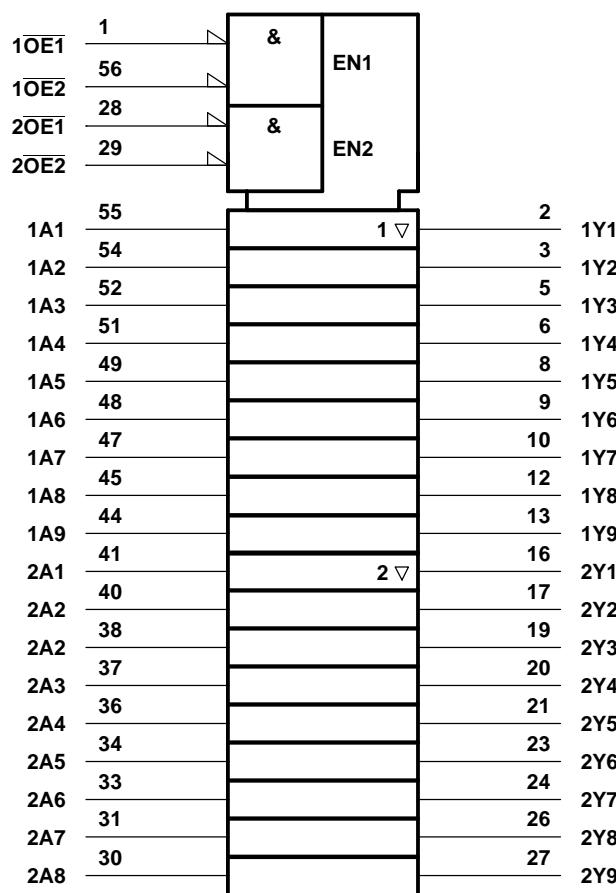
INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

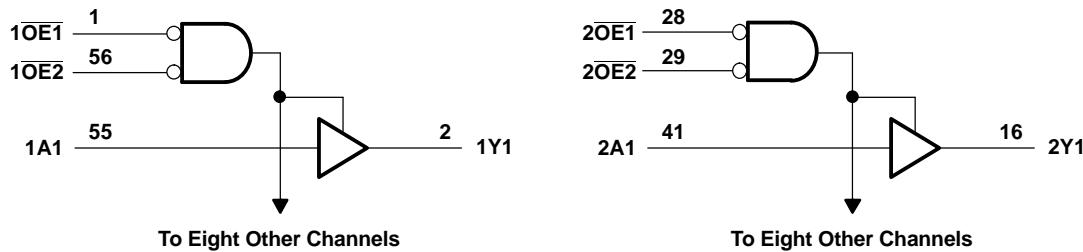
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LOGIC SYMBOL⁽¹⁾



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	4.6	V
V _I	Input voltage range ⁽²⁾	-0.5	4.6	V
V _O	Output voltage range ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current V _I < 0		-50	mA
I _{OK}	Output clamp current V _O < 0		-50	mA
I _O	Continuous output current		±50	mA
	Continuous current through each V _{CC} or GND		±100	mA
θ _{JA}	DGG package		81	°C/W
	DL package		74	
T _{stg}	Storage temperature range	-65	150	°C

- Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- This value is limited to 4.6 V maximum.
- The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	1.65	3.6	V
V _{IH}	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
	V _{CC} = 2.3 V to 2.7 V	1.7		
	V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
	V _{CC} = 2.3 V to 2.7 V	0.7		
	V _{CC} = 2.7 V to 3.6 V	0.8		
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	V _{CC} = 1.65 V	-4		mA
	V _{CC} = 2.3 V	-12		
	V _{CC} = 2.7 V	-12		
	V _{CC} = 3 V	-24		
I _{OL}	V _{CC} = 1.65 V	4		mA
	V _{CC} = 2.3 V	12		
	V _{CC} = 2.7 V	12		
	V _{CC} = 3 V	24		
Δt/Δv	Input transition rise or fall rate	10	ns/V	
T _A	Operating free-air temperature	-40	85	°C

- All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74ALVCH16825
18-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCES039D—JULY 1995—REVISED OCTOBER 2004

 **TEXAS**
INSTRUMENTS
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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	I _{OH} = -100 μ A	1.65 V to 3.6 V	V _{CC}	- 0.2		V
	I _{OH} = -4 mA	1.65 V		1.2		
	I _{OH} = -6 mA	2.3 V		2		
	I _{OH} = -12 mA	2.3 V		1.7		
		2.7 V		2.2		
		3 V		2.4		
V _{OL}	I _{OL} = -24 mA	3 V		2		V
	I _{OL} = 100 μ A	1.65 V to 3.6 V		0.2		
	I _{OL} = 4 mA	1.65 V		0.45		
	I _{OL} = 6 mA	2.3 V		0.4		
	I _{OL} = 12 mA	2.3 V		0.7		
		2.7 V		0.4		
I _I	I _{OL} = 24 mA	3 V		0.55		μ A
	V _I = V _{CC} or GND	3.6 V		\pm 5		
	V _I = 0.58 V	1.65 V		25		
	V _I = 1.07 V	1.65 V		-25		
	V _I = 0.7 V	2.3 V		45		
	V _I = 1.7 V	2.3 V		-45		
	V _I = 0.8 V	3 V		75		
I _{I(hold)}	V _I = 2 V	3 V		-75		μ A
	V _I = 0 to 3.6 V ⁽²⁾	3.6 V		\pm 500		
I _{OZ}	V _O = V _{CC} or GND	3.6 V		\pm 10		μ A
I _{CC}	V _I = V _{CC} or GND I _O = 0	3.6 V		40		μ A
Δ I _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		750		μ A
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	3.5		pF
	Data inputs			6		
C _o	Outputs	V _O = V _{CC} or GND	3.3 V	7.5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} = 2.5 V \pm 0.2 V	V _{CC} = 2.7 V	V _{CC} = 3.3 V \pm 0.3 V	UNIT		
			TYP	MIN	MAX	MIN	MAX		
t _{pd}	A	Y	(1)	1	4.1	3.9	1	3.4	ns
t _{en}	\overline{OE}	Y	(1)	1	6	5.7	1	4.7	ns
t _{dis}	\overline{OE}	Y	(1)	1.2	5.6	4.9	1.3	4.5	ns

(1) This information was not available at the time of publication.

OPERATING CHARACTERISTICS

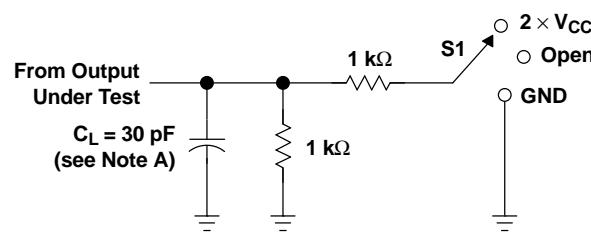
$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8 \text{ V}$	$V_{CC} = 2.5 \text{ V}$	$V_{CC} = 3.3 \text{ V}$	UNIT
		TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	Outputs enabled	(1)	16	18	pF
	Outputs disabled	(1)	4	6	

(1) This information was not available at the time of publication.

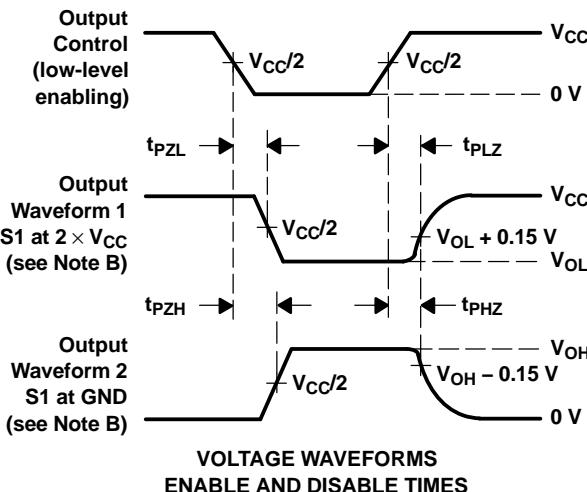
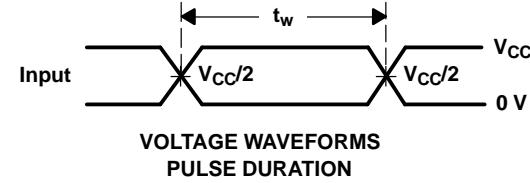
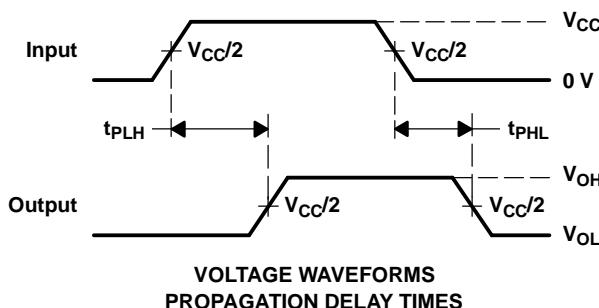
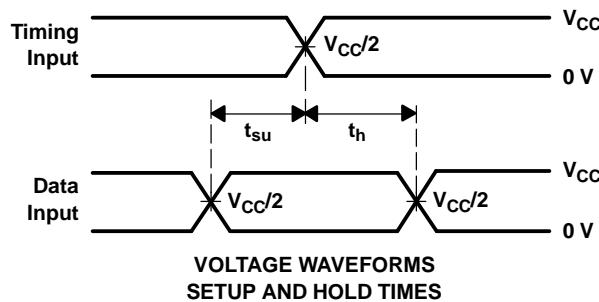
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8 \text{ V}$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



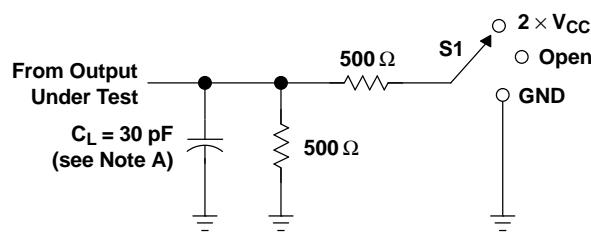
NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

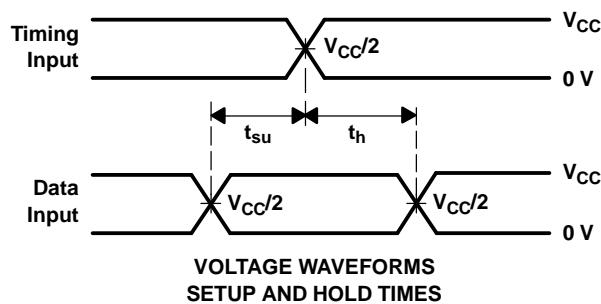
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

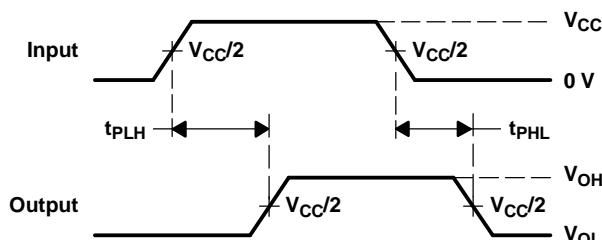


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

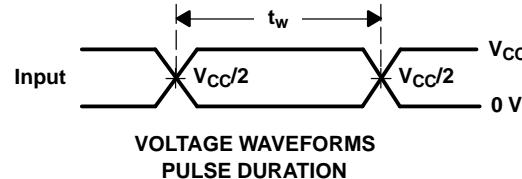
LOAD CIRCUIT



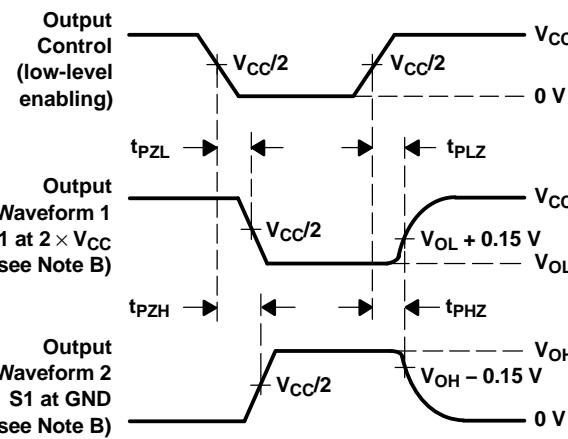
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

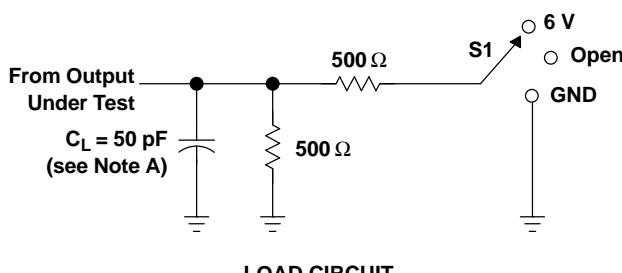
NOTES:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

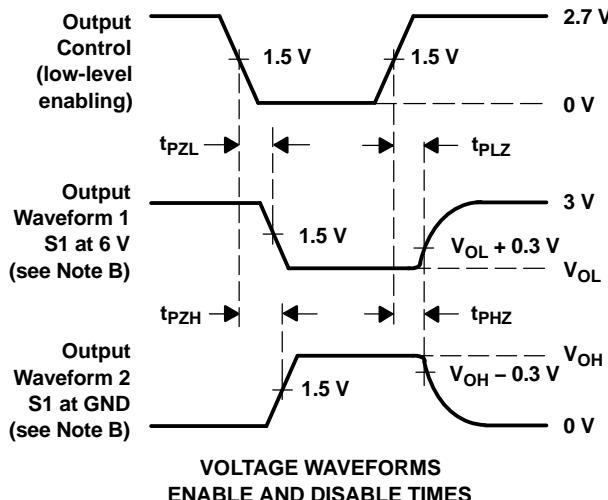
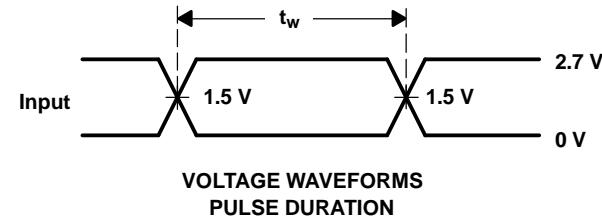
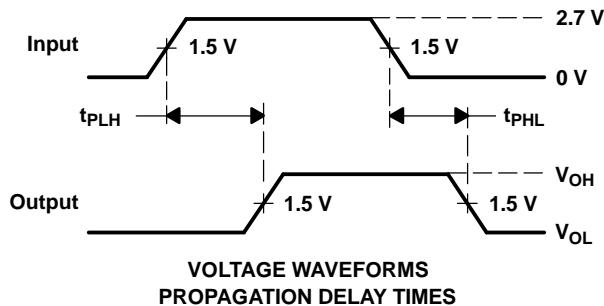
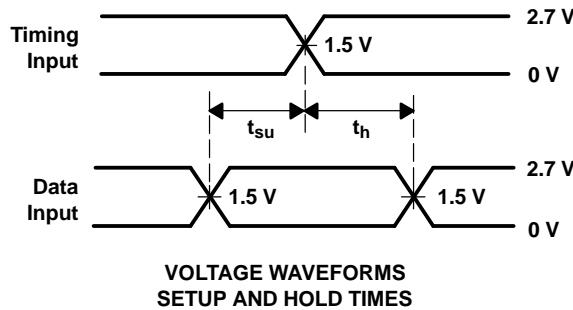
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND }3.3\text{ V} \pm 0.3\text{ V}$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ALVCH16825DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16825DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16825DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16825DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16825DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16825DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16825DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

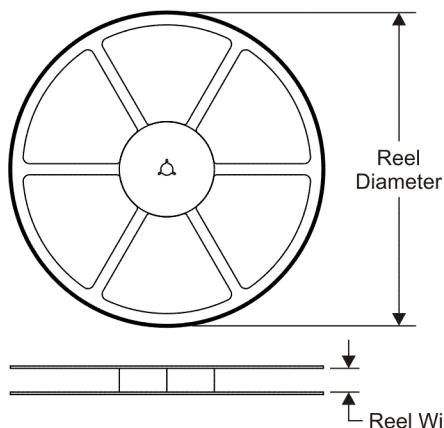
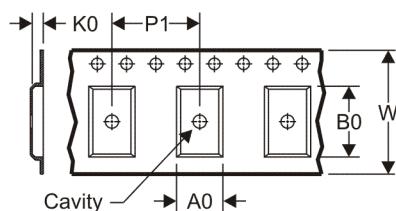
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

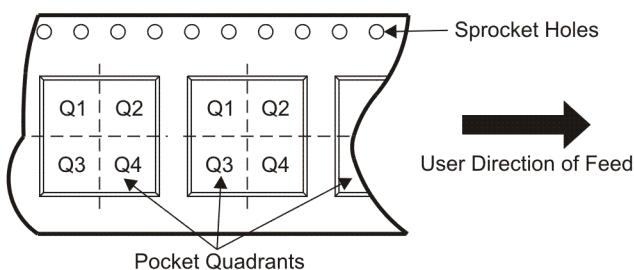
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


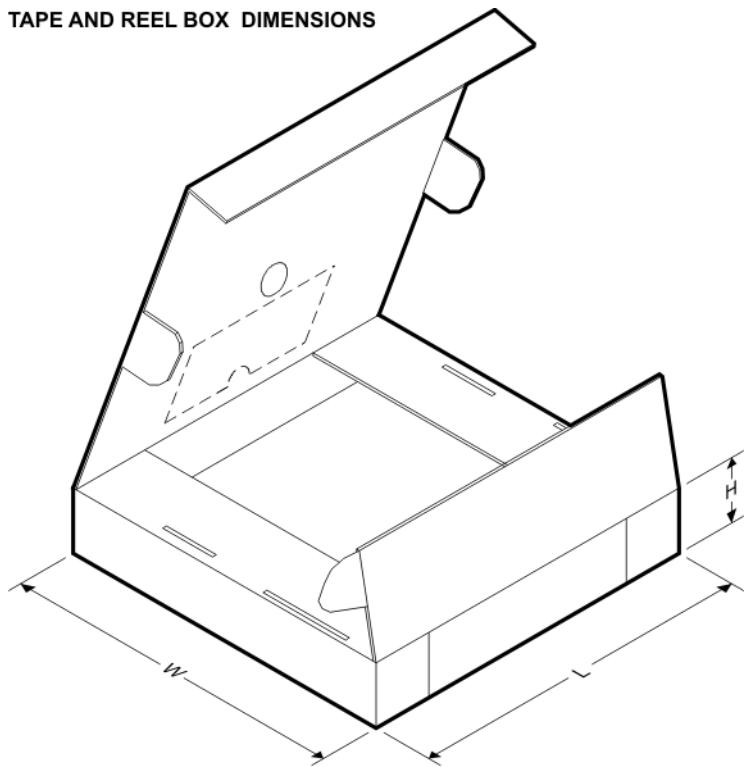
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH16825DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ALVCH16825DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



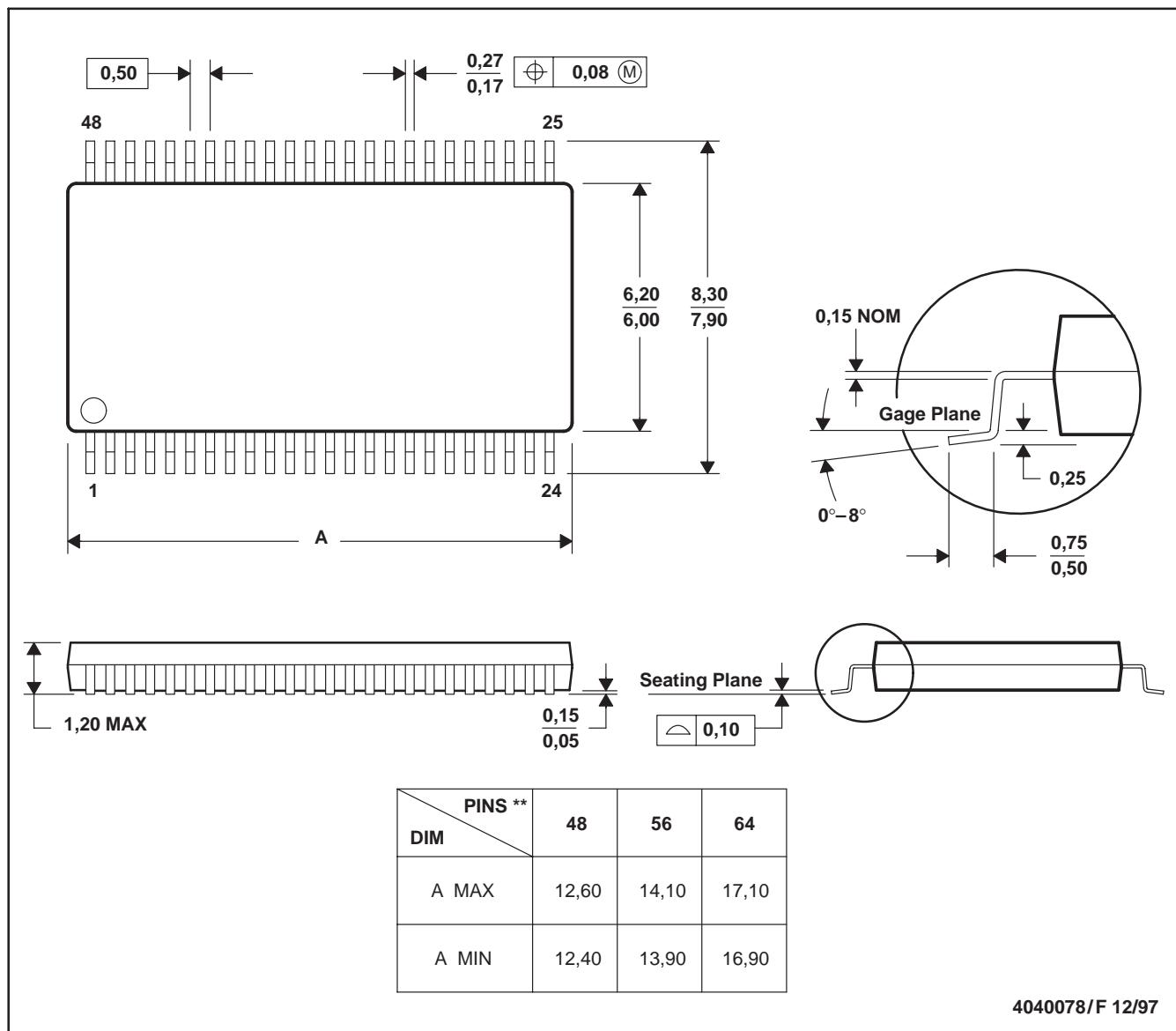
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH16825DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74ALVCH16825DLR	SSOP	DL	56	1000	346.0	346.0	49.0

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

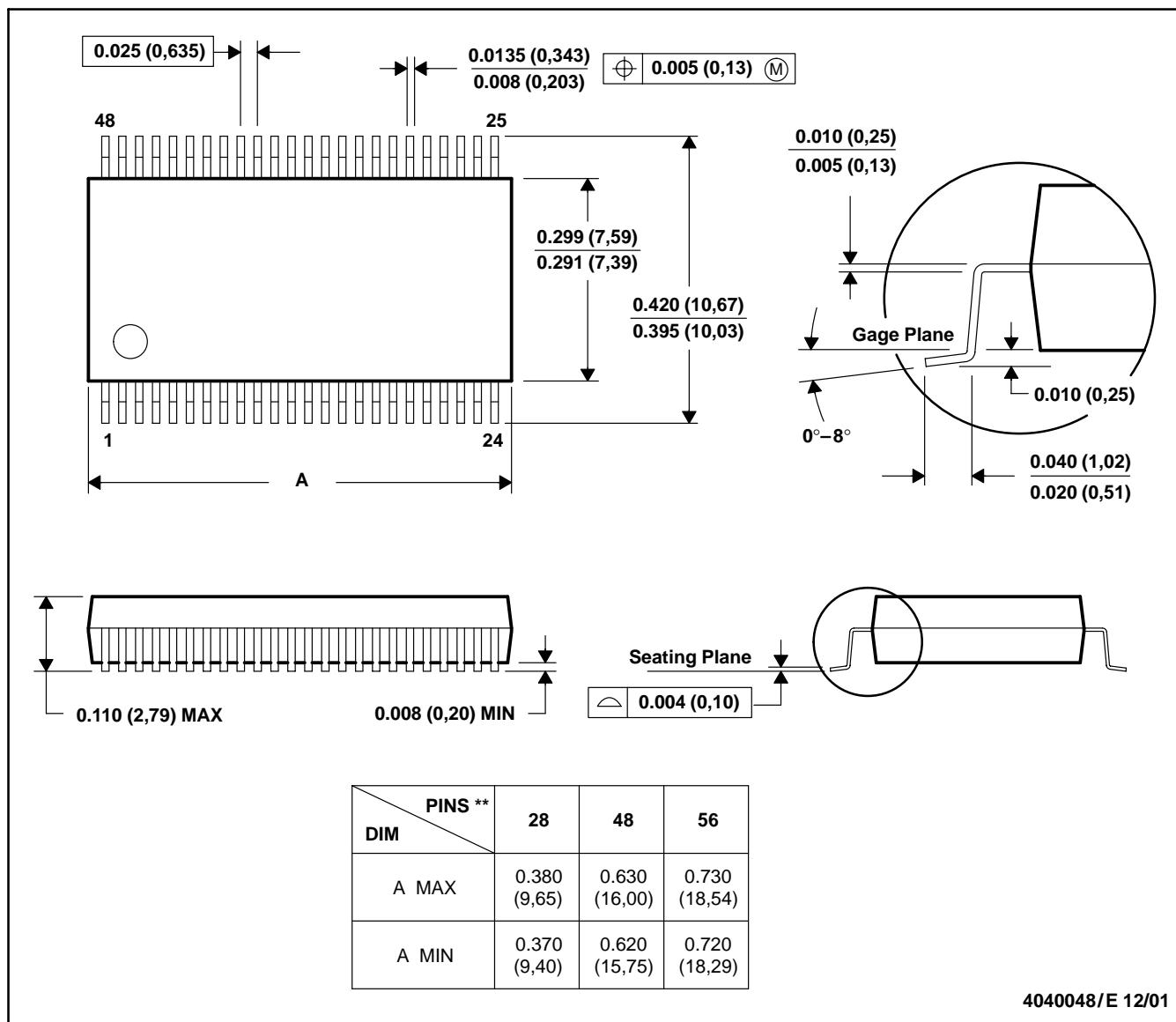


NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

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Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
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