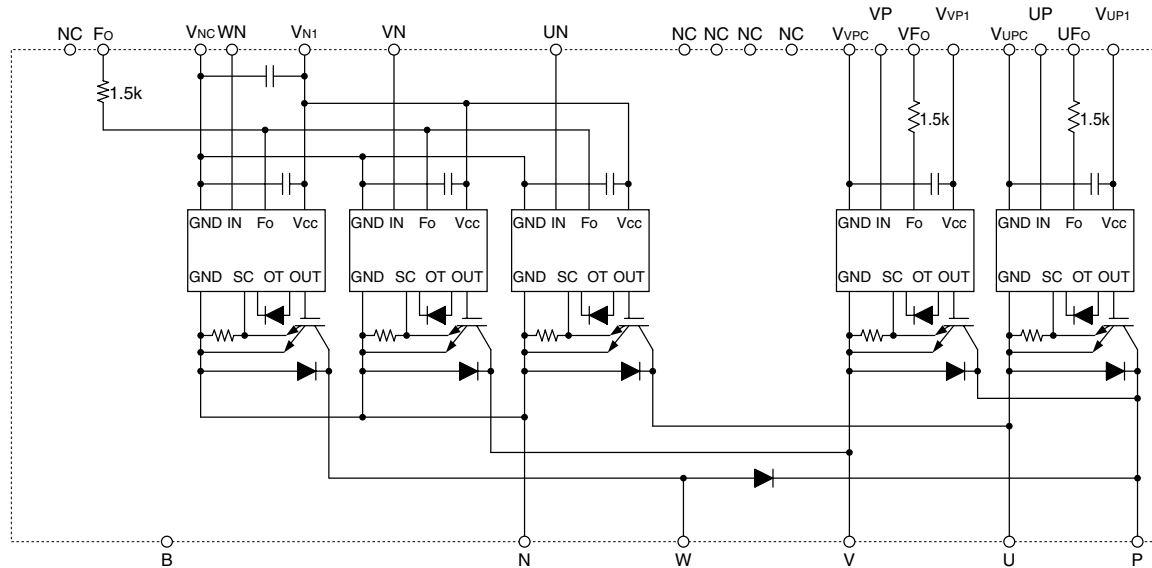


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FLAT-BASE TYPE
INSULATED PACKAGE

INTERNAL FUNCTIONS BLOCK DIAGRAM



MAXIMUM RATINGS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V _{CES}	Collector-Emitter Voltage	V _D = 15V, V _{CIN} = 15V	600	V
±I _C	Collector Current	T _c = 25°C	50	A
±I _{CP}	Collector Current (Peak)	T _c = 25°C	100	A
P _C	Collector Dissipation	T _c = 25°C	131	W
T _j	Junction Temperature		-20 ~ +150	°C

CONVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V _{CES}	Collector-Emitter Voltage	V _D = 15V, V _{CIN} = 15V	600	V
I _C	Collector Current	T _c = 25°C	50	A
I _{CP}	Collector Current (Peak)	T _c = 25°C	100	A
P _C	Collector Dissipation	T _c = 25°C (Note-1)	131	W
I _F	FWDi Forward Current	T _c = 25°C	50	A
V _{R(DC)}	FWDi Rated DC Reverse Voltage	T _c = 25°C	600	V
T _j	Junction Temperature		-20 ~ +150	°C

CONTROL PART

Symbol	Parameter	Condition	Ratings	Unit
V _D	Supply Voltage	Applied between : V _{UP1} -V _{UPC} V _{VPC} -V _{VPC} , V _{N1} -V _{N1}	20	V
V _{CIN}	Input Voltage	Applied between : U _P -V _{UPC} , V _P -V _{VPC} U _N • V _N • W _N -V _{N1}	20	V
V _{FO}	Fault Output Supply Voltage	Applied between : U _{FO} -V _{UPC} , V _{FO} -V _{VPC} , F _O -V _{N1}	20	V
I _{FO}	Fault Output Current	Sink current at U _{FO} , V _{FO} , F _O terminals	20	mA

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FLAT-BASE TYPE
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TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
V _{CC(prot)}	Supply Voltage Protected by SC	V _D = 13.5 ~ 16.5V, Inverter Part, T _j = +125°C Start	450	V
V _{CC(surge)}	Supply Voltage (Surge)	Applied between : P-N, Surge value	500	V
T _{stg}	Storage Temperature		-40 ~ +125	°C
V _{iso}	Isolation Voltage	60Hz, Sinusoidal, Charged part to Base, AC 1 min.	2500	V _{rms}

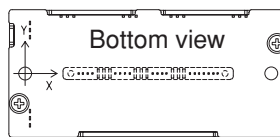
THERMAL RESISTANCES

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R _{th(j-c)Q}	Junction to case Thermal Resistances	Inverter IGBT part (per 1/4 module) (Note-1)	—	—	0.95	°C/W
R _{th(j-c)F}		Inverter FWDi part (per 1/4 module) (Note-1)	—	—	1.61	
R _{th(j-c)Q}		Converter IGBT part (Note-1)	—	—	0.95	
R _{th(j-c)F}		Converter FWDi upper part (Note-1)	—	—	0.95	
R _{th(j-c)F}		Converter FWDi lower part (Note-1)	—	—	1.61	
R _{th(c-f)}	Contact Thermal Resistance	Case to fin, (per 1 module) Thermal grease applied (Note-1)	—	—	0.038	

(Note-1) T_c (under the chip) measurement point is below.

(unit : mm)

arm axis	UP		VP		WP	UN		VN		WN	
	IGBT	FWDi	IGBT	FWDi	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi
X	32.7	32.2	62.8	63.3	82.9	38.8	39.3	53.0	52.5	75.6	75.1
Y	-10.0	-0.2	-8.8	-2.0	-8.4	8.0	0.8	3.8	-2.8	3.8	-2.8



ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V _{CE(sat)}	Collector-Emitter Saturation Voltage	V _D = 15V, I _C = 50A V _{CIN} = 0V (Fig. 1)	—	1.7	2.3	V
		T _j = 25°C T _j = 125°C	—	1.55	2.0	
V _{EC}	FWDi Forward Voltage	-I _C = 50A, V _D = 15V, V _{CIN} = 15V (Fig. 2)	—	2.2	3.3	V
t _{on}	Switching Time	V _D = 15V, V _{CIN} = 0V↔15V V _{CC} = 300V, I _C = 50A T _j = 125°C Inductive Load (Fig. 3,4)	0.3	0.7	1.4	μs
t _{rr}			—	0.1	0.2	
t _{c(on)}			—	0.2	0.4	
t _{off}			—	0.9	1.8	
t _{c(off)}			—	0.2	0.4	
I _{CES}	Collector-Emitter Cutoff Current	V _{CE} = V _{CES} , V _{CIN} = 15V (Fig. 5)	—	—	1	mA
		T _j = 25°C T _j = 125°C	—	—	10	

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FLAT-BASE TYPE
INSULATED PACKAGE

CONVERTER PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
VCE(sat)	Collector-Emitter Saturation Voltage	V _D = 15V, I _C = 50A	T _J = 25°C	—	1.7	2.3	V
		V _{CIN} = 0V, Pulsed (Fig. 1)	T _J = 125°C	—	1.55	2.0	
VEC	FWDi Forward Voltage	-I _C = 50A, V _{CIN} = 15V, V _D = 15V (Fig. 2)		—	2.2	3.3	V
VFM	Forward Voltage	I _F = 50A		—	1.9	3.0	V
ton	Switching Time	V _D = 15V, V _{CIN} = 0V↔15V V _{CC} = 300V, I _C = 50A T _J = 125°C Inductive Load (Fig. 3,4)		0.3	0.7	1.4	μs
trr				—	0.1	0.2	
tc(on)				—	0.2	0.4	
toff				—	0.9	1.8	
tc(off)				—	0.2	0.4	
ICES	Collector-Emitter Cutoff Current	VCE = VCES, V _D = 15V (Fig. 5)	T _J = 25°C	—	—	1	mA
			T _J = 125°C	—	—	10	

CONTROL PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
ID	Circuit Current	VD = 15V, V _{CIN} = 15V	V _{N1-VNC}	—	15	25	mA
			V _{P1-VPC}	—	5	10	
V _{th(ON)}	Input ON Threshold Voltage	Applied between : UP-VUPC, VP-VVPC UN • VN • WN-VNC		1.2	1.5	1.8	V
V _{th(OFF)}	Input OFF Threshold Voltage			1.7	2.0	2.3	
SC	Short Circuit Trip Level	−20 ≤ T _j ≤ 125°C, VD = 15V (Fig. 3,6)	Inverter part	100	—	—	A
			Converter part	100	—	—	
toff(SC)	Short Circuit Current Delay Time	VD = 15V (Fig. 3,6)		—	0.2	—	μs
OT	Over Temperature Protection	VD = 15V	Trip level	135	145	—	°C
OT _r		Detect T _j of IGBT chip	Reset level	—	125	—	
UV	Supply Circuit Under-Voltage Protection	−20 ≤ T _j ≤ 125°C	Trip level	11.5	12.0	12.5	V
UV _r			Reset level	—	12.5	—	
I _{FO(H)}	Fault Output Current	VD = 15V, V _{FO} = 15V (Note-2)		—	—	0.01	mA
I _{FO(L)}				—	10	15	
tFO	Minimum Fault Output Pulse Width	VD = 15V (Note-2)		1.0	1.8	—	ms

(Note-2) Fault output is given only when the internal SC, OT & UV protections schemes of either upper or lower arm device operate to protect it.

MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
—	Mounting torque	Mounting part screw : M5	2.5	3.0	3.5	N · m
—	Weight	—	—	340	—	g

RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Condition	Recommended value	Unit
V_{CC}	Supply Voltage	Applied across P-N terminals	≤ 450	V
V_D	Control Supply Voltage	Applied between : VUP1-VUPC, VVP1-VVPC V_{N1-VNC} (Note-3)	15 ± 1.5	V
$V_{CIN(ON)}$	Input ON Voltage	Applied between : UP-VUPC, VP-VVPC $U_N \cdot V_N \cdot W_N-VNC$	≤ 0.8	V
$V_{CIN(OFF)}$	Input OFF Voltage		≥ 9.0	
f_{PWM}	PWM Input Frequency	Using Application Circuit of Fig. 8	≤ 20	kHz
t_{dead}	Arm Shoot-through Blocking Time	For IPM's each input signals (Fig. 7)	≥ 2.0	μs

(Note-3) With ripple satisfying the following conditions : dv/dt swing $\leq \pm 5V/\mu s$, Variation $\leq 2V$ peak to peak

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FLAT-BASE TYPE
INSULATED PACKAGE

PRECAUTIONS FOR TESTING

- Before applying any control supply voltage (V_{DIN}), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state.
After this, the specified ON and OFF level setting for each input signal should be done.
- When performing "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
(These test should not be done by using a curve tracer or its equivalent.)

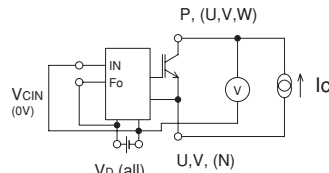


Fig. 1 $V_{CE(sat)}$ Test

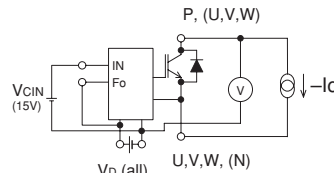


Fig. 2 V_{EC} , (V_{FM}) Test

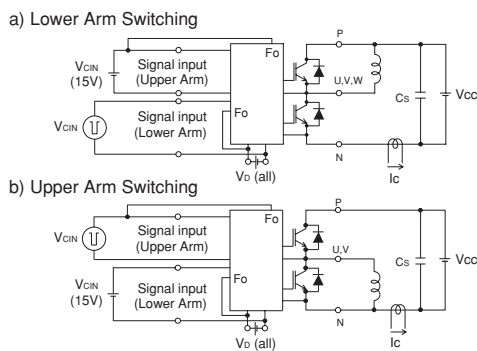


Fig. 3 Switching Time and SC Test Circuit

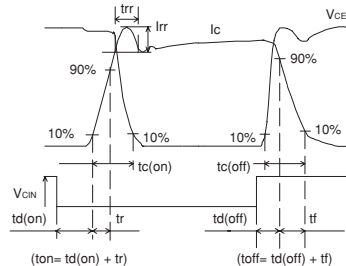


Fig. 4 Switching Time Test Waveform

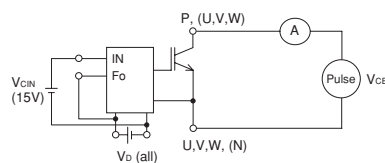


Fig. 5 I_{CES} Test

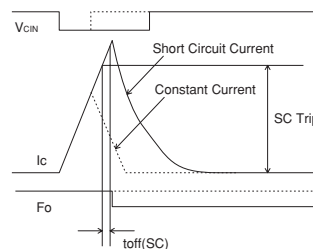
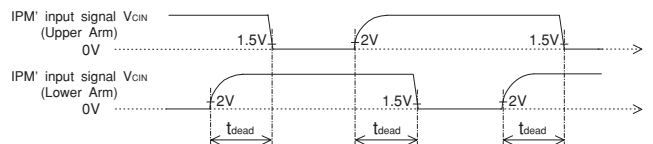


Fig. 6 SC Test Waveform



1.5V: Input on threshold voltage $V_{th(on)}$ typical value, 2V: Input off threshold voltage $V_{th(off)}$ typical value

Fig. 7 Dead Time Measurement Point Example

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FLAT-BASE TYPE
INSULATED PACKAGE

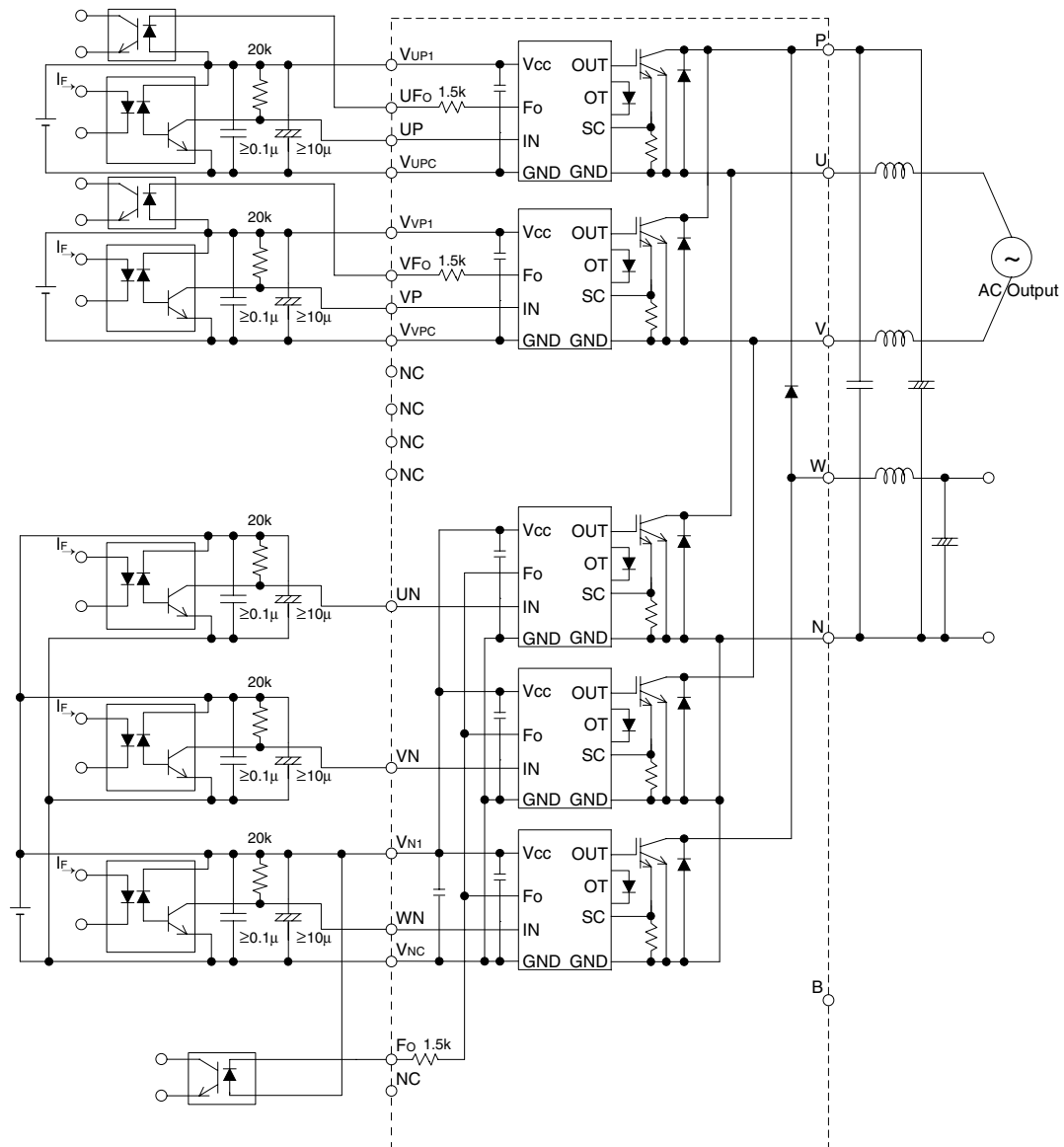


Fig. 8 Application Example Circuit

NOTES FOR STABLE AND SAFE OPERATION ;

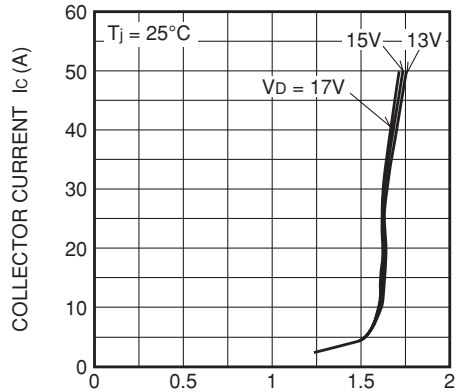
- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers: t_{PLH} , $t_{PHL} \leq 0.8\mu s$, Use High CMR type.
- Slow switching opto-coupler: CTR > 100%
- Use 3 isolated control power supplies (VD). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.

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FLAT-BASE TYPE
INSULATED PACKAGE

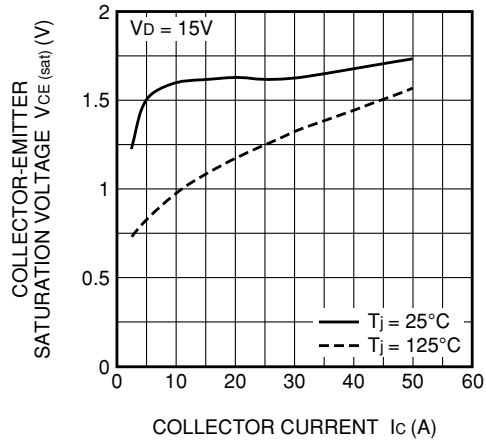
PERFORMANCE CURVES (INVERTER PART)

OUTPUT CHARACTERISTICS
(TYPICAL)

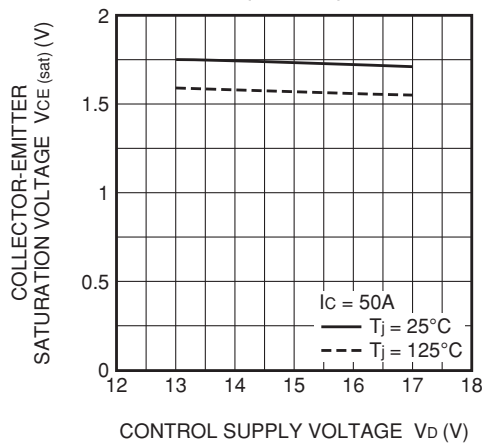


COLLECTOR-EMITTER SATURATION VOLTAGE $V_{ce(sat)}$ (V)

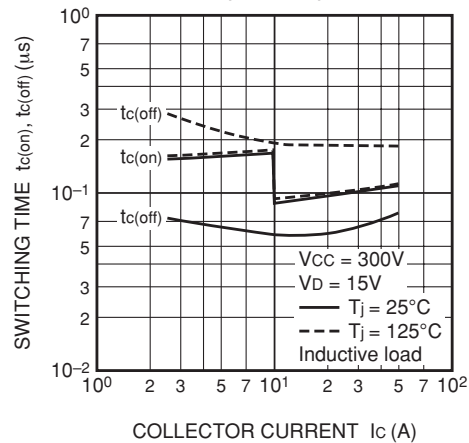
COLLECTOR-EMITTER SATURATION
VOLTAGE (VS. I_c) CHARACTERISTICS
(TYPICAL)



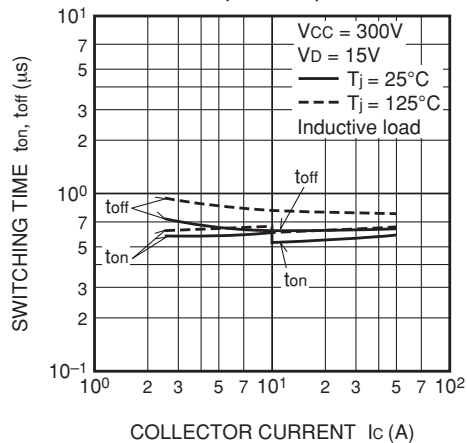
COLLECTOR-EMITTER SATURATION
VOLTAGE (VS. V_d) CHARACTERISTICS
(TYPICAL)



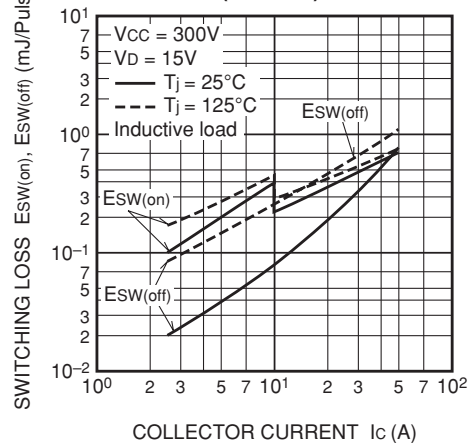
SWITCHING TIME CHARACTERISTICS
(TYPICAL)



SWITCHING TIME CHARACTERISTICS
(TYPICAL)



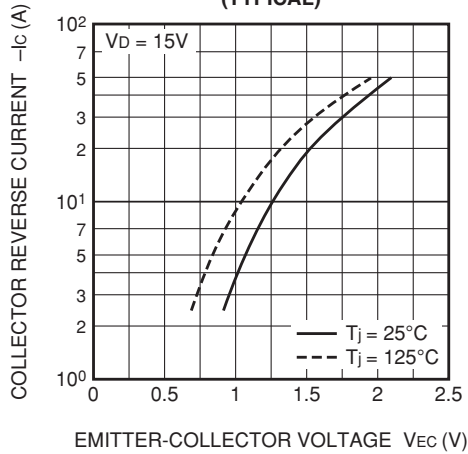
SWITCHING LOSS CHARACTERISTICS
(TYPICAL)



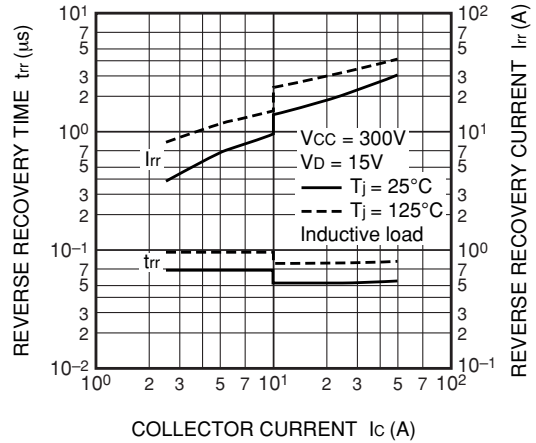
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FLAT-BASE TYPE
INSULATED PACKAGE

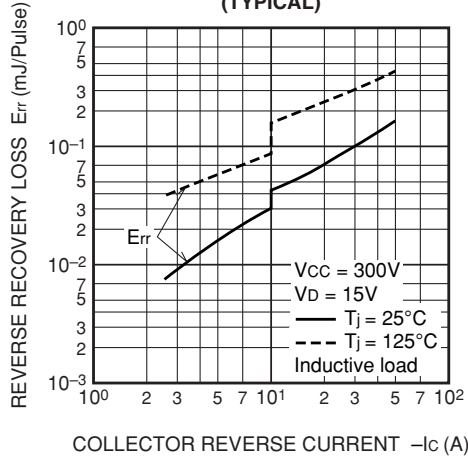
**FWDi FORWARD VOLTAGE CHARACTERISTICS
(TYPICAL)**



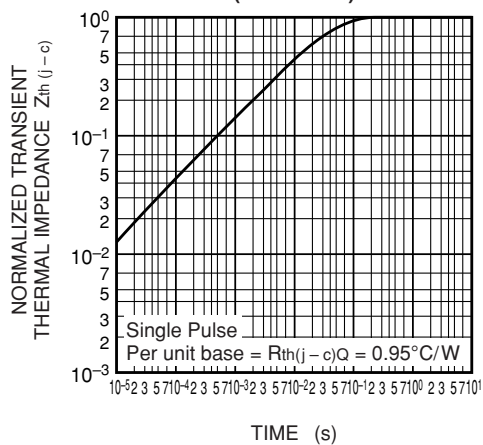
**FWDi REVERSE RECOVERY CHARACTERISTICS
(TYPICAL)**



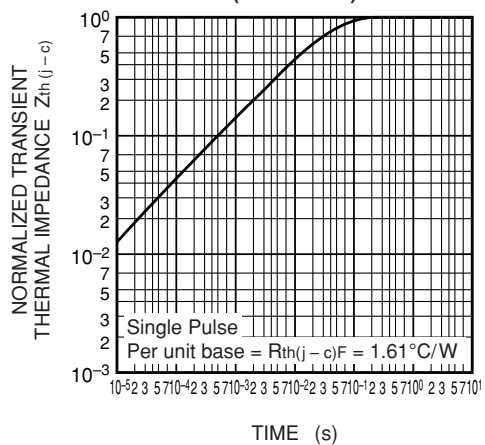
**FWDi REVERSE RECOVERY LOSS CHARACTERISTICS
(TYPICAL)**



**TRANSIENT THERMAL
IMPEDANCE CHARACTERISTICS
(IGBT PART)**



**TRANSIENT THERMAL
IMPEDANCE CHARACTERISTICS
(FWDi PART)**

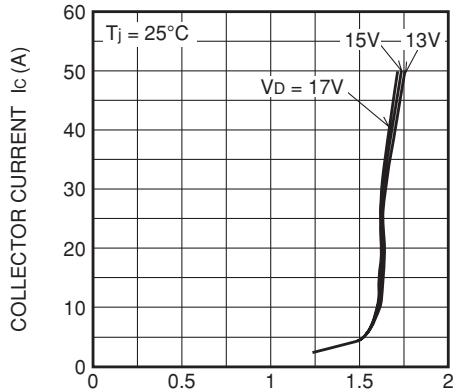


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FLAT-BASE TYPE
INSULATED PACKAGE

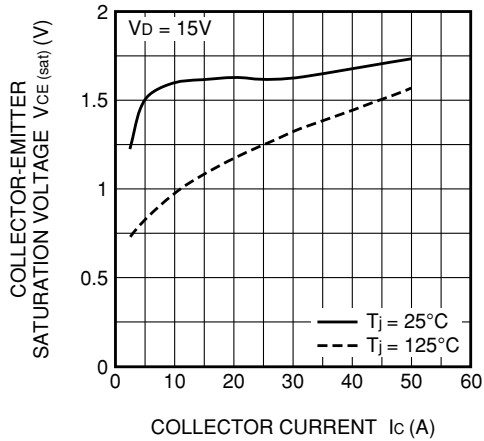
(CONVERTER PART)

OUTPUT CHARACTERISTICS
(TYPICAL)

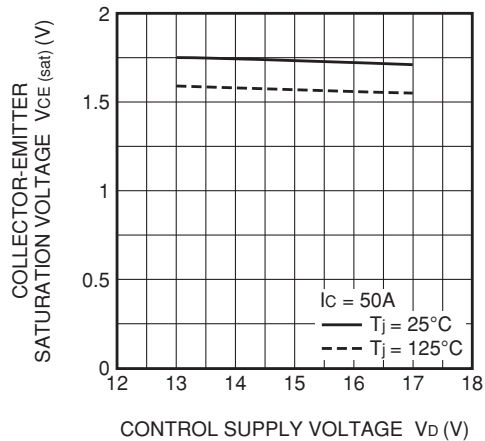


COLLECTOR-EMITTER SATURATION VOLTAGE $V_{CE(sat)}$ (V)

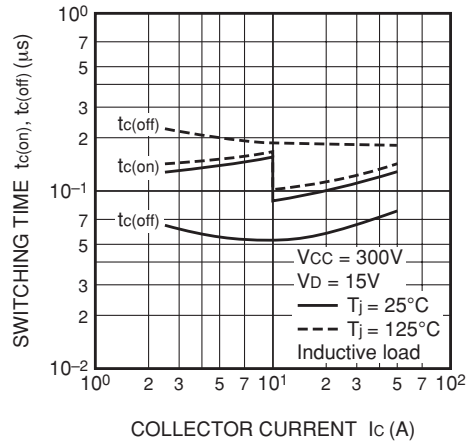
COLLECTOR-EMITTER SATURATION
VOLTAGE (VS. I_c) CHARACTERISTICS
(TYPICAL)



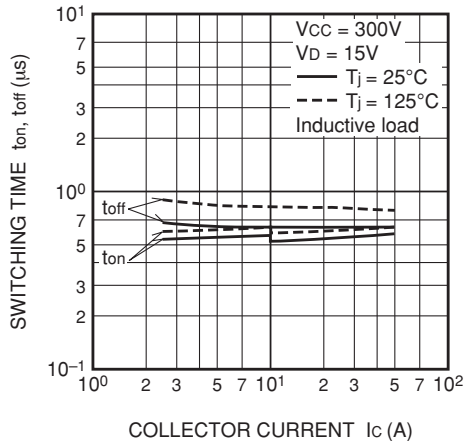
COLLECTOR-EMITTER SATURATION
VOLTAGE (VS. V_d) CHARACTERISTICS
(TYPICAL)



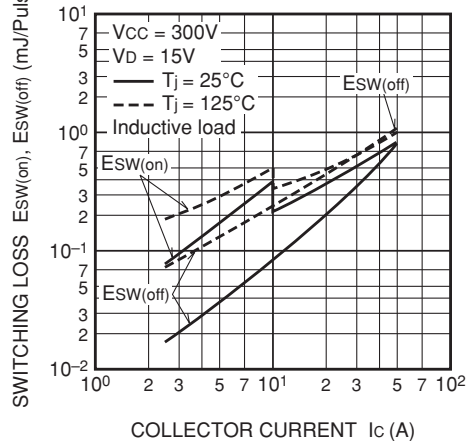
SWITCHING TIME CHARACTERISTICS
(Lower Arm - TYPICAL)



SWITCHING TIME CHARACTERISTICS
(Lower Arm - TYPICAL)



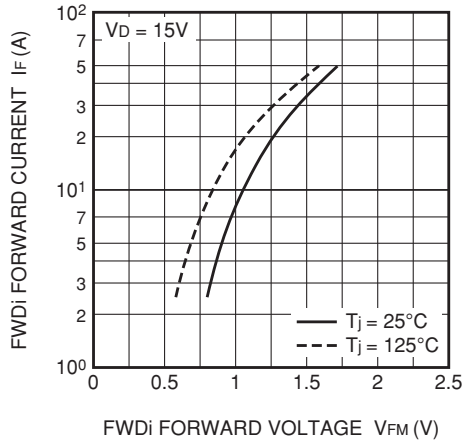
SWITCHING LOSS CHARACTERISTICS
(Lower Arm - TYPICAL)



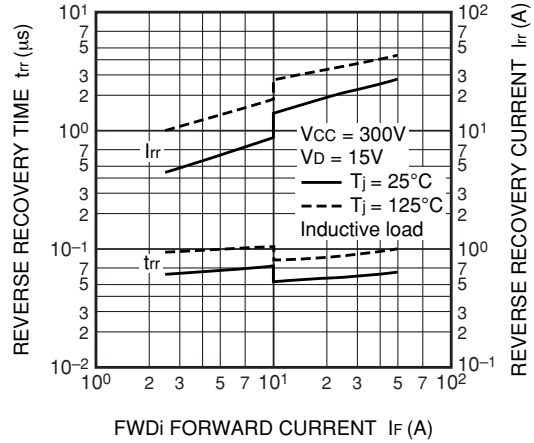
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FLAT-BASE TYPE
INSULATED PACKAGE

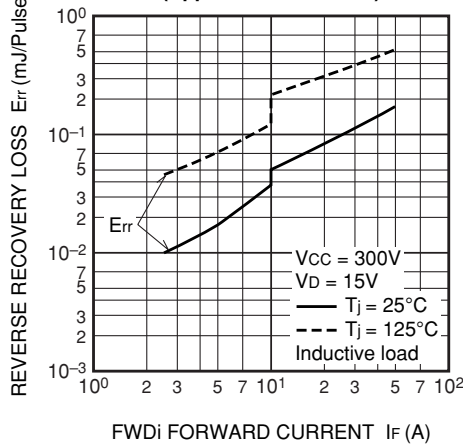
FWDi FORWARD VOLTAGE CHARACTERISTICS
(Upper Arm · TYPICAL)



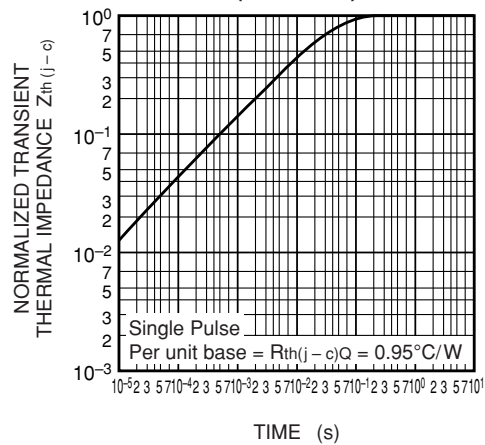
FWDi REVERSE RECOVERY CHARACTERISTICS
(Upper Arm · TYPICAL)



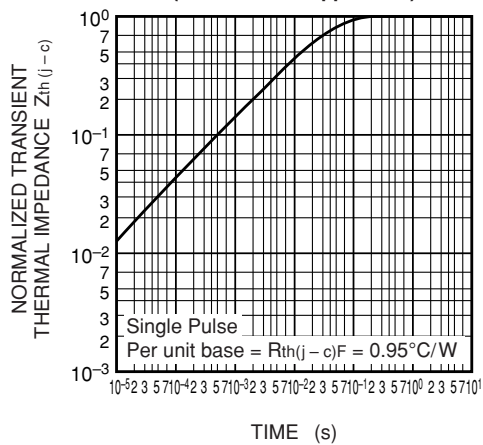
FWDi REVERSE RECOVERY LOSS CHARACTERISTICS
(Upper Arm · TYPICAL)



TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS
(IGBT PART)



TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS
(FWDi PART · Upper Arm)



TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS
(FWDi PART · Lower Arm)

